A low-power small-area 6T SRAM cell for tracking detector applications

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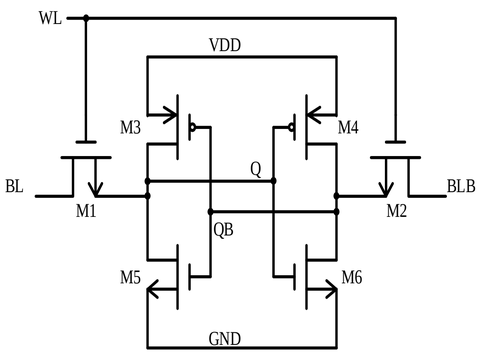
Introduction

Pixel detectors have been widely used for high energy particle physics and medical applications, which play a role of energy measurement, tracking detection and time of arrival measurement [1] [2] [3]. To improve detection efficiency, it is necessary to reduce the threshold. However the fake hit rate increases significantly if the dispersion of the threshold is large. Hence it is important to improve the threshold uniformity. The most direct method is by increasing the area of the transistor, but it deteriorates the spatial resolution. The other method is tuning the threshold of each pixel, which is composed of course and fine adjustment. As usual, the fine adjustment is realized by in-pixel Digital-to-Analog Convertor (DAC) with registers of the corresponding bit number. The conventional D-type Flip Flop (DFF) register can be competent to store the input data of the DAC [2]. However, DFF registers have large area and large power consumption, especially for more bits. Compared to DFF registers, the conventional six-transistor (6T) Static Random Access Memory (SRAM) cell reduce both area and power consumption. In this paper, we propose a novel 6T SRAM cell for the configuration in tracking detectors. The proposed 6T SRAM cell only uses one bit line instead of two bit lines and cuts the competition path during the writing phase to reduce more power consumption compared to the conventional 6T SRAM cell.

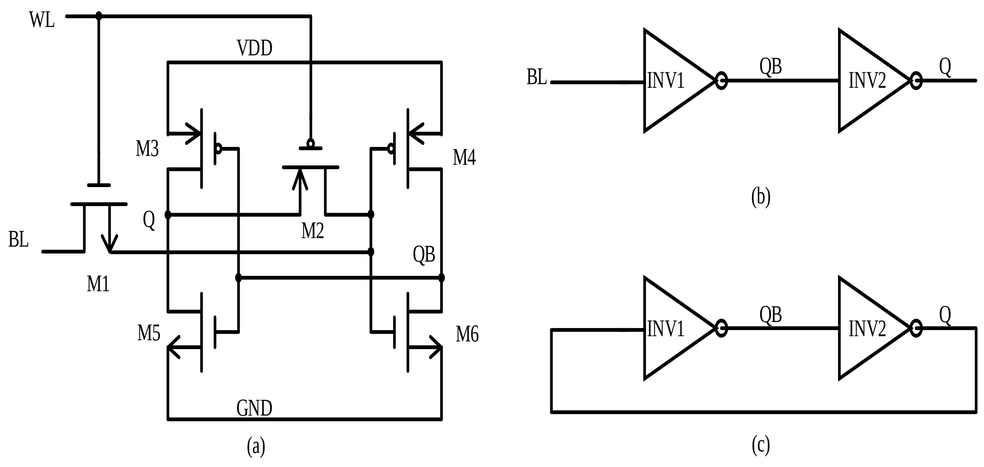
Conventional 6T SRAM cell



The conventional 6T SRAM cell is composed of two cross-coupled inverters (M3~M6) and two access transistors (M1, M2. There are three operating modes in SRAM, write, read and hold.

- ✓ **Write :** BL and BLB are precharged to VDD. WL is connected to VDD. Meanwhile, the bit-line pairs is driven to VDD and GND to flip the SRAM cell state, respectively.
- ✓ **Read:** BL and BLB are precharged to VDD. WL is connected to VDD. The internal node of "0" voltage level pulls down the corresponding bit line toward ground voltage.
- ✓ **Hold:** WL is connected to GND. The cross-coupled inverters must maintain a bi-stable operation point to hold its state correctly.

Proposed 6T SRAM cell



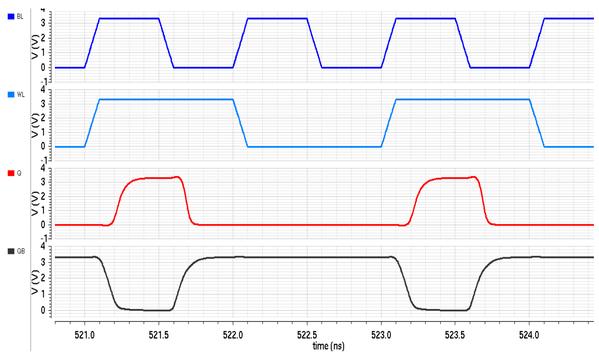
The proposed 6T SRAM cell consists of two cross-coupled inverters (M3~M6), one access transistor (M1) and a cut-off transistor (M2). Compared to the conventional SRAM cell, only a single bit line substitutes two complementary bit lines but an additional cut-off transistor M2 is added. The write operation depends on cutting off the feedback connection between the two inverters. The p-type transistor M2 and the n-type transistor M1 are both controlled by WL. Before the write operation, the WL is set to be high level. M1 is turned on while M2 is turned off. Hence, during the write operation, the cell can be simplified to two cascaded inverters, INV1 followed by INV2. The data of the cell only depends on a single bit line during the write operation. Hence, the bit line bar is reduced in the proposed 6T SRAM cell. The data is written through the bit line and the access transistor M1. While the complementary output data (Q and QB) is directly driven by the two cross-coupled inverters.

The dynamic power consumption is given by the following equation.

$$\mathrm{P} = \mathrm{I} * \mathrm{U} = \frac{Q}{t} * U = \frac{C * U}{t} * U = C * U^2 * f$$

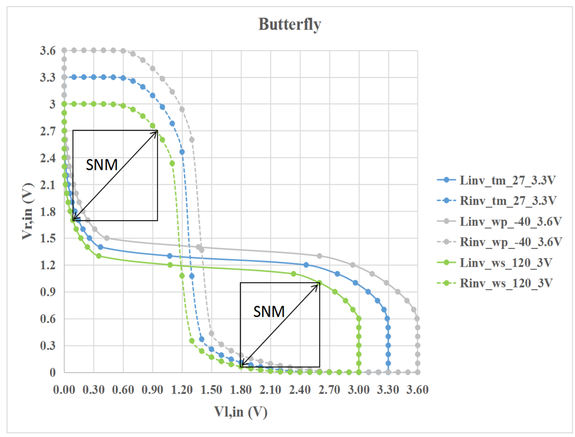
where P is power consumption, I is current, U is the voltage across the bit line, C is the capacitance load of the bit line, t is integration time and f is the writing frequency. Compared to the conventional 6T SRAM cell, the power consumption of the proposed 6T SRAM cell can be reduced half since it only uses one bit line. The cut-off transistor M2 eliminates the completion between the cross-coupled inverters during the writing operation. Even though the both width and length of transistors in the cross-coupled inverters is minimum, the writing operation can also be correct. The area of the proposed 6T SRAM cell is also smaller than that of the conventional 6T SRAM cell.

Waveform of write operation



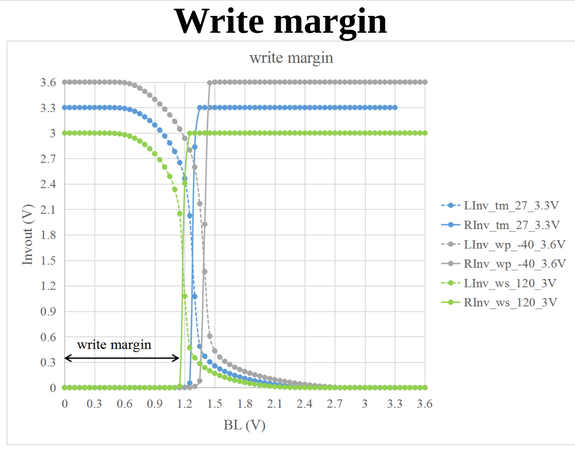
According to the write waveform, the outputs of both Q and QB depend on the BL signal. When the WL signal is at high level voltage, the output Q follows the BL signal with a delay of 137 ps from "1" to "0" and 184 ps from "0" to "1". When the WL signal is at low level voltage, the outputs Q and QB is kept its previous value, respectively.

Butterfly



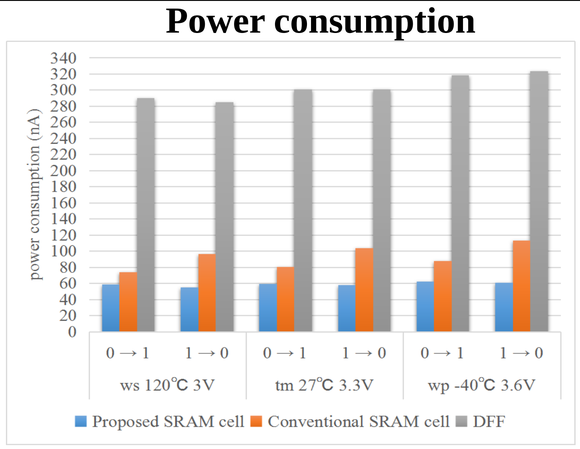
A graphical technique called as a "butterfly curve" is usually used to determine the SNM. Only Static noise is taken into account for the analysis of SNM in this paper. A basic understanding of the SNM is obtained by drawing and mirroring the inverter characteristics and finding the maximum possible square between them. The SNM is calculated when the WL is set low level. The SNM value under the case of Process = worst speed, Voltage = 3V, Temperature = 120℃ is 1.131V, which is the minimum value among the three PVTs.

Write margin



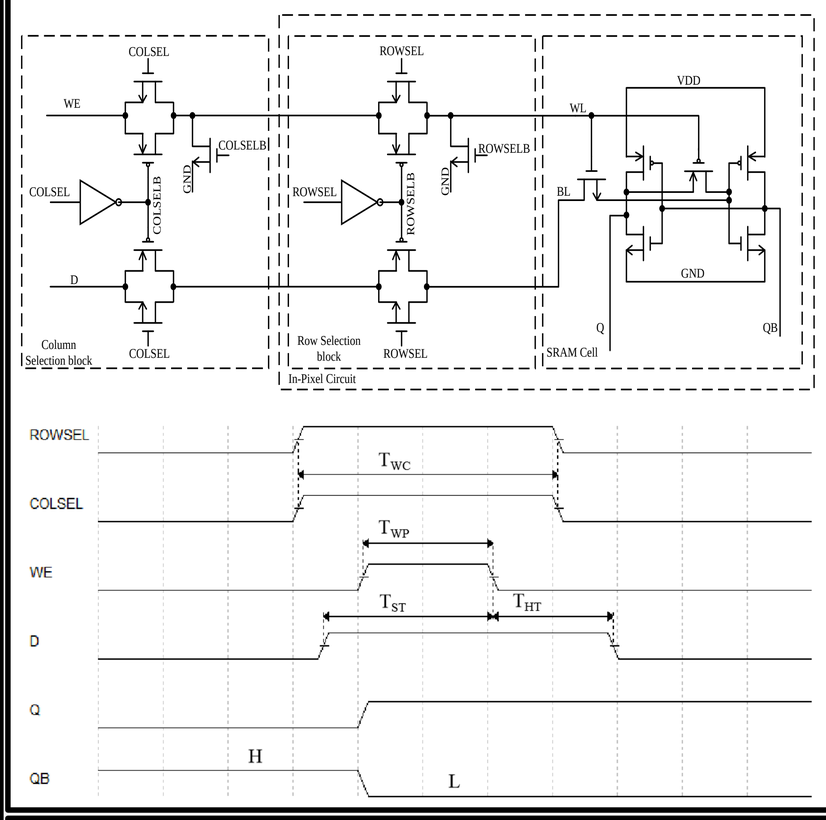
A minimum bit line voltage required to flip the state of the SRAM cell is called write margin. It is used to measure the ability to write data into the SRAM cell. The minimum write margin is about 1.15V.

Power consumption



Compared to the conventional SRAM cell and DFF, the power consumption of the proposed SRAM cell is reduced by 20% and 80% during the rising edge, respectively, and is decreased by 43% and 81% during the falling edge, respectively.

Application in pixel array detector

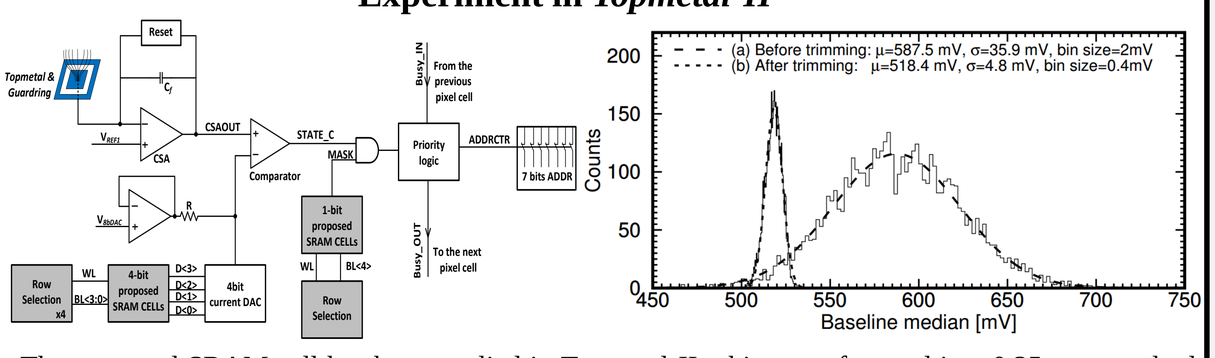


The schematic of the configuration cell for pixel detectors is composed of a column selection block, a row selection block and a SRAM cell.

The column selection block is located in the bottom of each column, and shared among pixels in the same column. While the row selection block and the SRAM cell is located in each pixel. The data is configured pixel by pixel through COLSEL and ROWSEL signals.

After configurations, the configuration data is stored in the SRAM cell. The signal Q or QB is fed directly into the input of the DAC.

Experiment in *Topmetal-II-*



The proposed SRAM cell has been applied in Topmetal-II- chip manufactured in a 0.35 μm standard process. The *Topmetal-II-* chip is composed of 72 x 72 pixels and periphery circuitry. 5-bit proposed SRAM cells and row selection circuits are designed in each pixel, of which 4 bits are used to store the input data of the 4-bit current DAC and another 1 bit is used to store a MASK signal. The 4-bit current DAC tunes the threshold of the comparator in each pixel individually. The MASK signal is used to disable a dead pixel. Each SRAM cell has its own bit line while all 5-bit SRAM cells share only one word line. After trimming, the dispersion of the threshold is reduced from 35.9 mV down to 4.8 mV. It can be concluded that the proposed SRAM cell works very well.

Conclusions

This paper presents a novel six-transistor (6T) Static Random Access Memory (SRAM) cell, which uses only one bit line and applies an additional switch to cut the competition path during the write access. The proposed 6T SRAM cell has been applied in a pixel array detector to configure a digital-to-analog converter in each pixel to improve the charge threshold uniformity. Compared to the conventional 6T SRAM cell, the proposed 6T SRAM bit cell features smaller area and lower power consumption. Simulation results show the power consumption is reduced by about 44% and the area is decreased by about 25% without the performance degradation. The measurement results show that the proposed 6T SRAM cell works very well.

References

[1] N. Wermes, "Pixel detectors for charged particles", Nuclear Inst. and Methods in Physics Research A 604 (2009) 370–379 (DOI: 10.1016/j.nima.2009.01.098)
[2] Rafael Ballabriga, Michael Campbell, Xavier Llopart, "Asic developments for radiation imaging applications: The medipix and timepix family", Nuclear Inst. and Methods in Physics Research, A 878 (2018) 10–23 (DOI: 10.1016/j.nima.2017.07.029)
[3] W. Snoeys, "Monolithic pixel detectors for high energy physics", Nuclear Inst. and Methods in Physics Research A 731 (2013) 125–130 (DOI: 10.1016/j.nima.2013.05.073)