

## A low-power small-area 6T sram cell for tracking detector applications

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This paper presents a low-power small-area six-transistor (6T) SRAM cell, which uses only one bit line and applies an additional switch to cut the competition path during the write access. The proposed 6T SRAM cell has been applied in a pixel array detector to configure a Digital-to-Analog Converter (DAC) in each pixel to improve the charge threshold uniformity. Compared to the conventional 6T SRAM cell, simulation results show the power consumption is reduced by about 44% and the area is decreased by about 25% without the performance degradation. The measurement results show that the novel 6T SRAM cell works very well.

Pixel detectors have been widely used for high energy particle physics and medical applications, which play a role of energy measurement, tracking detection and time of arrival measurement. They are developed toward the trend of large scale, high resolution and low power consumption. To improve detection efficiency, it is necessary to reduce the threshold and improve the threshold uniformity. An effective method is tuning the threshold of each pixel, which is composed of coarse and fine adjustment. As usual, the fine adjustment is realized by in-pixel DAC with registers of the corresponding bit number. The conventional D-type Flip Flop (DFF) register can be competent to store the input data of the DAC. However, DFF registers have large area and power consumption, especially for more bits. Compared to DFF registers, the conventional six-transistor (6T) SRAM cell reduces both area and power consumption. The proposed 6T SRAM cell reduces more power consumption compared to the conventional 6T SRAM cell.

In the conference, we will introduce the structure and performance of the proposed 6T SRAM cell in detail. We will also show the improvement of the threshold uniformity of a pixel detector after the proposed 6T SRAM cell is applied.

### Submission declaration

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