Module Development for the Phase-2 ATLAS ITk Pixel Upgrade

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Abstract
In the high luminosity era of the Large Hadron Collider, the instantaneous luminosity is expected to reach unprecedented values resulting in up to 200 proton-proton interactions per bunch crossing. To cope with the resultant increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk). The innermost part of ITk will consist of a state-of-the-art pixel detector, with an active area of about 14 m². Because of the extremely high radiation environment the sensors will operate at low temperature, • Coolant temp -45°C • Sensor temp -25°C rising to 0°C over 10 yrs • Operational temperature range (OTR) +60°C -> -55°C • -55°C would be caused by a coolant leak • Large temp range introduces thermal stress/strain due to CTE mismatch in the module
This poster presents work done to understand and mitigate this stress/strain.

Requirements and Testing
The QA/QC testing regime for the modules state that the modules must survive one cycle over the OTR, a number of +40°C -> -40°C cycles and a 48hr burn in. Trials were carried out to test for bump disconnection over both ranges. Even at the lower range there were significant BB disconnections.
FEA analysis was used to determine which of the components of the flex was contributing most to the BB stress. Linear models were used initially to estimate stress in the bump bond (BB) layer and to get appropriate values. The copper layer was shown to have the most effect and the thickness was limited to 25μm after these models.

Non-linear viscoplastic solder model
FEI4 chips, 80x336 pixels on a 250x50μm pitch were used to develop the technique before modelling an ITK PiP chip. This has 400x368 pixels per chip with a 50x50μm pitch. These large models run using symmetry with 25 densely meshed bumps in the high stress/strain region at the corner with the interior being more coarse. These were initially used to match FEA to lab results by calculating cycles to failure for FEI4 modules from the shear strain using the modified Coffin-Manson law which includes the effect of the thermal cycle frequency and range

Parylene coating
Further mitigation of the thermal stress in the BB layer comes from parylene coating which is the baseline for HV protection. This plot shows even FEI4 modules with thick Cu layers can survive hundreds of thermal cycles with no additional disconnects after parylene coating. This is additional security that the modules will be suitable for use in the challenging environment.

Future work
Continue modelling ITK Pix scale devices to show the effects of long term creep on the BB. New flex with ~25μm of copper have been produced and will be tested in the lab using real devices and daisy chain structures.