Results from the CBC3.1 readout ASIC for CMS 2S-modules

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CBC3.1

The CBC3.1 is the final version of the CMS Binary Chip (CBC) for readout of the outer regions of the upgraded CMS Tracker at the High Luminosity LHC (HL-LHC). The 254-channel, 130 nm CMOS ASIC is designed to be bump-bonded to a hybrid substrate to which two sensors will be wire-bonded. It will instrument double-layer 2S-modules, containing two overlaid silicon microstrip sensors, closely spaced and aligned along the direction of the strips. On-chip logic identifies Level-1 trigger primitives from high transverse-momentum tracks by identifying correlated clusters in the two sensors [1].

The first version of the CBC [2] was designed based on the current CMS outer tracker readout chip, APV, but targeted for the upgraded tracker and HL-LHC conditions. The second version, the CBC2 [3], was designed with the necessary logic to correlate clusters and provide information to the Level-1 trigger. The CBC3.0 [4] was the first that was designed to satisfy all the requirements for the final system and was produced in 2016. Since then, the CBC3.0 has undergone module tests, beam tests, wafer probing, TID test and SEU test [5], [6].

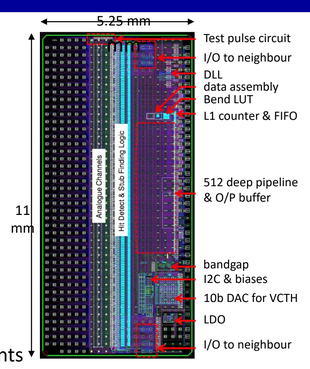
The CBC3.1 was designed including some optimization based on the test result on the CBC3.0 while keeping the interface unchanged. Total 61 wafers, with 478 chips on each wafer, have been produced and tested on a probe station so far. Testing proved that the CBC3.1 design solved some minor timing issues discovered in the CBC3.0. The average yield of the wafers is above 80%, with spread of around 5 - 10 % for the three different lots. A TID test was performed and less than a 1% increase in the total power consumption of a module was estimated, unchanged from the CBC3.0. Testing the CBC3.0 for SEUs uncovered a vulnerability in the I2C registers and a small optimization was made for the CBC3.1. A subsequent test revealed that while the SEU vulnerabilities in the chip are not yet fully understood, the rate of SEUs in the I2C registers for the CBC3.1 is reduced and would result in an upset rate of ~0.01 /hour per CBC at HL-LHC, which is well within requirements [7].

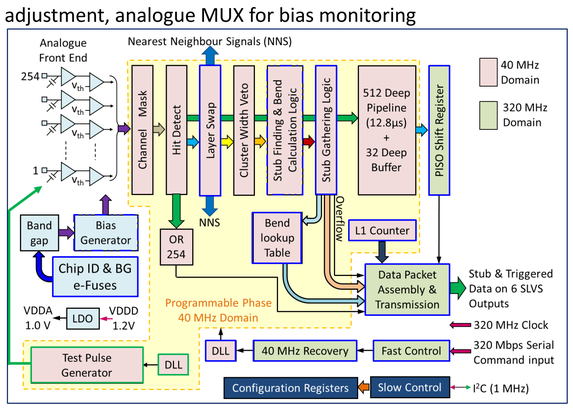
Measured characteristics

- **The noise -** Less than 1000 e for external capacitance up to 10 pF.
- **The signal shape -** Stable with 15 ns of peaking time and coming back to the pedestal in 50 ns for injected charge up to 10.0 fC and external capacitance up to 12 pF.
- **Gain -** The CBC has a global threshold, VCTH, and the offset adjustment is done for each channel. With the adjustment, the gain and the spread was measured to be about 47 mV/fC and 5%, respectively.
- **The power consumption -** 350 µW for analogue and 160 µW for digital circuit per channel.
- HIP (Highly Ionising Particle) suppression - The logic suppresses a tail of a signal created by a HIP event. The tail could last more than 1 µs on a couple of channels and the logic is to suppress this to avoid for false triggers to be generated. The expected performance of the logic was confirmed with external capacitance of 4pC.

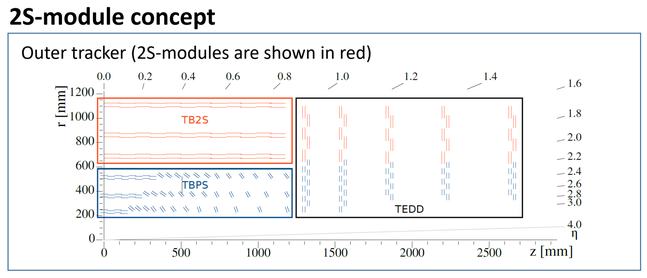
CBC3.1 chip summary

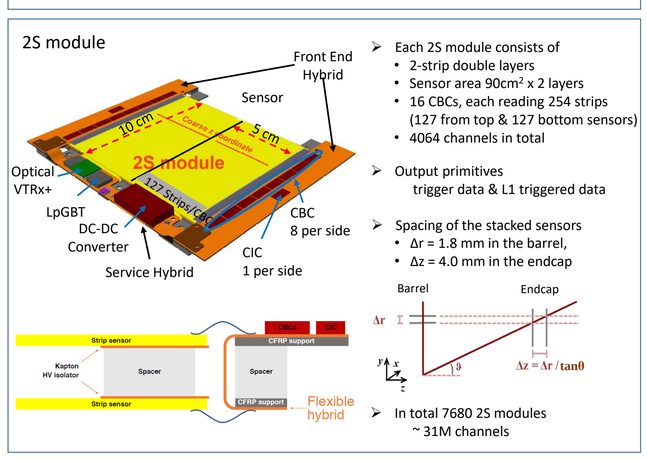
- 130 nm CMOS
- Bump pad pitch : 250 um
- Wire-bond pad for wafer probe
- Binary, unsparsified readout
- I2C interface
- Powering
  - LDO for analogue power & bandgap for biases
- Analogue frontend optimized for AC coupling n-on-p 5cm strip sensors with 254 channels
- 32 deep buffers for triggered events
- Trigger logic
- SEU tolerant Whitaker cells for I2C registers and pipeline logic counters
- Pipeline length : 512 for 12.8 us
- e-Fuse to set chip-id and bandgap
- Chip testing features, internal test pulse with DLL and pulse size adjustment, analogue MUX for bias monitoring



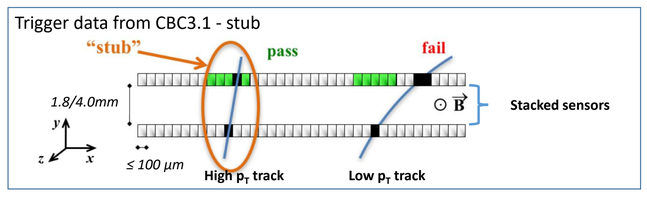


2S-module concept





- Each 2S module consists of
  - 2-strip double layers
  - Sensor area 90cm² x 2 layers
  - 16 CBCs, each reading 254 strips (127 from top & 127 bottom sensors)
  - 4064 channels in total
- Output primitives
  trigger data & L1 triggered data
- Spacing of the stacked sensors
  - Δr = 1.8 mm in the barrel,
  - Δz = 4.0 mm in the endcap
- In total 7680 2S modules
  ~ 31M channels



Wafer testing

The CBC3.1 wafers were produced in three engineering runs, lot 1, 2, and 3. The first set of 13 wafers, lot1, arrived in September 2018 and 2 sets of 24 wafers, lot2 & lot3, in September 2019. There are 478 chips on each wafer and automated testing system was developed with a probe station at Imperial College London.

- **Test program**

  The testing includes checks of I2C register stuck bit, output data, current, VDDA, offset tunings and gains of channels, pipeline, buffer, channel mask, stub logic, Hit detect and HIP suppression logic, delay logic, analogue voltage levels from AMUX , responses to the commands, and any error in the testing process. The e-Fuses are burned during the test and the values are checked.
- **Yields and the patterns of faulty chips in the wafers**

  The average yield of good chips in lot1 wafers is high, 82%, but a clear pattern of faulty chips was found in the centres of the wafers; this was also observed for other chips in the same process and reported to the manufacturer. The lot2 was produced with a modified process in which the metal layers were made thinner. The pattern of the faulty chips is not significant in this lot and the average yield of nearly 90% was achieved. However, a ring pattern of faulty chips at the edges of the wafers appeared in the lot3 which uses the same process as the lot2. The average yield of the lot3 wafers is about the same as the lot1 but the distribution spreads widely.

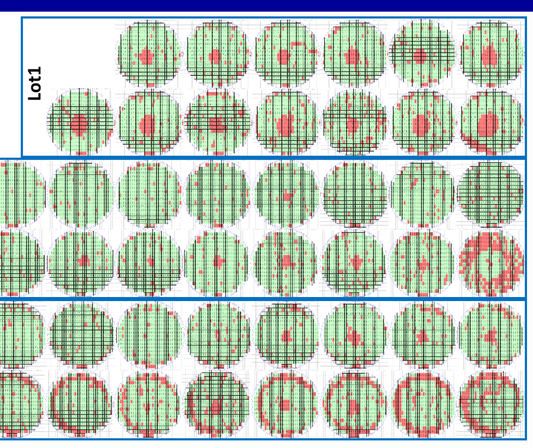
  Characteristics of the failures in the patterns
  - **The central region of the wafers**

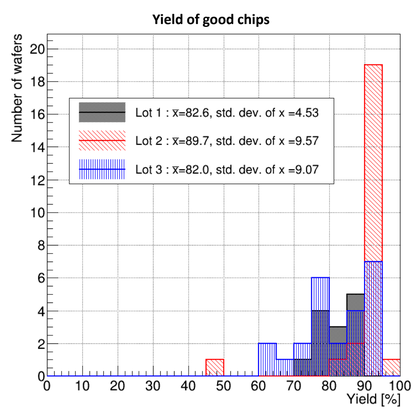
    For the chips in the lot1 wafers, the tests were failing in very early stages at checking either the I2C communication or the serial data coming out of the chips. While the faulty chips at the centres in the lot2 and 3 wafers tend to have gain problems in a couple of channels.
  - **The outer region of the wafers**

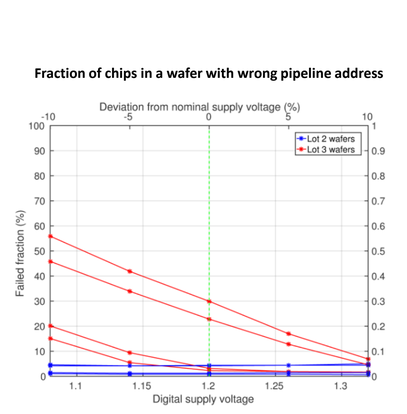
    A large number of faulty chips in a wafer with the lowest yield in the lot2 have high current on digital and low current on analogue part. This was observed only on this wafer. The faulty chips in the rings at the edges in lot3 wafers have a trouble meeting timings. This is observed in the triggered data on the pipeline address values; the Whitaker cells used in the counters in the pipeline logic are relatively slower than other cells and the timing starts failing at the value in the DLL domain is passed to the original clock domain with lower supply voltage or lower temperature; the supply voltage dependence on fraction of the chips with this failure is observed as shown in a plot on the right. It is suspected that the voltage drop is caused by the thinner metal layers in the region. The pipeline address value in the triggered data is used only for debugging and not used in the data taking in the HL-LHC and this is the only observed failure correlated with the supply voltage so far. Also, the powering during the wafer testing is done with the wire-bonding pad, which is at the edge of the chip and not ideal. Therefore, the bump-bonded chip is expected to perform better.
- **Voltage scan and cold test**

  Wafer testing for the supply voltage range and the cold environment expected in the HL-LHC could is planed for the production. The testing takes about 4 hours for a single wafer for one voltage; the testing for multiple voltage is possible given maximum one year allocated for the testing for about 300 wafers. Some wire-bonded CBC3.0 and CBC3.1 chips were tested in a cold chamber from the room temperature down to -40 C° with voltage scans; the correlation between the voltage and temperature for timing issues has been measured. For the wafer testing, a cold chamber for the wafer probing system is planned to be kept low.

Wafers are ordered from the one with high yield to the one with low yield from the top left to the bottom right. The good chips are in green and the bad chips are in red.







SEU test

The SEU tolerance was considered in the designs for counters in the pipeline logic and the I2C registers; the both are made with Whitaker cells since the CBC3.0. The SEU tests of the CBC chips were carried out in the Light Ion Irradiation Facility (LiF) at UC Louvain, where the test beam was provided by a proton cyclotron and the energy was set to the maximum, 62 MeV and the maximum available intensity at the time.

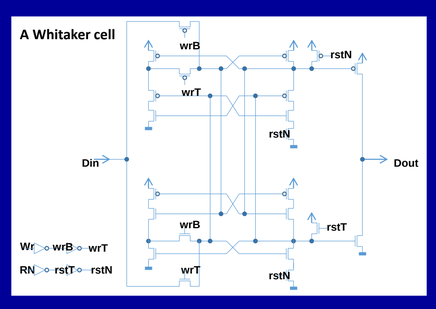
- **Pipeline logic**

  No SEU event was observed in the counters of pipeline logic in both versions of the chip; the upper limit was set to 0.017 SEU/hour (99% CL) per CBC for the HL-LHC condition combining the test results. The corruption of the logic is to be checked in the data frame during the experiment and the upper limit is enough for the recovery operation; the reset signal for the logic takes a couple of bunch crossings.
- **I2C registers**

  The SEU rate on I2C registers for the CBC3.0 was estimated to be 0.03 /hour per CBC for the HL-LHC condition. While this rate is already acceptable, the vulnerability in the control logic, write/reset, of each register cell was identified; with an SEU event on the write node on a register cell, the value in the last 8-bit I2C write data buffered on the I2C bus is written to the cell while an SEU on the reset node writes the default value of the cell.

  In the CBC3.1, the capacitance of the standard inverters used in the logic were increased and the inverters for 8 register cells which form an 8-bit I2C register were connected to make the overall capacitance larger. In the SEU test for CBC3.1, the value in the write data buffer on the bus was set to different values. This revealed that the SEU rate is significantly lower when the value of the write data buffer is set to '00000000' rather than '11111111'. This could be simulated with extremely large deposited charge of 1.2 pC, where only '0' to '1' bit-flip starts happening.

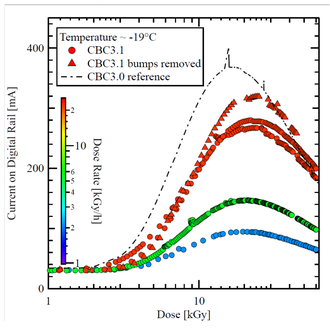
  The SEU sensitive nodes in write/reset and the different bit-flip rates on logic '0' and '1' make the SEU rate depends on the combination of the register setting and the last written value. In the test for the CBC3.1, the registers were configured as close as possible to the setting in the actual experiment. Keeping the last written value to '00000000' would result in the SEU rate per CBC at HL-LHC to be 0.01 /hour. About 20 registers out of 338 are important global settings and should be corrected for the chip to operate correctly. The SEU event rate on these important registers in the entire system is 0.02 registers/sec. One read I2C transaction requires 40 µs with 1 MHz I2C clock and 1 Hz of monitoring for 20 registers/chip with 16 chips per module is reasonable to correct the bit-flips caused by SEU events.



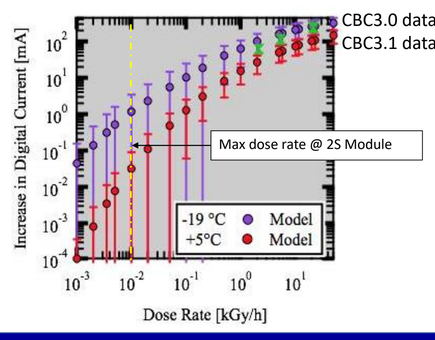
TID test

The TID test was carried out with an X-ray at CERN for the CBC3.0 and the CBC3.1. The digital current increases and peaks in few Mrad region and falls back to pre-irradiation values. The peak current depends on the dose-rate and the temperature. The maximum power consumption was extrapolated to the HL-LHC condition and the effect is negligible with less than 1% increase of the module power consumption. The chip performance was stable during the irradiation up to 60 kGy for the dose-rate 0.1 to 20 kGy/hour.

Digital current vs. Dose



Digital current increase vs. dose rate



Summary and Plan

The CBC3.1 has been tested and verified to satisfy the required performance under the HL-LHC radiation environment. The wafer testing for engineering runs shows high yield of good chips and provided useful information to validate the chip performance reliably for conditions expected in the final system. These studies endorse the readiness of the CBC3.1 for the production expected to start in 2020.

Acknowledgements

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