The design and hardware evaluation of the optical-link system for the ATLAS Liquid Argon Calorimeter Phase-II Upgrade

**Introduction**

- The front-end readout electronics of the ATLAS Liquid Argon Calorimeter is being developed for the HL-LHC upgrade.
- In the proposed upgrade, the detector data are transmitted out of the detector to the counting room about 150 meters away with no trigger filtering.
- In the trigger-less readout scheme, large amounts of data are transmitted through optical links.
- In addition to the data transmission, the front-end electronics needs clocks, control and monitoring from the backend through optical links.
- The optical link system is based on lpGBT and VTRx+.
- The optical link system serves 1524 Front-End Boards (FEBs) through 26 optical fibers per FEB.
- A printed circuit board has been designed to evaluate the major functions of the optical link system.
- The design of the optical link system and the evaluation results are presented.

**Optical link system overall architecture**

- For data links, each FEB has 22 simplex optical links, each operating at 10.24 Gbps. The detector data come from 640 Mbps e-ports of 8-analog-channel ADCCs.
- For control links, each FEB employs 2 duplex optical links. Control links provide recovered clocks for ADCCs, a bunch crossing reset (BCR) signal for each ADC, remote control ASICs, and monitor the temperatures and power supply voltages/currents of each FEB.

**Demo-link system design**

- We designed a PCB to demonstrate the optical link functions.
- The demo board has an lpGBT and a VTRx+.
- The demo board has two FMC connectors to interface with an FPGA.
- The FPGA emulates two ADCs and generates/checks data.
- The demo board includes SMA connectors for clocks and e-links and headers for I2C, ADCs, DAC, and general-purpose I/Os (PIO).
- A second FPGA operates as the back end.

**Data transmission design and verification**

- Recovered data of downlink on the front-end
- Recovered data of uplink in backend
- Recovered data of downlink on the front-end
- Recovered data of uplink at 10.24 Gbps

**BCR distribution design and verification**

- Each downlink provides BCR for 16 ADC chips
- Each lpGBT has 16 e-port outputs

**Clock distribution design and verification**

- A control lpGBT recovers a clock form the serial data and operates on a clock recovered by itself.
- A data lpGBT operates on a clock recovered by a control lpGBT.

**ASIC configuration design and verification**

1. lpGBT, as an I2C slave
   - Can be configured by an external I2C master. Verified.
   - Can be configured by its IC channel. To be verified.
   - Can be configured by its EC channel. To be verified.
2. lpGBT, as an I2C master
   - Can configure (write/read) an I2C slave (our optical module). Verified

**PIO, DAC and ADC design and verification**

- General purpose I/O (PIO) can control a digital I/O signal (e.g., EN of BPOL12V, Reset of ADC lpGBT, etc.). Verified.
- PIO can monitor a digital I/O signal (e.g., Power Good of BPOL12V). Verified.
- DAC can control a voltage. Verified.
- ADC can monitor temperature/voltage/current. Verified

**Summary and outlook**

- An optical link system is being designed for the ATLAS LAr Calorimeter Phase-II upgrade.
- Major functions of the optical link system have been verified in the current link demonstrator board, though extensive tests are still ongoing.
- After all the tests are complete, a new slice (multiple lpGBT chips and VTRx+ modules) of optical link system will be designed.

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**Designers and Contributors**

- Birwei Deng, Chonghan Liu, Datao Gong, Chufeng Chen, Xing Huang, Suen Hou, Tiankuan Liu, Hanhan Sun, Li Zhang, Wei Zhang, Jingbo Ye

**Institutional Affiliations**

- Department of Electronic Information Engineering, Huabei Polytechnic University, Huangshi, P.R. China
- Department of Physics, Southern Methodist University, Dallas, TX 75275, USA
- Department of Physics, Central China Normal University, Wuhan, Hubel 430079, P.R. China
- Institute of Physics, Academia Sinica, Nangang 11529, Taipei, Taiwan

**Contact Information**

- tliu@mail.smu.edu

**Conference Information**

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