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FAST: a 30 ps time resolution front-end ASIC for a 4D tracking system based on Ultra-Fast Silicon Detectors

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The UFSD group of Turin is working at the development of custom front-end electronics for the read-out of thin silicon sensors with moderate internal gain (the so called Ultra-Fast Silicon Detectors- UFSD), aiming at applications that require very precise time tagging. The activity of the group is mainly focused on meeting the requirements of the next generation of HEP colliders where the main role is played by the LHC High-Luminosity upgrade, with the expected challenging pile-up factor of 150-200 events per bunch crossing. In this context, time tagging is one of the fundamental tools which can be exploited to distinguish events overlapping in space but separated in time by a few tens of pico-seconds: both ATLAS, with the High Granularity Timing Detector and CMS, with the MIP Timing Detectors, are pursuing time tagging projects with a 30 ps time resolution.

The measurement of the Time of Arrival of a particle is affected by uncertainties coming both from the sensor used to detect particles and from the readout electronics used to measure the weak signals generated by the sensor. In order to increase the time resolution, signals with high amplitudes and small rising time are key points. In this context, UFSD sensors are proposed as a good candidate for time measurements, due to their capability to generate signals with the properties listed above. For what concerns the contribution of the readout electronics, the slew rate and the front-end noise are mainly influencing the timing performances.

In this paper we present **FAST**, a 20 channels novel low power front-end electronics for UFSD, devoted to timing resolution with a **jitter lower than the 30 ps** target. In order to map different solutions, we designed three flavors of FAST differing in the amplification stages and component-level technical choices. During the design phase, extensive simulation considered the intrinsic sensor signal shaping, including radiation damage effects.

The ASIC tape-out is foreseen for September 2019 and on-silicon characterization results will be shown at the conference.

Submission declaration

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