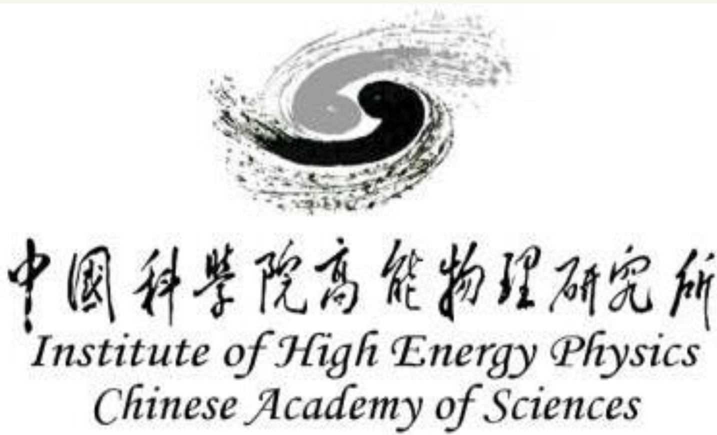
The TSV Processing in the Hybrid Pixel Detector for the High Energy Photon Source



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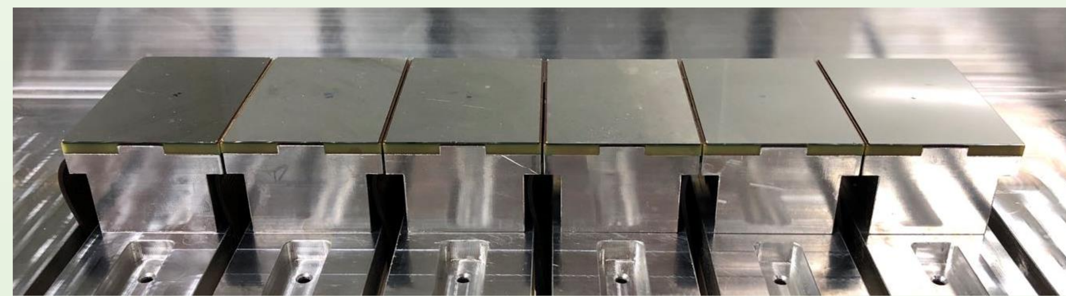
1. MOTIVATION



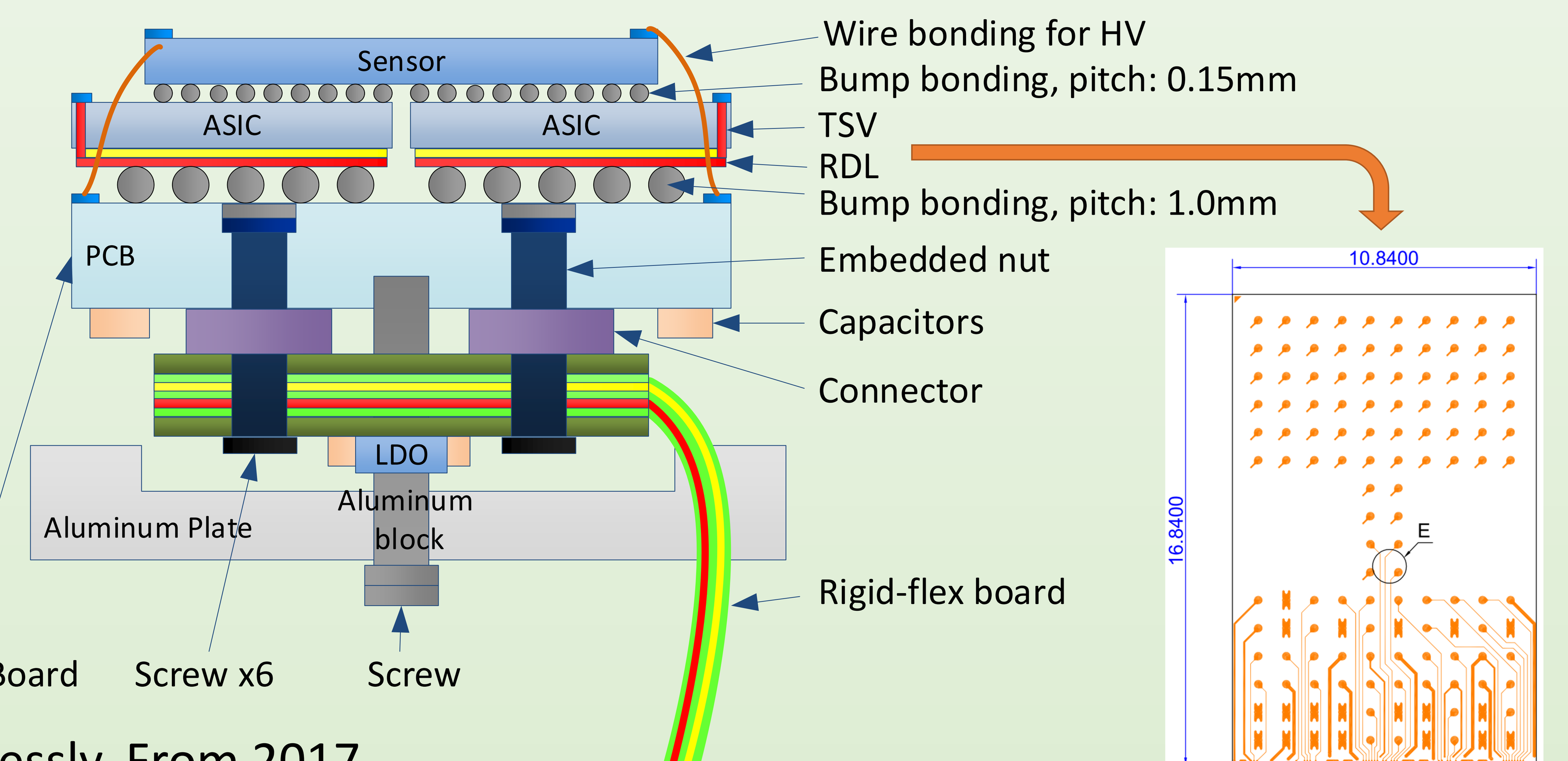
Photograph of the prototype containing six individual TSV modules mounted on the aluminum carriers.

High Energy Photon Source-Test Facility (HEPS-TF) is a project to study and verify the feasibility of the key technologies which will be applied to the building and running of HEPS during the 13th Five-Year Plan in China. The hybrid pixel detector is one of the most important components of synchrotron light sources.

HEPS-BPIX3 is the third prototype of single-photon counting pixel detector with 1.4 million pixels developed for HEPS. It follows the first prototype, HEPS-BPIX, with a pixel size of 150 μm x 150 μm and frame rate up to 1.2 kHz at 20-bit dynamic range.

With the increasing sensitive area, the modules should be tileable to cover large area seamlessly. From 2017, we started to use the Through Silicon Vias(TSV) processing to replace the wire-bonding processing.

The block diagram of the front-end module.



The redistribution layer

2. IMPLEMENTATION

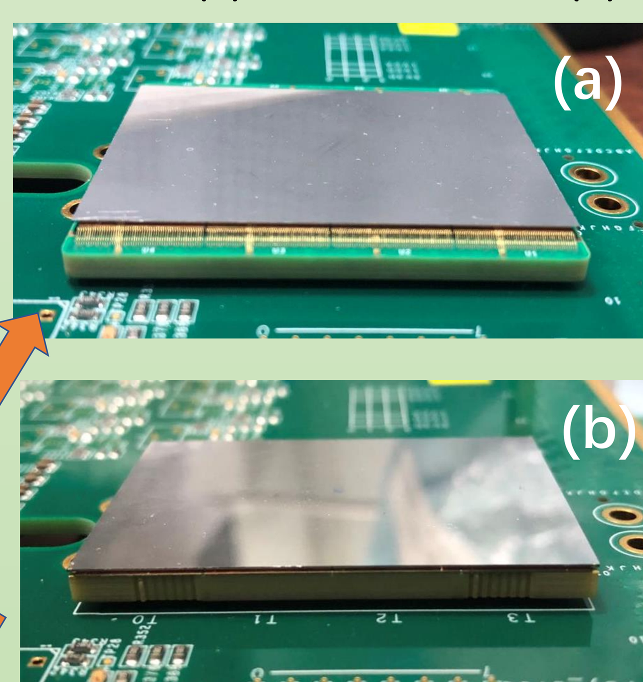
On the top, the sensor consisting of p+ pixelized implants on a 300 μm n-silicon substrate is bump-bonded with 8 readout chips. The X-ray or synchrotron radiation light crossing the sensor component creates electron–hole pairs. The electrons and holes are separated by an applied reverse bias voltage, allowing the charge carriers to be collected by the appropriate pixels of the read-out chip. The readout chip is divided into the analog part and digital part. The charge is first amplified with a low noise amplifier, shaped through a shaper and then discriminated with an adjustable threshold. Then the output from each pixel performs the counting. When receiving frame signal, the counts is locked and read out by the shift register.

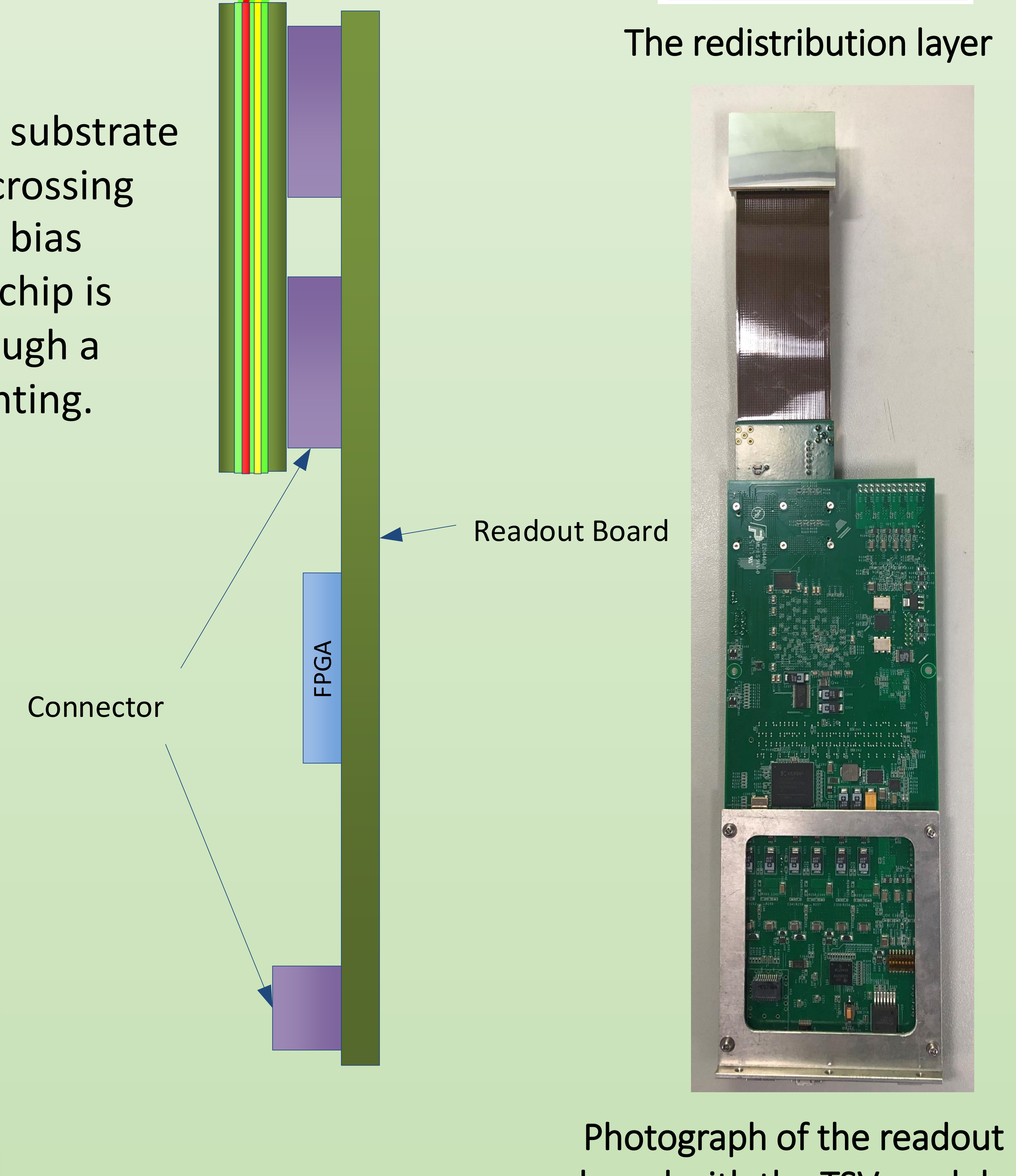
To replace the wire bonding, the TSV processing drills the via at the pad, and makes connection between the front and back sides of the read-out chip. The Redistribution Layer (RDL) and bump bonding are performed at the bottom of read-out chip. The control, readout signals and power supplies are provided through flexible PCBs to the readout board. By this way, the insensitive area is reduced from 26.3% to 12.5%.

Table 1. Dimension comparison between the wire-bonding module and TSV module

	L/mm	W/mm	insensitive gap between modules					
			Percentage	L		W		
				mm	pixels	mm	pixels	
Effective area	43.8	31.4	-	-	-	-	-	
Wire bonding	45.75	40.8	26.3%	1.95	13.0	9.40	62. 7	
TSV+RDL	45.8	34.3	12.5%	2.00	13.3	2.90	19.3	

Photograph of the wire-bonding module(a) and TSV module(b)





Photograph of the readout board with the TSV module

3. PRELIMINARY RESULT

Two TSV modules and two wire-bonding modules were tested with X-ray and synchrotron radiation.

1. Electronics Calibration

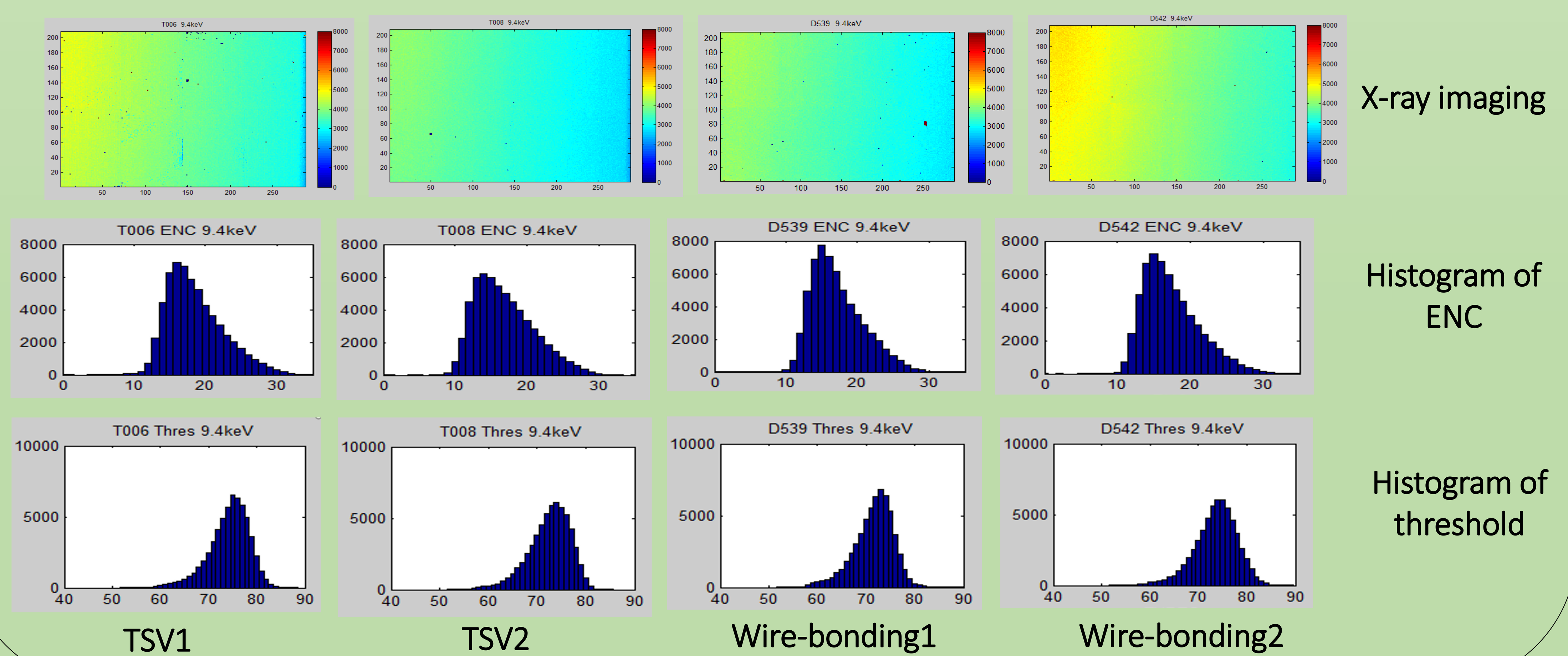
Table2 shows that the noise of the TSV modules and the wire-bonding modules are similar after electronic calibration.

Table 2. The noise and threshold level of the TSV and wire bonding modules

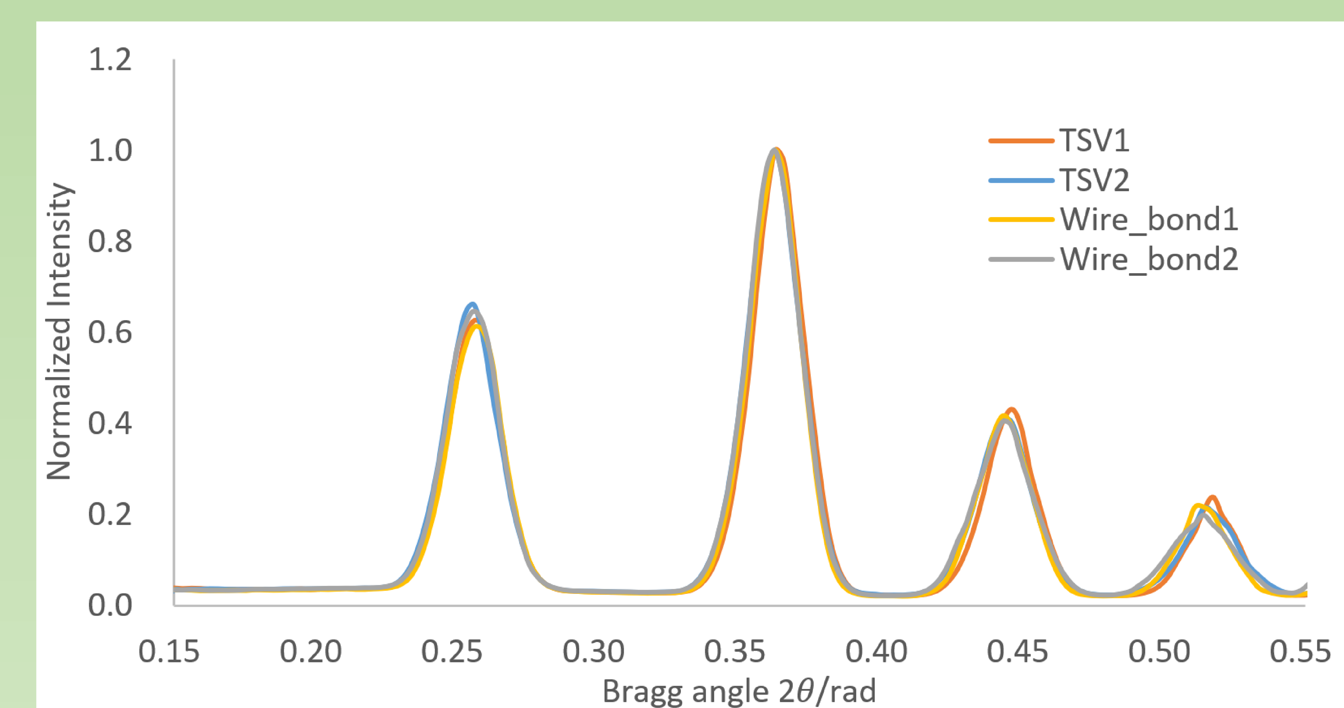
module	ENC	ENC_std	thres	thres_std
TSV1	17 mV	1 mV	245 mV	5 mV
TSV2	16 mV	2 mV	232 mV	6 mV
Wire-bonding1	18 mV	2 mV	272 mV	4 mV
Wire-bonding2	18 mV	1 mV	266 mV	6 mV

2. X-ray responding

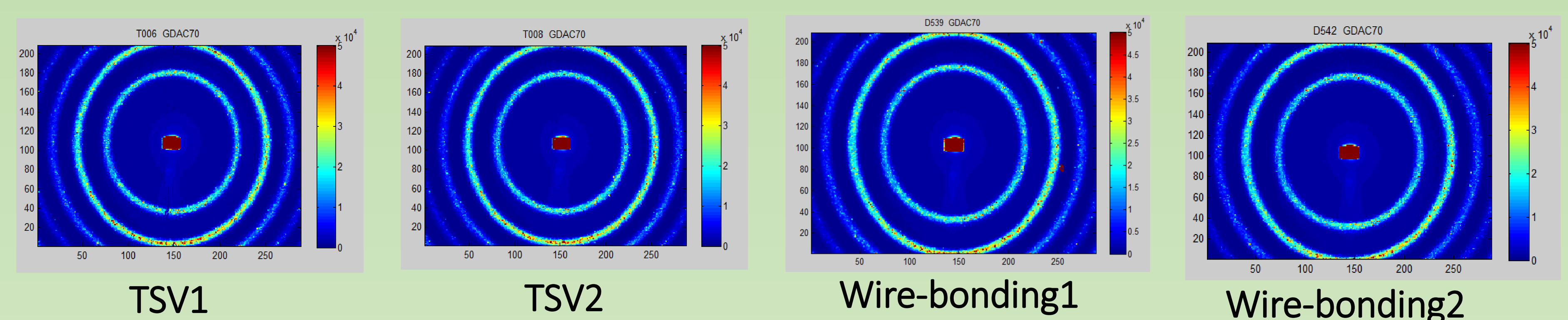
under an Au X-ray tube powered at 9.4 kV



3. Power diffraction imaging



The diffraction rings of the powder sample LaB_6 exposed under the 1W2B beamline of BSRF for 10s at 12keV.



The extracted spectrum shows the read-out chip can be operated electrically through the TSV processing without any performance degradation.