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A 12-Channel 120 Gbps Optical Transmitter in 55 nm CMOS for High-Energy Physics Experiments

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VCSEL-based array optical data transmission system has been prevailingly researched and developed for the front-end data acquisition in high-energy physics experiments with advantages in density, data throughput, power consumption and radiation performance. This paper presents the design and test results of a 12-channel 12 x 10 Gbps VCSEL driving ASIC fabricated in 55nm CMOS technology. Each channel in the driver consists of an input equalizer stage, a pre-driver (limiting amplifier) stage and an output driver stage. The equalizer stage adopts a 4-step adjustable CTLE structure to compensate the high frequency losses from the system level including PCB traces and bonding wires. The pre-driver stage uses the passive shared inductor technique to obtain sufficient bandwidth (16.5 dB, 8.3 GHz) in a limited area (212 μm x 235μm). The output driver stage employs both the programmable R-C degradation pre-emphasis structure and the feed-forward capacitor to improve the bandwidth. All 12 channels can be controlled independently by the I2C module, which is strengthened with the Triple Modular Redundancy (TMR) structure.

The driving ASIC features a size of 1450 μm x 4000 μm with 74 pads. The chip has been wire bonded on the test board, and a full 12-channel electrical test has been conducted. Widely-open 10-Gbps eyes have been captured for all 12 channels at the typical settings of 2 mA bias current and 5 mA modulation current. The deterministic jitter (DJ) of the captured 10-Gbps eye is 12.9 ps, the random jitter (RJ) is 870 fs (rms), and the total jitter is 25.1 ps at a bit error rate of 1E-12. The tested power consumption of the chip is 32.5 mW/ch when working at 10 Gbps/ch. The full channel test results will be reported in the meeting.

Submission declaration

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