Monolithic CMOS sensors for sub-nanosecond timing

Thanushan Kugathasan[1], Takeharu Goji Etoh[2], Dominik Dannheim[1], Magdalena Munker[1], Heinz Pernegger[1], Angelo Rivetti[3], Kazuhiro Shimonomura[2] and Walter Snoeys[1]

[1]CERN, Geneva, Switzerland [2]Ritsumeikan University, Kyoto, Japan [3]INFN, Torino, Italy

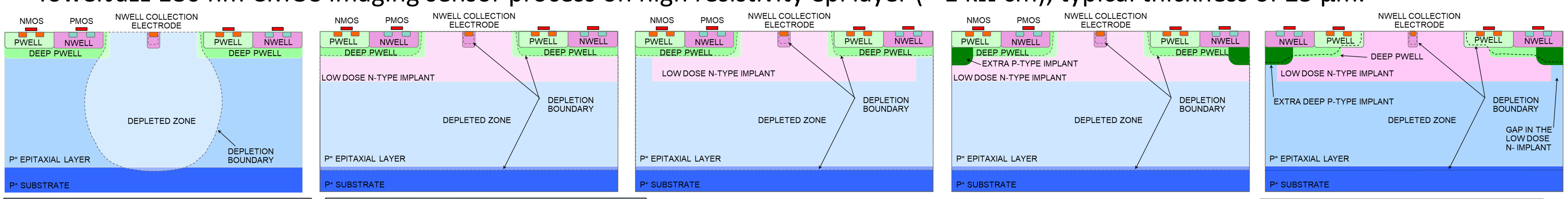
This project has received funding from the ATTRACT project funded by the EC under Grant Agreement 777222

Abstract

In the ATTRACT project FASTPIX we investigate monolithic pixel sensors with small collection electrodes in CMOS technologies for fast signal collection and precise timing in the sub-nanosecond range.
Deep submicron CMOS technologies allow tiny, sub-femtofarad collection electrodes, and large signal-to-noise ratios, essential for very precise timing. However, complex in-pixel circuits require some area, and one of the key limitations for precise timing is the longer drift time of signal charge generated near the pixel borders. Laying out the collection electrodes on a hexagonal grid and reducing the pixel pitch minimize the maximum distance from the pixel border to the collection electrode. The electric field optimized with TCAD simulations pulls the signal charge away from the pixel border towards the collection electrode as fast as possible. This also reduces charge sharing and maximizes the seed pixel signal hence reducing time-walk effects. Here the hexagonal geometry also contributes by limiting charge sharing at the pixel corners to only three pixels instead of four. We reach pixel pitches down to about 8.7 µm between collection electrodes in this 180 nm technology by placing only a minimum amount of circuitry with the pixel and the rest at the matrix periphery. Consuming several tens of micro-ampere per pixel from a 1.8 V supply offers a time jitter of only a few tens of picoseconds. This allows detailed characterization of the sensor timing performance in a prototype chip with several mini-matrices of 64 pixels each with amplifier, comparator and digital readout and some additional pixels with analog buffers. The aim is to prove sensor concepts before moving to a much finer line width technology and fully integrate the readout within the pixel at lower power consumption.

CMOS sensor with small collection electrode - Process Cross Section

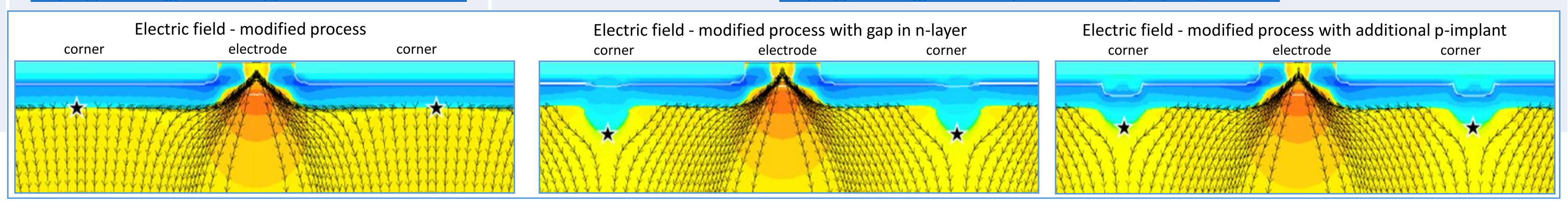
TowerJazz 180 nm CMOS imaging sensor process on high resistivity epi layer (> 1 kΩ cm), typical thickness of 25 µm.



Standard process — CMOS circuit in deep-p-well with small n-well collection electrode. Low sensor capacitance (≈2 fF) for power optimization and large Signal to Noise ratio. Charge collection time limited by diffusion (≈100 ns).
Ref. ALPIDE pixel sensor https://doi.org/10.1016/j.nima.2015.09.057

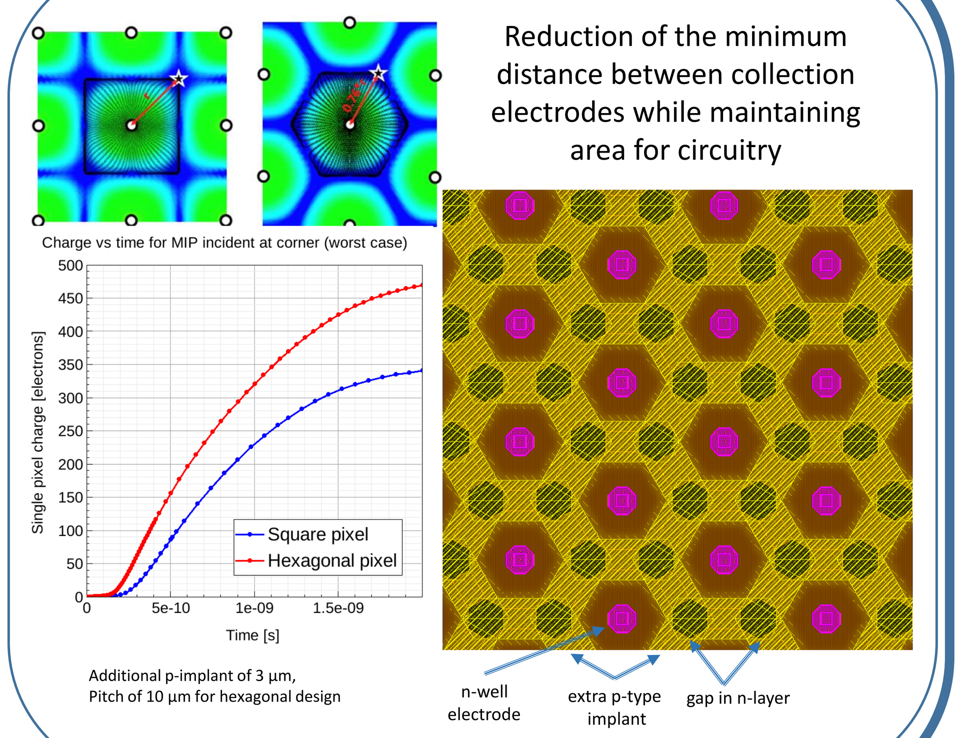
Modified process — Low dose n-type implant to achieve full lateral depletion and full charge collection by drift (≈10 ns).
Ref. W. Snoeys et. al https://doi.org/10.1016/j.nima.2017.07.046

Modification with increase lateral electric field — Additional p-type implant or gap in n-layer at the pixel edges to increase lateral electric field in the corner regions. This allows faster charge collection by drift and reduced charge sharing.
Ref. M. Munker et. al https://doi.org/10.1088/1748-0221/14/05/c05013



FASTPIX — Combination of extra p-type implant and gap in n-layer at the pixel corners to further bend the electric filed lines towards the collection electrode. Increase of the charge collection speed for time resolution < 1 ns.

Top view - hexagonal grid

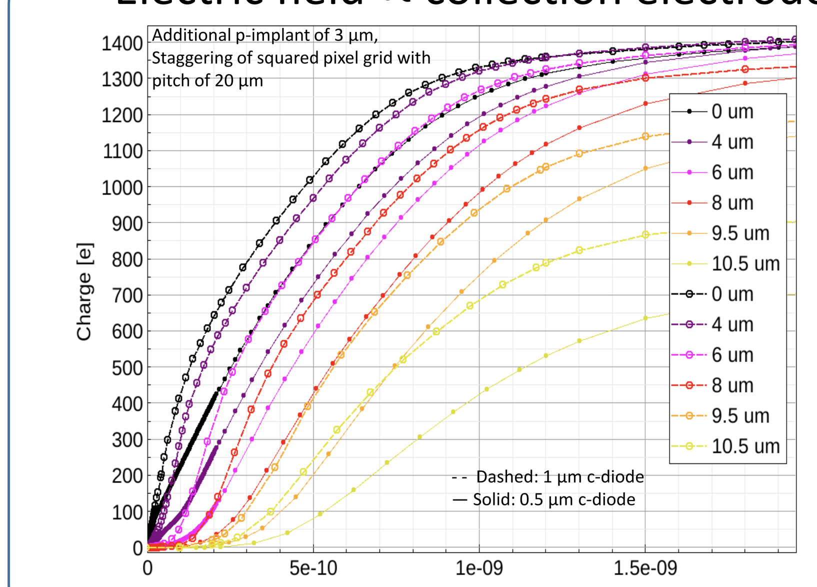


Collection electrode optimization – TCAD simulations

Ref. talk "Vertex and Tracking Detector R&D for CLIC", M.Munker, 15/12/2019 @ 12.00

Collection electrode size

- Capacitance ∝ collection electrode size
- Electric field ∝ collection electrode size

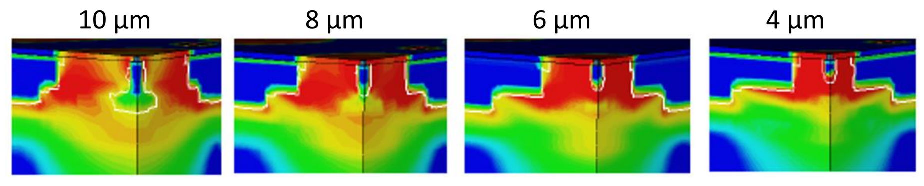


→ **Trade-off:**
- Small collection electrode → Small capacitance but lower field
- Large collection electrode → Large capacitance but higher field + better contact to low dose n-layer

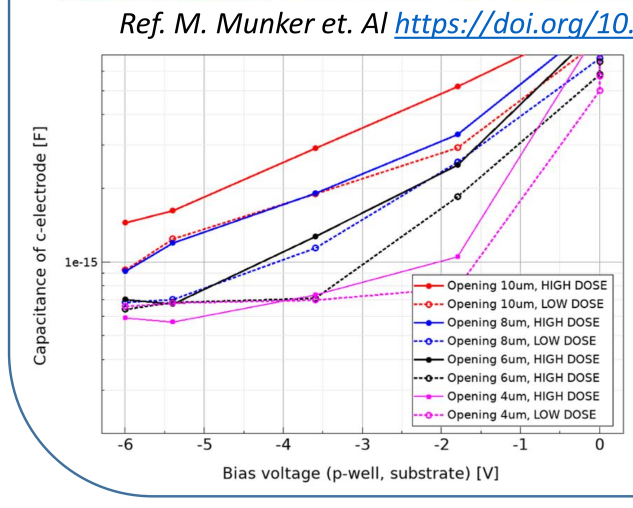
Electrode – p-well distance (opening)

- Capacitance ∝ opening
- Electric field ∝ opening

Electric field and depletion around the collection electrode for different openings



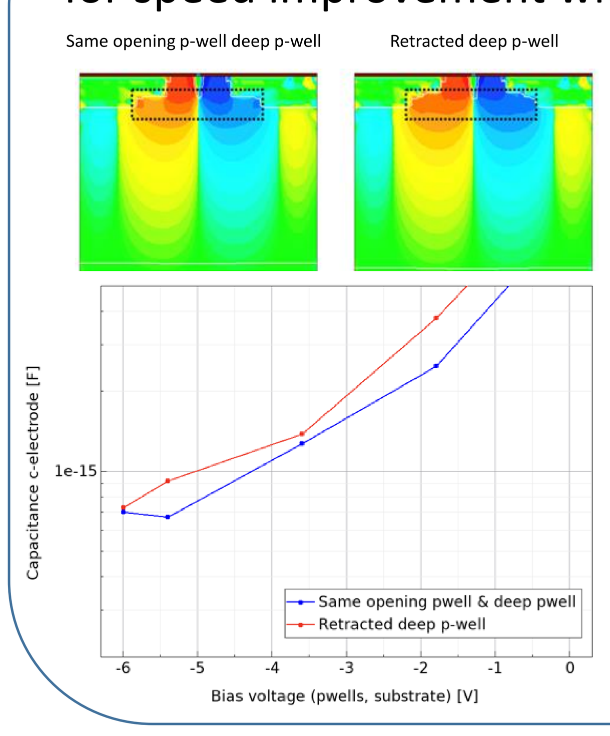
Ref. M. Munker et. Al https://doi.org/10.22323/1.348.0033

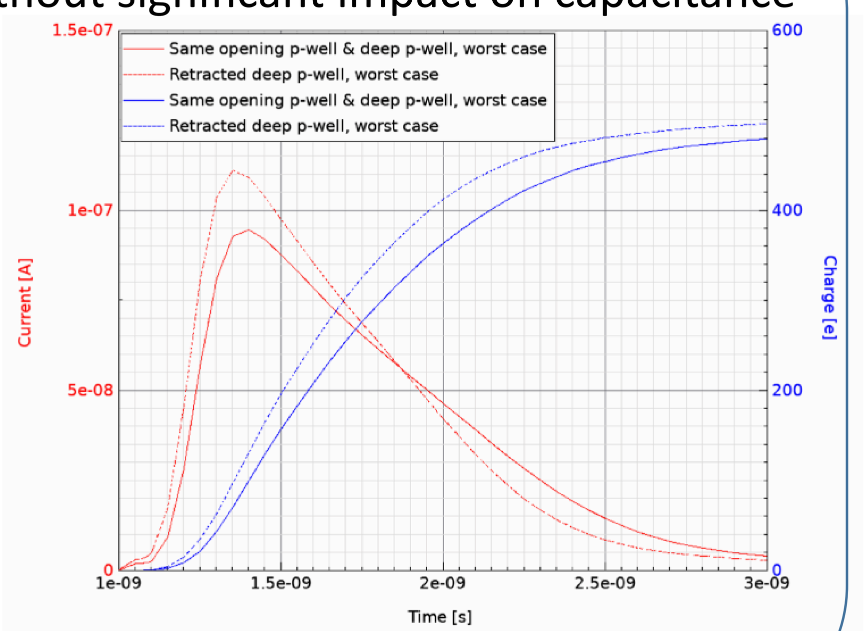


Capacitance optimized with a bias of -6 V and a p-wells opening not larger than 6 µm

Deep p-well placement

Deep p-well can be retracted as far shielding of circuitry allows for speed improvement without significant impact on capacitance

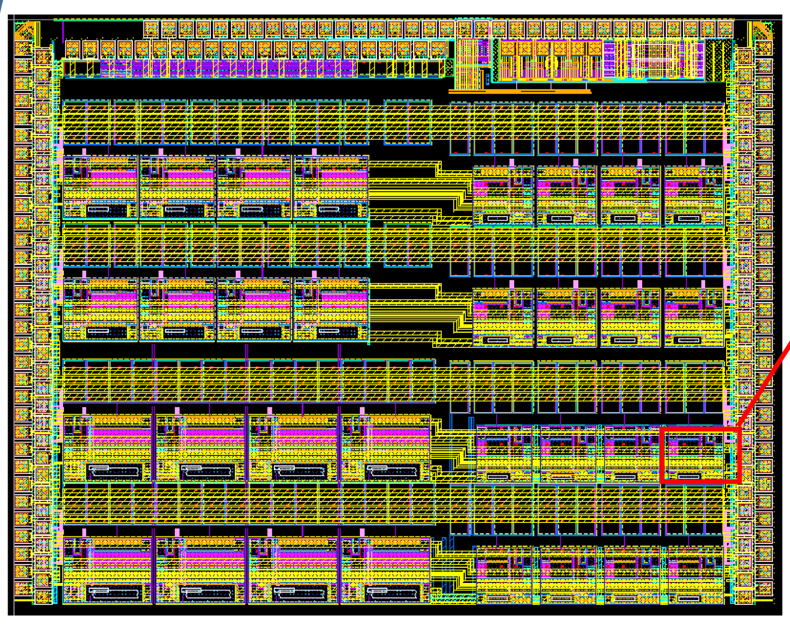




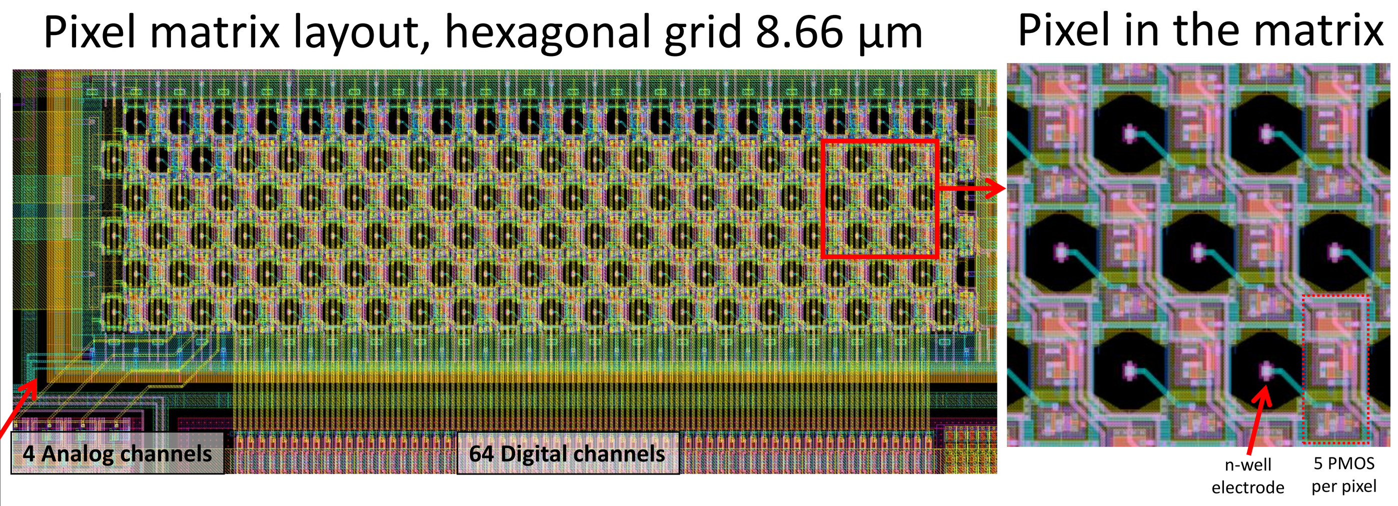
Additional p-implant of 3 µm, pitch of 15 µm for hexagonal design (no retraction of deep p-well possible for small pitch of 10 µm)

FASTPIX Test Chip – Design and simulations

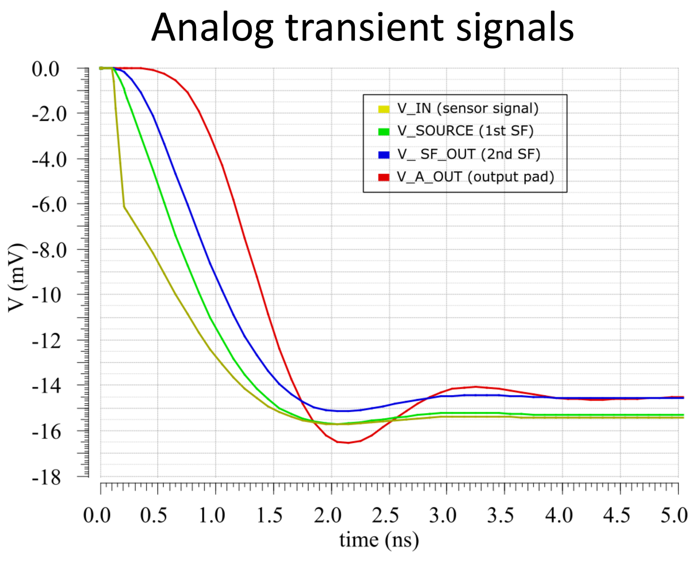
FASTPIX layout (5.3 x 4.1 mm²)



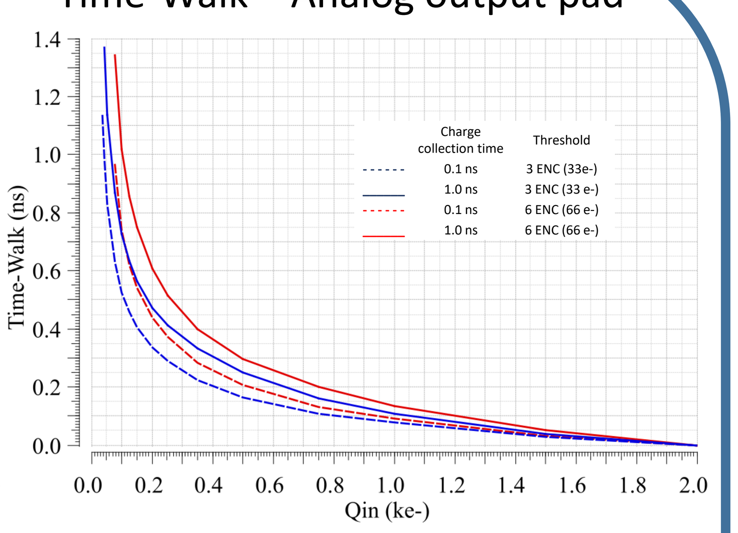
Pixel matrix layout, hexagonal grid 8.66 µm — Pixel in the matrix



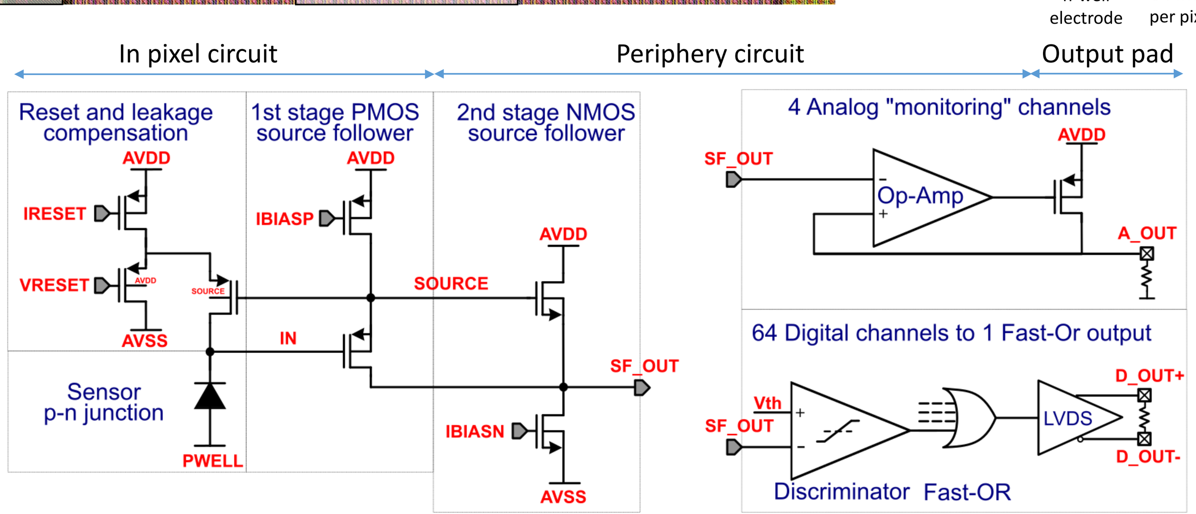
Analog transient signals



Time-Walk – Analog output pad



- 1 LVDS Rx for test injection pulse input
- 3 LVDS Tx for digital pulse output
- 4 x 4 Analog "monitoring" output
- Bias regulation for 9 currents and 6 voltages
- 4 x 8 Matrices, hexagonal grid, pitch of:
  - 8.66 µm, 10.0 µm, 15.0 µm, 20.0 µm



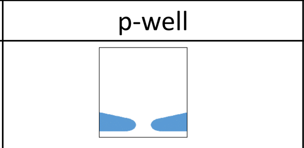
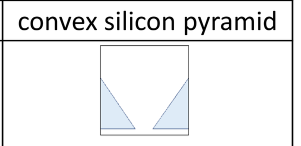
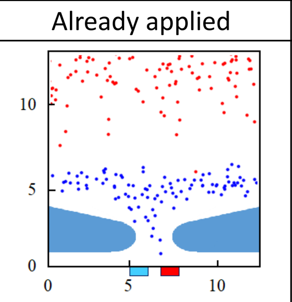
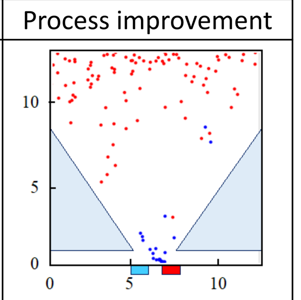
Sensor capacitance		1 fF
Equivalent Noise Charge		11 e⁻
Jitter (for Q_{in} = 1000 e⁻)		20 ps
Power	In pixel source follower	18 µW
	Periphery discriminator	150 µW
	Analog monitoring buffer	20 mW

3D Electric field shaping for sub-nanosecond timing

Timing resolution in the sub-nanosecond range can be achieved with special sensor structures that shape the electric field creating a funnel to accelerate the signal charge to the collection electrode.

Monte Carlo simulations for visible light

Performance overview of structures for back side illuminated image sensors with 100% fill factor that could be used for ionizing particles.

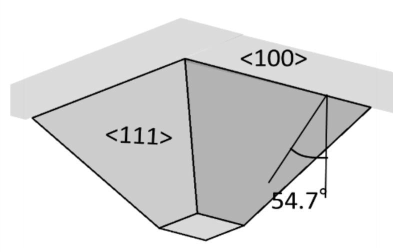
Structure	p-well	convex silicon pyramid
Cross section (electrode at the bottom)		
Pixel shape	square pixel of 12.73 µm pitch and 13.1 µm thick	
Temporal resolution 2σ	990.0 ps	87.5 ps
Vertical field	5 kV/cm	25 kV/cm
Technical feasibility	Already applied	Process improvement
Visible light incident at the top. • photo-electrons creation point • photo-electrons after 200 ps [scales in µm] Possibility to have multiple electrodes at the bottom		

Convex silicon pyramid micro-machined in silicon

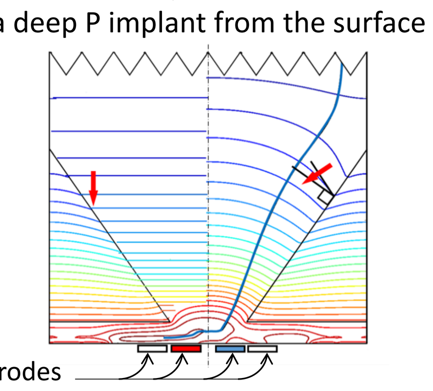
The pyramid charge collector further reduces the temporal resolution to 1/10 of that of the p-well charge collector/potential separator.

1. Efficient suppression of the horizontal motion causing mixing of signal electrons
2. A larger vertical field than that of the p-well causing punch-through for a high field

Shape: 1 pixel
Truncated pyramid with square section.

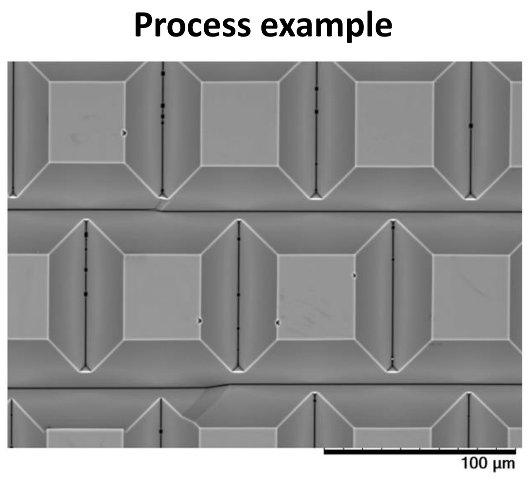


Potential simulation
The right side shows the equipotential lines when adding 100 nm B implant on the wall + a deep P implant from the surface



Multiple electrodes

Process example



Summary

Fastpix is a monolithic pixel chip with small collection electrode (C_d < 1 fF) for sub-nanosecond timing applications.
Fastpix is implemented in TowerJazz 180 nm CMOS modified process with a sensor structure that increases the lateral electric field. It features 32 matrices with hexagonal grid and pixel pitches from 8.66 µm to 20 µm.
Monte Carlo simulations show that a sensor with a convex pyramidal structure could reduce the charge collection time below 100 ps.

Contact: thanu@cern.ch