Highly compact digital pixel structures developed for the CEPC vertex detector*

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ABSTRACT

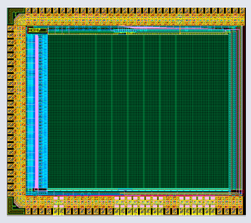
A prototype named JadePix-2 comprising a matrix with 112×96 pixels has been designed and fabricated in a 0.18 μm CMOS Image Sensor process. It contains two digital pixel structures, both have been realized within 22 μm pitch size. The prototype operates in the rolling-shutter mode, with processing speeds of 100ns/row and 80ns/row, respectively, for the two pixel structures. Experimental results show the total ENC and power dissipation of the two structures are about 29 e^- with 6.5 μA/pixel, and 31 e^- with 3.7 μA/pixel respectively.

INTRODUCTION

The proposed CEPC (Circular Electron Positron Collider) will offer the measurements of the Higgs properties with a new level of precision. The precise determination of the charged particle tracks and reconstruction of the primary and displaced decay vertices, impose stringent requirements on the CEPC vertex detector, which somehow incompatible with each other, such as high spatial resolution (<3μm), low power consumption (<50mW/cm^2) and fast processing speed (<10μs/frame). CMOS pixel sensor with pixel level discrimination represents one of the most promising candidates. However, the complexity of in-pixel digital circuit always leads to increased pixel size, which is disfavored to obtain high spatial resolution.

In this context, we propose two pixel structures with balance between high precision and circuit simplicity to guarantee compact pixels, yet with satisfying high signal over noise ratio. Both of the two structures are based on the DMAPS (Depleted Monolithic Active Pixel Sensors) concept, employ a high-voltage (up to 10 V) biased charge collection diode, AC-coupled to a comparator with OOS (Output Offset Storage) technique to mitigate pixel-to-pixel performance dispersion. The main difference between the two structures concentrates on the signal amplification stage used in the comparator.

Specifications of JadePix-2



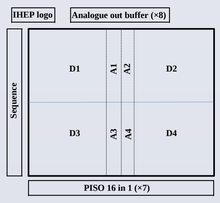


Figure 1: Layout (left) and architecture (right) of JadePix-2.

- Some prototype specifications:
  - 0.18 μm CMOS Imaging Sensor (CIS) technology;
  - Quadruple well, 6 metal layers process;
  - ~ 20 μm high resistivity (≥1 kΩ•cm) epitaxial layer
  - 112×96 square pixels with 22 μm pitch size;
  - 3×3.3 mm^2 layout size;
  - 8 test sub-matrices for two pixel versions, D1-D4 with digital output, A1-A4 with analogue output;
  - 8 Analogue output channels;
  - 16 Column digital data serialized in one LVDS output pair; 7 LVDS pairs in total.
  - Output data speed: 160 MHz
  - Pixel version 1: ~3.7 μA/pixel (power), ~31 e^- (noise), 100ns/row (operation speed);
  - Pixel version 2: ~6.5 μA/pixel (power), ~29.5 e^- (noise), 80ns/row (operation speed)

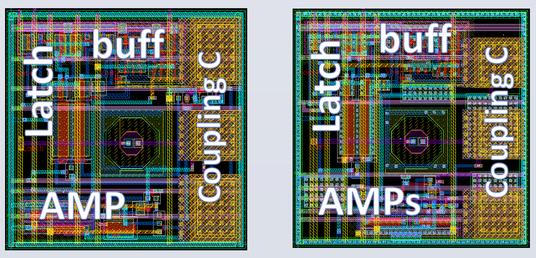


Figure 2: Layout of the two pixel versions, both pitch sizes are 22μm.

In-pixel architecture and signal treatment

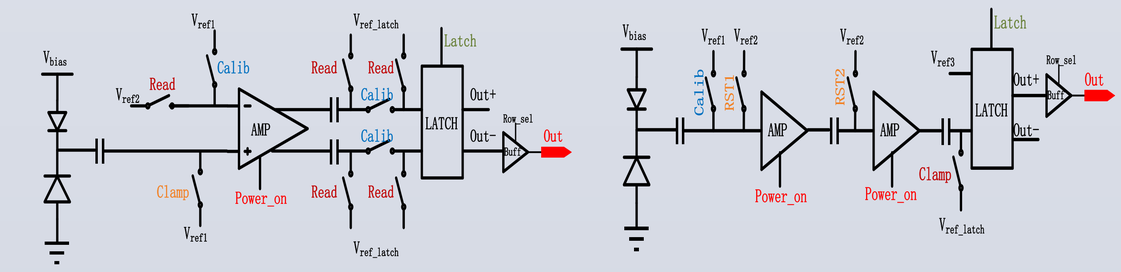


Figure 3: Two pixel structures with a differential amplifier + Latch (version 1, left), and two stage Common-Source amplifier +Latch (version 2, right).

- In-pixel Architecture:
  - High-voltage biased N-well/p-epi collection node (V_{bias} up to 10V) AC coupled to the following electronics.
  - Comparators designed with the Output Offset Storage (OOS) technique;
  - Thresholds adjusted externally at the differential amplifier (Version 1) and at the dynamic Latch (Version 2) ;

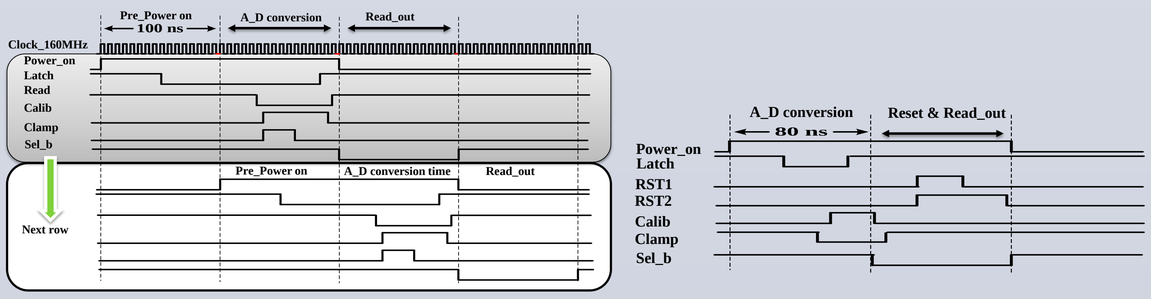


Figure 4: operation timing of the pixel version 1 (left) and version 2 (right).

- Signal and Noise treatment:
  - The useful signal (amount of e^- collected by the diode) is translated into a ΔV on the diode; AC coupled structure transmit this ΔV to the following comparators where signal is amplified and digitalized; digital signal is then stored in the Latch and output to column through a digital buffer row by row;
  - The offsets of the amplifiers are compensated by the combined offset cancellation technique;

Equivalent Cap. of the sensing node

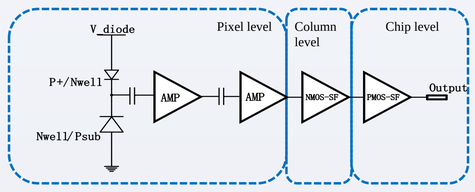


Figure 5: schematic of the signal transmission used for the ^{55}Fe source test (while it was not an good option for this test)

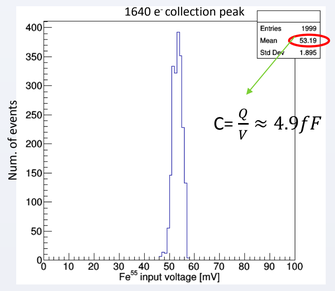


Figure 6: Charge collection response peak of ^{55}Fe source: the X-axis value shows the ΔV on the sensing node while the whole 1640 e- were collected by one pixel.

Set-up conditions:

- 4 stage Amp.: limit only ~ 10 mV linear response range on the sensing node; leave other situation either no gain or saturated.
- the Amp. was tuned to let the input signal ~ 1600e^- in the linear response range, while no response for smaller signals and saturate for larger ones.
- Events only with S/N > 10 was recorded.

Performances of the in-pixel Amp. and dynamic Latch

Differential amplifier in pixel version 1:

- Input DC level: 600 mV
- Gain: ~ *6.9*
- *RMS of* Gain distribution: ~ 0.4

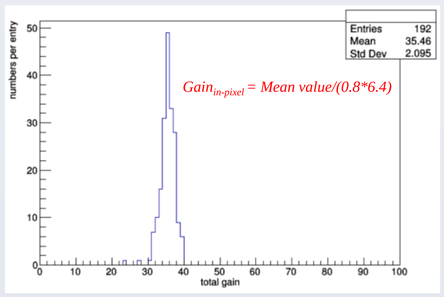


Figure 7: Gain distribution of the in-pixel differential amplifiers; the value includes 6.4 amplitude on the PCB and 0.8 of two-stage source followers on the sensor.

Single-end CS Amplifier in pixel version 2:

- Input DC level: 520 mV
- Gain: ~ *52*
- *RMS of* Gain distribution: ~ 15

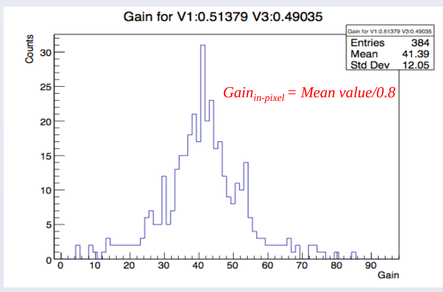
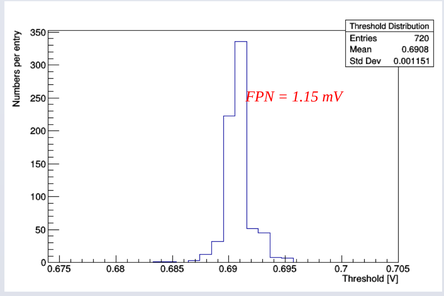


Figure 8: Gain distribution of the in-pixel two stages single-end CS amplifiers; the value includes 0.8 of two-stage source followers on the sensor.



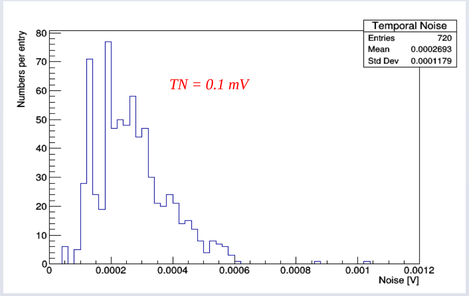
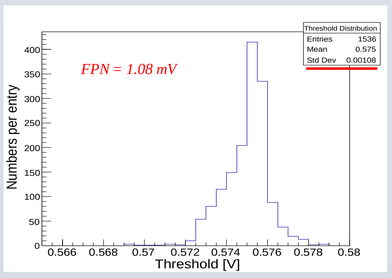


Figure 9: Fix Pattern Noise (left) and Temporal Noise (right) of the in-pixel dynamic Latch. (test results)

Table 1: ENC of the in-pixel latch.

Pixel version	TN	FPN
Version 1	negligible	≈ 4 e^-
Version 2	negligible	negligible

Performances of the pixel matrix



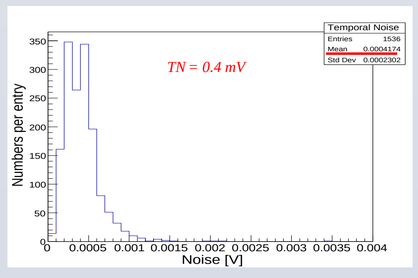
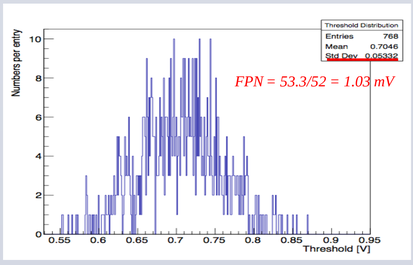


Figure 10: Noise (equivalent at the sensing node) of pixel matrix version 1: FPN (left) and TN (right)



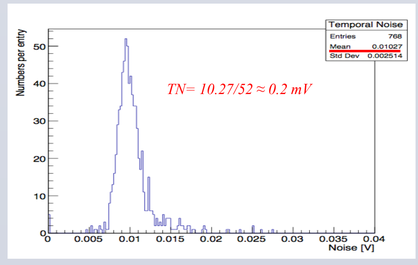


Figure 11: Noise (equivalent at the sensing node) of pixel matrix version 2: FPN (left) and TN (right).

Table 2: ENC of the pixel matrix.

Matrix version	TN	FPN	Total Noise
Version 1	11 e^-	29 e^-	~31 e^-
Version 2	5.5 e^-	29 e^-	~29.5 e^-

CONCLUSION AND PERSPECTIVES

We proposed two pixel structures with balance between high precision and circuit simplicity to guarantee compact pixels (22 μm pitch size). Both versions operate in the rolling-shutter mode and take 100ns and 80ns, respectively, to process one row. Experimental results show the total ENC and power dissipation of the two structures are about 29 e^- with 6.5 μA/pixel, and 31 e^- with 3.7 μA/pixel respectively. The knowledge learned from JadePix-2 will guide the design of the next generation vertex detector for CEPC and achieve the desired high spatial resolution.

*** This study was supported by the National Key Program for S&T Research and Development (2016YFA0400400) and the National Natural Science Foundation of China (11605217)**