

A 12-Channel 120-Gb/s Optical Receiver Array in a 55 nm CMOS technology for High-Energy Physics Experiments

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Optical data transmission, characterized by high data rate capacity, low power consumption and space saving, has been extensively used in the detector readout electronics in high-energy physics (HEP) experiments. The photodiode (PD)-based optical receiver array is a key component to build paralleled optical links at the receiving end. The light traveling through a fiber experiences optical power loss before reaching a photodiode. Each channel of an optical receiver array consists of a transimpedance amplifier (TIA) and a few limiting amplifier (LA) stages and aims at converting the small optical current in the photodiode to a voltage and further amplifying it.

This paper presents the design and measurements of a 12-channel 120-Gb/s optical receiver array ASIC fabricated in a standard 55-nm CMOS technology. A pseudo-differential CMOS push-pull TIA with resistive feedback is utilized to provide common-mode noise rejection and improve jitter performance. A novel three-order active feedback strategy is employed in five LA stages to expand the bandwidth and optimize the gain performance. The shared-inductor peaking and RC degeneration techniques are used to further improve the bandwidth. The single channel of the optical receiver array exhibits a total gain of 89.4 dB Ω with a bandwidth of 7.5 GHz.

The whole chip occupies 1.4 mm \times 4 mm and consumes 672 mW with all 12 channels enabled. Wide-open eyes diagrams are recorded and a bit error rate (BER) of less than 1E-12 is achieved at 10 Gbps/ch. Random jitter (RJ) is 1.16 ps (RMS), deterministic jitter (DJ) is 10.1 ps (peak-to-peak) and total jitter is 26.8 ps. All channels demonstrate similar performance. The measurements indicate that we achieve our design goal.

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