JICG CMOS Transistors for Reduction of Total Ionizing Dose and Single Event Effects in a 130nm Bulk SiGe BiCMOS Technology

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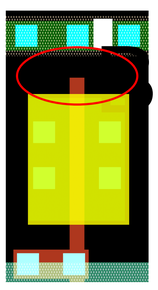
MOTIVATION & GOALS

Integration of radiation tolerant core and IO MOS transistors fabricated in a 130nm bulk SiGe BiCMOS technology for aerospace applications and high energy physics experiments

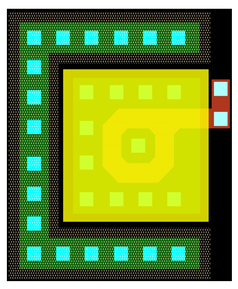
- Mitigation of TID (total ionization dose) and SEE (single event effects) induced malfunctions in digital circuits using a novel radiation hardening by design approach (RHBD)
- Reduction of TID induced drain leakage for NMOS transistors and channel pinch-off for PMOS transistors due to trapped fixed positive charges in the surface interface region of the shallow trench isolator (STI) by introduction of a lateral junction isolation (JI) of the MOS transistors.
- Negligible TID induced MOS DC parameter degradations for doses > 1 Mrad (^{60}Co source)
- SEE onset LET_{SEEth} > 100 MeV cm^2/mg by introduction of redundancy on transistor level

RESULTS

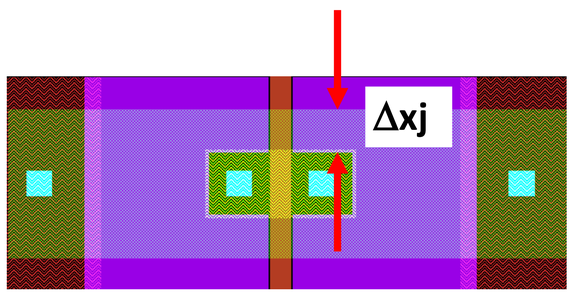
Suppression of TID induced source drain leakage by lateral junction isolation (JI) using silicide blocked well regions



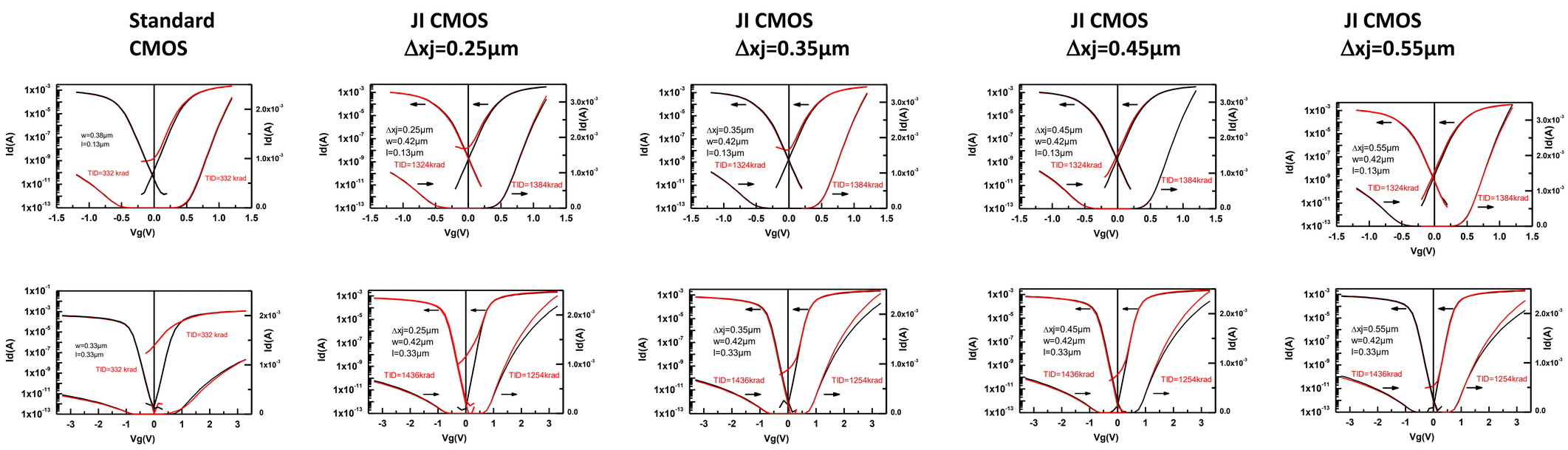
Standard CMOS transistor with source/drain-body isolation via STI. Well connection separated by STI.



Commonly used ELT transistot to suppress TID related source drain leakage. Well connection in separate ACTIVE region.



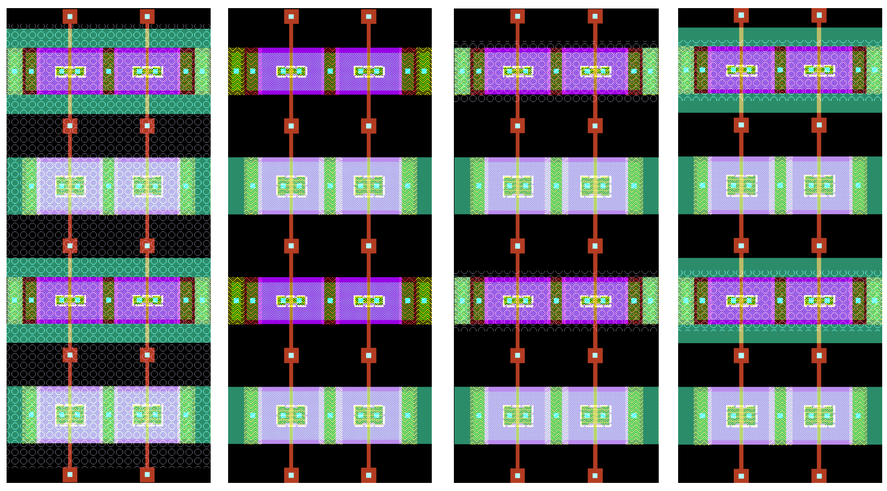
Mitigation of TID induced S/D leakage: Lateral junction isolation (JI) of MOS transistors by using a finely structured silicid blocker layer. Advanced litho processes enable a complete silicidation of the poly gate and to isolate the body regions from the source drain regions. JI enables a low resistance well connection in the same ACTIVE which sufficiently suppresses the turn on of parasitic bipolar transistors at single events after a high energy particle strike in the sensitive device region.



Degradation of MOS transfer characteristics measured @ Vd=|0.1|V of standard and junction isolated (JI) core and IO MOS transistors after exposure to ionizing radiation. For the JI MOS transistors the distance of the lateral source drain edges to the STI edge Δxj was varied from 0.25µm to 0.55µm.

TID Testing: Devices were irradiated with a Co-60 source at a dose rate of 10 krad/h. During the irradiation core/IO NMOS transistors were biased with the nominal gate voltage of Vg= 1.2 V/3.3 V. The source drain and body terminals were on Vss=0V. The gates of the PMOS transistors were connected with source during irradiation.

Suppression of SEU induced malfunctions of digital gates by means of redundancy on transistor level, each MOS transistor is replaced by a stack of two locally separated single transistors which share a common gate (CG)



Four inverter chain designs with stacked single MOS transistors enabling a redundancy on transistor level. The designs differ in the capability of NMOS to collect excess minority charge i.e. electrons after a particle strike.

Mitigation of SETs: Efficient draining of SEE induced excess majority charge carriers towards the body contact and excess minority charge carriers towards MOS device regions with collector functionality (deep n-well for NMOS and deep p-well for PMOS) to avoid that a significant portion of excess minority charge reaches the drain region. Sheet resistance of well regions in the source region crucially determines the turn on behavior of parasitic bipolar transistor.
Test circuit: Chain of 2200 JICG CMOS single inverter with RS-latch, NMOS and PMOS always with low resistance body connection in the same ACTIVE region, w_n=0.3µm, w_p=0.64µm, Δxj=0.45µm. The vertical distance of stacked single transistors 7.4 µm . 4 designs to test efficiency of SET mitigation measures:
D1: **isolated NMOS, 0 events detected**
D2: NMOS with deep n-well beneath NMOS active region, σ<4E-3 µm2/inverter
D3: standard NMOS , σ<3E-3 µm2/inverter
D4: **isolated NMOS, deep n-well in the whole inverter area, 0 events detected**

Switching speed and chip area consumption:
Due to the decreased driver capability and the increased gate area of a MOS transistor stack in comparison to a single MOS device JICG CMOS gates have an increased Inverter gate delay: JICG CMOS/Standard CMOS: 103ps/51ps. The chip area consumption is increased by a factor JICG CMOS/ Standard CMOS =2.3 .

SEE Testing: Heavy ion testing performed at RADEF heavy ion accelerator facility at the University of Jyvaskyla, Finnland, with 126Xe44+ ions, E= 2059 MeV, LET_bragg_peak=138MEVcm2/mg , irradiation through 100µm thick Kapton foil, flux= 1E5 cm^{-2} s^{-1}, tilt=60°, fluence 1E8 cm^{-2}, LET=138MeV cm^{-2}/mg.
No SEL events were detected for designs D1 and D4.

Summary & Conclusions

- A novel RHBD approach for radiation tolerant CMOS circuits fabricated in a 130nm bulk SiGe BiCMOS technology was successfully tested
- JICG CMOS transistor arrangements have proven very robust against TID induced source-drain leakage and SET induced malfunctions JICG CMOS designs with isolated NMOS transistors show the best SEE tolerance
- Core and IO PMOS transistors do not show any TID induced MOS parameter degradations. With a distance of the lateral source drain edges to the STI edge Δxj> 0.45µm core and IO JI NMOS transistor arrangements do not show significant TID induced degradations of MOS parameters
- Penalties for the improved radiation tolerance of JICG CMOS circuits are the significant increase of chip area and gate delay time.
- CMOS and LDMOS transistors with lateral junction isolation and redundancy on transistor level are promising candidates for mixed mode ASIC applications when an extreme radiation tolerance is required

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