JIGC CMOS Transistors for Reduction of Total Ionizing Dose and Single Event Effects in a 130nm Bulk SiGe BiCMOS Technology

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MOTIVATION & GOALS

Integration of radiation tolerant core and IO MOS transistors fabricated in a 130nm bulk SiGe BiCMOS technology for aerospace applications and high energy physics experiments

- Mitigation of TID (total ionization dose) and SEE (single event effects) induced malfunctions in digital circuits using a novel radiation hardening by design approach (RHBD)
- Reduction of TID induced drain leakage for NMOS transistors and channel pinch-off for PMOS transistors due to trapped fixed positive charges in the surface interface region of the shallow trench isolator (STI) by introduction of a lateral junction isolation (JI) of the MOS transistors.
- Negligible TID induced MOS DC parameter degradations for doses > 1 Mrad (60Co source)
- SEE onset LET_{50} > 100 MeV cm^2/mg by introduction of redundancy on transistor level

RESULTS

Suppression of TID induced source drain leakage by lateral junction isolation (JI) using silicide blocked well regions

Mitigation of TID induced S/D leakage: Lateral junction isolation (JI) of MOS transistors by using a finely structured silicid blocker layer. Advanced litho processes enable a complete silicidation of the poly gate and to isolate the body regions from the source drain regions. It enables a low resistance well connection in the same ACTIVE which sufficiently suppresses the turn on of parasitic bipolar transistors at single events after a high energy particle strike in the sensitive device region.

Suppression of SEE induced malfunctions of digital gates by means of redundancy on transistor level, each MOS transistor is replaced by a stack of two locally separated single transistors which share a common gate (CG)

Mitigation of SETs: Efficient draining of SEE induced excess majority charge carriers towards the body contact and excess minority charge carriers towards MOS device regions with collector functionality (deep n-well for NMOS and deep p-well for PMOS) to avoid that a significant portion of excess minority charge reaches the drain region. Sheet resistance of well regions in the source drain regions crucially determines the turn on of parasitic bipolar transistor.

Test circuit: Chain of 2200 JIGC CMOS single inverter with RS-latch, NMOS and PMOS always with low resistance body connection in the same ACTIVE region. \( w_n=0.3\mu m, \quad w_p=0.4\mu m, \quad x_j=0.45\mu m \)

The vertical distance of stacked single transistors 7.4 \( \mu m \) - 4 designs to test efficiency of SET mitigation measures:

D1: isolated NMOS, \( \Delta j \) events detected
D2: NMOS with deep n-well beneath NMOS active region, \( \Delta <|0.3\mu m \)
D3: standard NMOS, \( \Delta <|0.3\mu m \)
D4: isolated NMOS, deep n-well in the whole inverter area, \( \Delta < 0.3\mu m \)

Switching speed and chip area consumption:
Due to the decreased driver capability and the increased gate area of a MOS transistor stack in comparison to a single MOS device JIGC CMOS gates have an increased inverter gate delay. JIGC MOS/Standard CMOS: 10asis/51as. The chip area consumption is increased by a factor JIGC CMOS/Standard CMOS = 2.3.

No SET events were detected for designs D1 and D4.

Summary & Conclusions

- A novel RHBD approach for radiation tolerant circuits fabricated in a 130nm bulk SiGe BiCMOS technology was successfully tested
- JIGC CMOS transistor arrangements have proven very robust against TID induced source-drain leakage and SET induced malfunctions JIGC CMOS designs with isolated NMOS transistors show the best SEE tolerance
- Core and IO PMOS transistors do not show any TID induced MOS parameter degradations. With a distance of the lateral source drain edges to the STI edge \( \Delta j \geq 0.45\mu m \) core and IO JI NMOS transistor arrangements do not show significant TID induced degradations of MOS parameters
- Penalties for the improved radiation tolerance of JIGC CMOS circuits are the significant increase of chip area and gate delay time.
- CMOS and LDMOS transistors with lateral junction isolation and redundancy on transistor level are promising candidates for mixed mode ASIC applications when an extreme radiation tolerance is required

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