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JICG CMOS Transistors for Reduction of Total Ionizing Dose and Single Event Effects in a 130nm bulk SiGe BiCMOS technology

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We report on the mitigation of TID and SEE induced malfunctions for digital circuits fabricated in a 130 nm bulk SiGe BiCMOS technology using a novel RHBD approach. To avoid an increase of drain leakage for NMOS transistors and channel pinch-off for PMOS transistors due to trapped fixed positive charges at the lateral Shallow Trench Silicon interface we introduced a lateral junction isolation (Jl) of the MOS transistors instead of shallow trench isolation (STI). To suppress SEE induced malfunctions in CMOS circuits as a result of generated electron hole pairs after an high energy particle impact we have introduced a redundancy on transistor level combined with suitable device construction measures which ensures that the CMOS output node remains its signal integrity. The constructive measures applied result in a JICG CMOS arrangement (Junction Isolated Common Gate) as a basic element for digital circuits suitable for applications in harsh radiation environments. The redundancy on transistor level in logical CMOS gates is achieved by splitting each NMOS and PMOS block into a series connection of two spatially distributed low side and high side blocks which share common gates (CG). The radiation tolerance of the JICG CMOS circuits designed were tested using a gamma source up to TIDs > 1.3 Mrad(Si) and SEE tests were performed at a heavy ion accelerator with LET values > 100 MeVcm² mg⁻¹ (LET:linear energy transfer). The penalties for the substantially increased radiation tolerance of the JICG CMOS gates as an increased chip area and a reduced digital switching speed will be discussed.

Submission declaration

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