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## 1.28 and 5.12 Gbps multi-channel twinax cable receiver ASICs for the ATLAS Inner Tracker Pixel Detector Upgrade

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We present two prototypes of a gigabit transceiver ASIC, GBCR, in a 65-nm CMOS technology for the ATLAS Inner Tracker Pixel readout upgrade.

The first prototype has four upstream receiver channels and a downstream transmitter channel. Each upstream channel receives the data at 5.12 Gbps through a 5-meter 34-AWG twin-axial cable from another ASIC called Aggregator and drives the optical transmitter in a VTRx+. The upstream channels consist of an equalizer, a DFE module (only in the 4th channel), a CDR, and an output driver. The downstream channel receives the data at 2.56 Gbps from an optical receiver of the VTRx+ and drives a receiver of the Aggregator through a cable of the same type. The test results indicate that the prototype chip works as expected except that the test of the DFE module is still ongoing. For an upstream channel, the total jitter (peak-peak) is 72.7 ps when the CDR is off and decreases to 35.4 ps when the CDR is on. The chip consumed 318 mW when the CDR is on. A TID test has been begun and will be completed in early September. A SEE test will be performed in the future.

The second prototype has seven upstream channels and each channel works at 1.28 Gbps to recover the data directly from the RD53 driver through a cable of 1-m flex and 6-m Twinax. Each channel consists of an equalizer, a retiming logic, a limiting amplifier, and an output driver. The retiming clock is provided by a phase shifter. From the post-layout simulation results, the additional jitter of the output signal is about 80 ps (peak-peak) when the retiming logic is off. When the retiming logic is on, the total jitter is estimated to be 50 ps. The entire chip consumes about 150 mW when the retiming logic is off. The design will be submitted by the end of October 2019.

### Submission declaration

Original and unpublished

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