A fully functional peripheral readout logic design for a CMOS pixel sensor prototype developed for the CEPC vertex detector

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ABSTRACT

The CEPC vertex detector system expects high resolution, low material, fast readout, and low power. Monolithic CMOS Pixel Sensors (CPS) are preferred. In the past, several chips have been developed for studying the sensing diode and the readout architectures. This work presents a fully functional CPS， especially the design of the peripheral readout logic design. We realize a fast readout architecture to full fill the requirements of 12 MHz/cm^2 and dead time of 500 ns for a double column, and necessary functions for adapting different pixel designs, trigger mode, and interface frequencies.

Design Overview

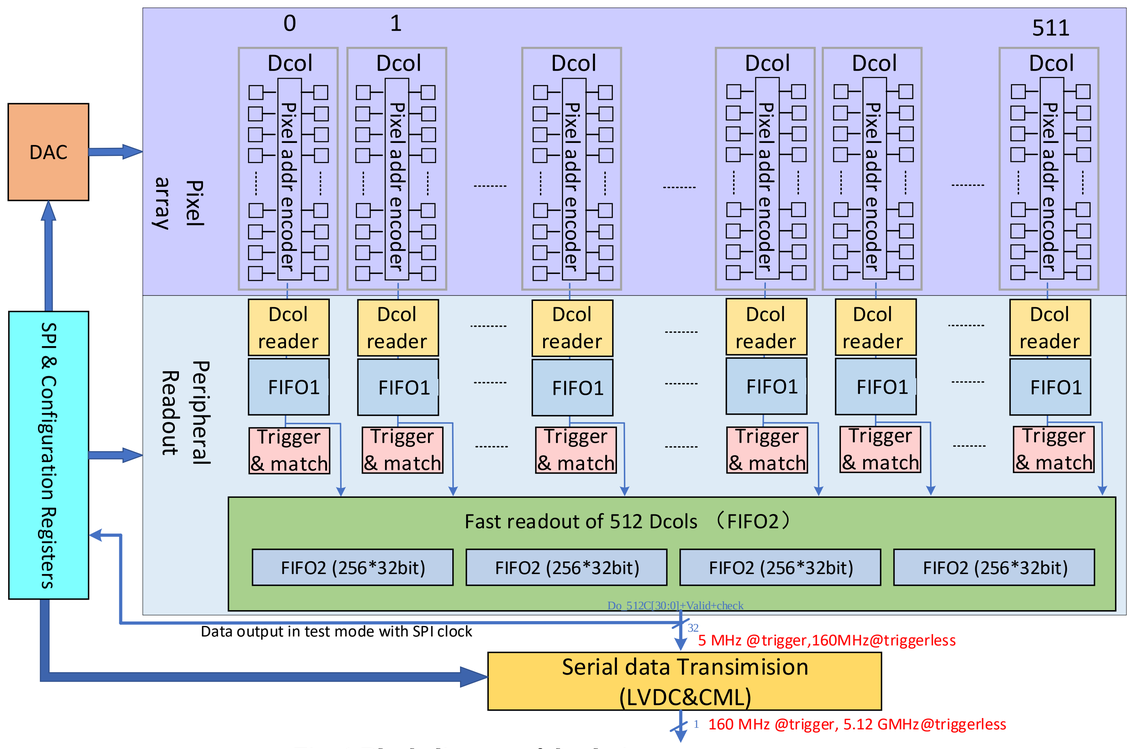

Fig. 1 Block diagram of the design

■ Main feature

- Pixel array: 512 * 1024
- Pixel pitch: 25 μm, two version
- Time walk: <25 ns
- Dead time for pixel: 25 ns
- Dead time for Dcol: 500ns
- Power consumption: 200mW/ cm^2
- Support trigger and triggerless mode
- Support data compression
- On-chip test
- Bias adjustable by DAC
- Data output by serial interface
- SPI configuration

Peripheral readout logic design

■ Readout for two version of pixel designs

In our design, two different kinds of pixel readout circuits (Fig. 2) were realized. The timing of these two schematics are different. In the peripheral circuits, the readout timing is degined as Fig. 3 and is finally realized with the same readout circuit.

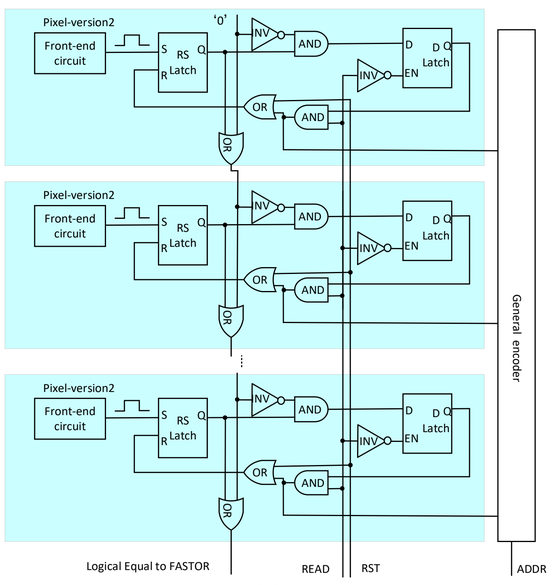

Fig. 2 simplified schematic of the pixels (a) FEI3-like version, (b) ALPIDE-like version

Designed readout timing: Readout timing of double column is shown in Fig. 3. FASTOR/VALID is set when any pixel in the double column is hit. Since the hit pixel will be reset after readout, FASTOR/VALID changes into zero when the last hit address is read out. TDFOR and TDVLD should be less than 44.5 ns (two clock cycles -5.5ns) and 19.5 ns (one clock cycle-5.5ns) respectively. (Because TDFOR refers to READ posedge and TDVLD refers to READ negedge). FASTOR/VLIDA is synchronized as Fastor_syn/Valid_syn in peripheral logic. READ is generated when Fastor_syn/Valid_syn is "1". The cycle of READ is 50ns which corresponds TDA (maximal delay of the addressing encoding for FEI3 schema) is 19.5 ns and TDA_ALP (maximal delay of the addressing encoding for ALPID schema) is 44.5ns. For the peripheral logic, the hit timestamp (Time_stamp[7:0]) is recoded at the positive edge of Fastor_sync/Valid_syn. The hit timestamp has been corrected internally by subtracting 1 clock cycle because Fastor_sync/Valid_syn has one clock cycle delay referring to Fastor/Valid. The address of hit pixel (ADDR[9:0]) is taken at the clock positive edge when ADDR[9:0] are available.

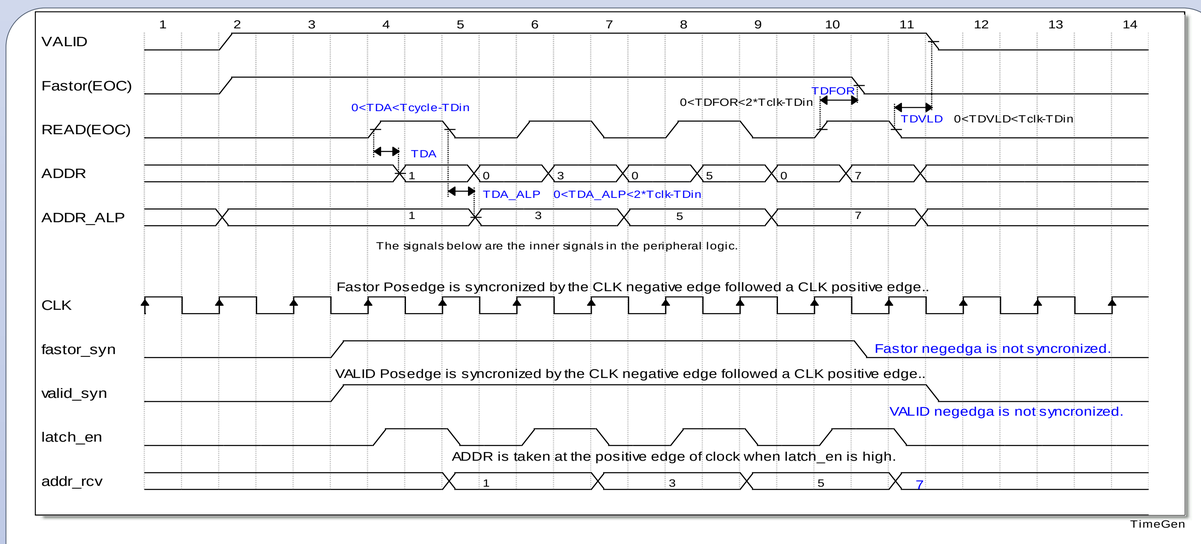

Fig.3 Designed readout timing for the two version of pixels

■ Trigger & Triggerless mode readout

- In trigger mode, all the received data are stored in FIFO1, but only the matched data are send to FIFO2. In triggerless mode, all the data are buffered in FIFO1, and FIFO 2 is only used for matching different clocks.
- In order to reduce the pixel area, the timestamp is only recorded in Dcol level. Uncertain of the timestamp is considered in the trigger discriminating logic.

■ Data compression

Compression method: As shown in Fig. 4, recording the address of the first pixels in a package, the following three pixels are indicated by a three-bit code, where "0" indicates no hit in the pixel and "1" indicates a hit pixel. This function is realized in Dcol reader.

Benefits: Reduce the required depth of FIFO1 and FIFO2 and the data volume to be send off chip (30~50% reduction if compressible).

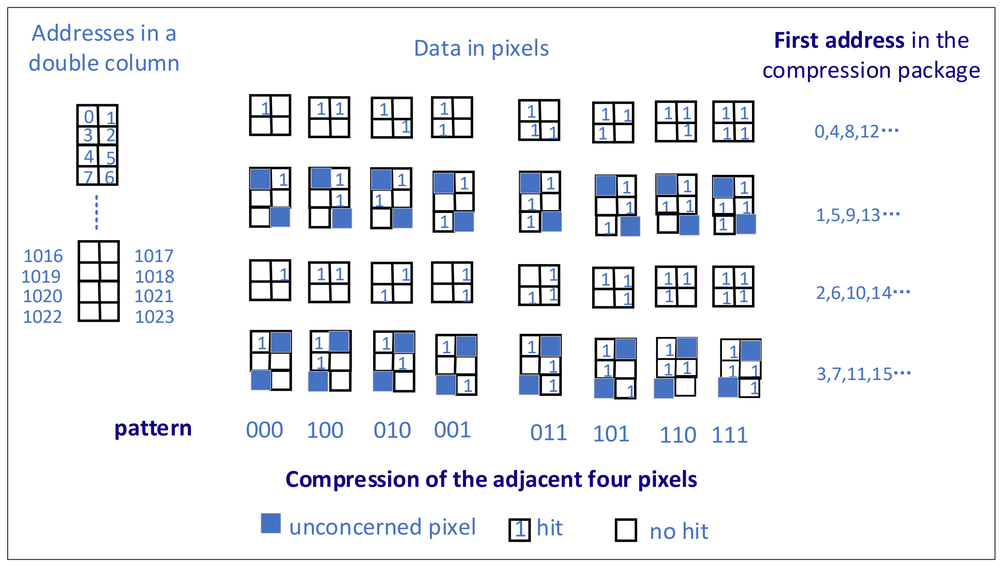

Fig. 4 Data compression (a) compression method, (b) data format of FIFO1, (c) data format of FIFO2

Results

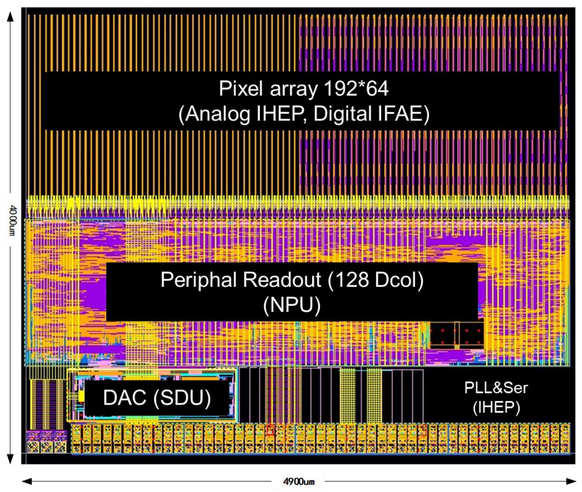

Fig. 4 chip layout

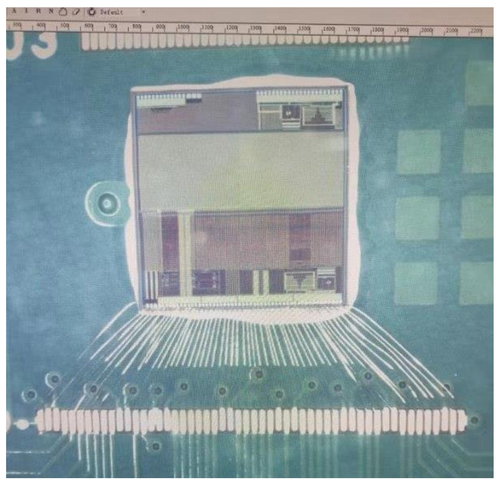

Fig. 5 photo of the chip

The design was finally realized in the 0.18μm Tower Jazz process. In the simulation, all the proposed functions were well supported. The hit rate of 120MHz for 1024×512 pixels can be well processed. The power consumptions of the peripheral readout logics are estimated as 25~30 mW/cm^2 in trigger mode and 35~45 mW/cm^2 in triggerless mode. The peripheral readout logic was designed for a 1024×512 pixel array and was reduced for 192×64 pixel array in order to be integrated in the prototype of CMOS pixel sensor named TaichuPix1. The chip area is 4.9 mm×4 mm, where the peripheral readout logic occupies 4.8 mm×1.3 mm. TaichuPix1 is under evaluation, and the test results are expected soon.