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A fully functional peripheral readout logic design for a CMOS pixel sensor prototype developed for the CEPC vertex detector

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The CEPC vertex detector system expects low resolution, low material, fast readout, and low power. Monolithic CMOS Pixel Sensors (CPS) are preferred. In the past, several chips have been developed for studying the sensing diode and the readout architectures. This work aims to realize a fully functional peripheral readout logic design for CPS.
In the CEPC experiments, the bunch spacings and the hit densities are 680ns and 2.5/bunch/cm2 at 240GeV, 210ns and 2.5/bunch/cm2 at 160GeV, and 25ns and 0.2/bunch/cm2 at 91GeV. The maximal the data rate is near 120MHz, and the dead time for the pixel readout is about 500ns every double column. The existing CPS cannot satisfy all the requirements. Therefore, we propose a new readout architecture, where the hit pixel addresses in a double column of the pixel array are read out based on the data-driven scheme like FEI3 and ALPIDE, and all the double columns are read out parallel. The main functions of the peripheral readout circuits include: providing the read control signals for both ALPIDE and FEI3 timing, supporting trigger and triggerless modes, and providing real-time data compression. The possible error of timestamps is considered and a time window can be set in trigger mode. The design is also adapted with different address orders of pixels in a column. In addition, the chip tests are considered. Including the scan chains and the memory BIST, we also support to mask pixels with a well-designed setting flow and to generate the test patterns for the function test of peripheral readout circuits.
The design was finally realized in the 0.18μm Tower Jazz process. In the simulation, all the proposed functions were well supported. The hit rate of 120MHz for 1024×512 pixels can be well processed. The power consumptions of the peripheral readout logics are estimated as 25˜30mW/cm2 in trigger mode and 35˜45mW/cm2 in triggerless mode. The peripheral readout logic was reduced for 192×64 pixels in the CPS prototype named TaichuPix1. TaichuPix1will be characterized this November.

Submission declaration

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