X-ray irradiation studies of a large area HVCMOS pixel sensor chip for ATLAS ITk

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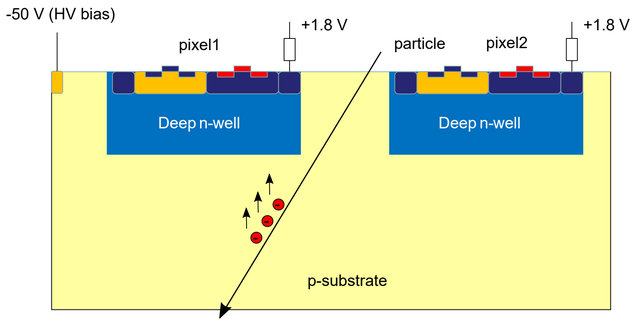
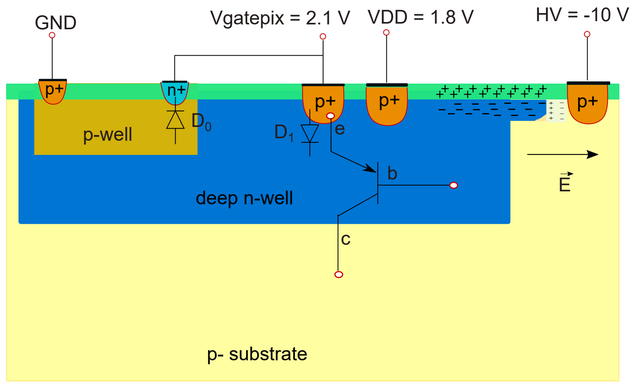
HVCMOS sensor in AMS 180 nm process



Working Principle:
Depletion region is enlarged by the application of high voltage. Electrons which are generated by particle hit are collected by the deep n-well (by drift). Thickness of the sensor can be reduced to 50 µm by thinning.

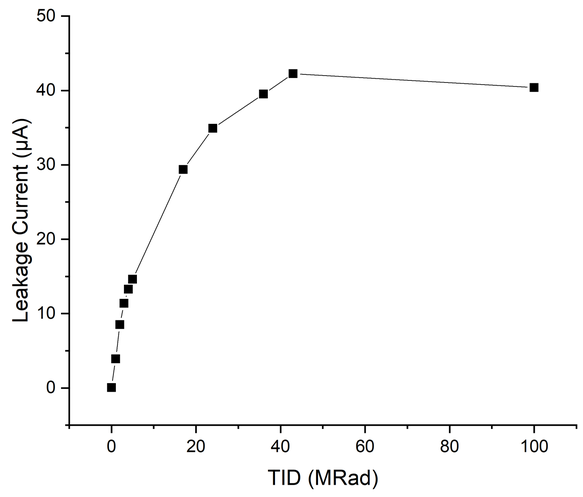
This work presents the results of X-ray irradiation studies conducted on a (1.96 x 0.36) cm^2 HVCMOS prototype with triggered readout. The pixel size is (50 x 60) μm^2 .
The ATLASpix sensors follow the large-charge collection electrode topology. Pixel-electronics include a charge sensitive amplifier, a comparator, 4-bit tune DAC and RAM to store the configuration bits. Read out circuitry is located at the chip periphery to avoid digital cross-talk.

Effect of radiation on Si-SiO_2 interface



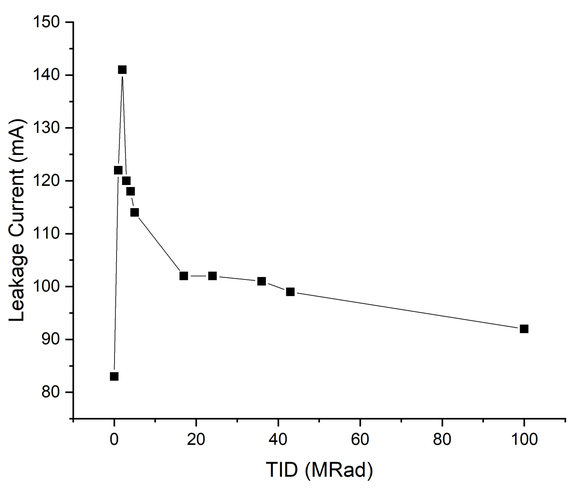
The formation of a parasitic BJT is possible between the pwell of rotection diodes, deep nwell and the p-substrate. This hypothesis has been proven by the following experiment: The hypothetical PNP transistor has its emitter, base, collector terminals at pwell for protection diode (Vgatepix), deep nwell (VDD) and p-substrate (HV) respectively. Keeping the high voltage constant. at -10 V, VDD was varied from 1.8 to 1.2 V. The decrease in collector-base reverse bias resulted in a steady decrease of the HV leakage current from 24 µA to 22 µA. At this point, the emitter-base forward bias was increased from 0.6 V to 0.8 V, by increasing Vgatepix. A sudden increase in the HV leakage current (from 20 µA to 100 µA) was observed, implying the conduction of the parasitic PNP transistor. The formation of parasitic BJT is also possible in the pixel area but it has not been verified by this work.

High Voltage leakage current after irradiation



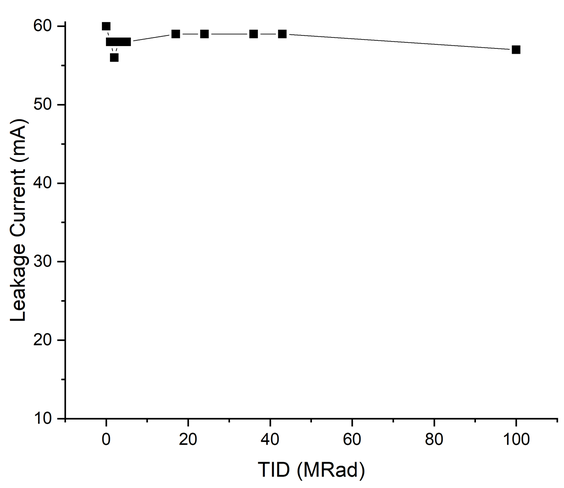
The trapping of holes in STI oxide leads to strong inversion of the p substrate beneath. This induced n-type channel like region touches the deep nwell and the p+ high voltage contact. It causes a strong electric field at the extended deep nwell - p+ junction. The leakage current at this reverse bias pn junction increases at higher radiation doses because of the increase in number of holes getting trapped in STI oxide. The breakdown of this pn junction can cause a high leakage current. This effect was annealed over a period of time.

Leakage current (digital)



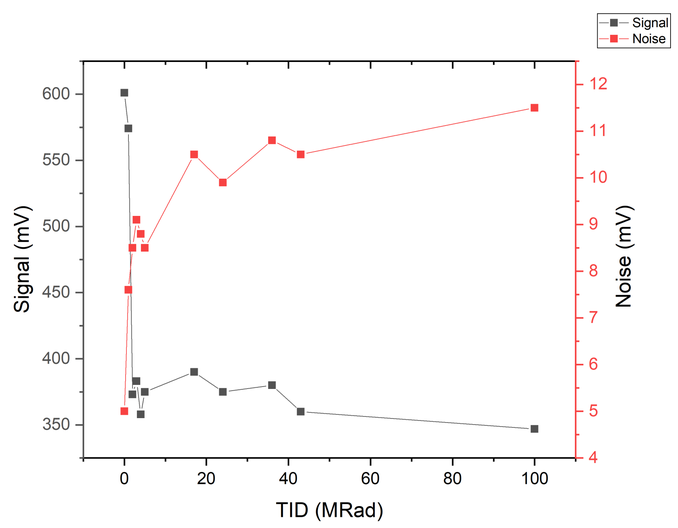
The digital power, VDDD current consumption is mostly because of linear NMOS transistors in the digital part. The lowering of threshold of NMOS due to oxide traps causes a steep increase in the leakage current till 5-10 MRad. A slow and steady buildup of interface trap charge dominates beyond 10 MRad. For NMOS, the interface traps are negatively charged which causes positive threshold voltage shifts. Hence the leakage current takes a negative slope after 10 MRad.

Leakage current (analog)



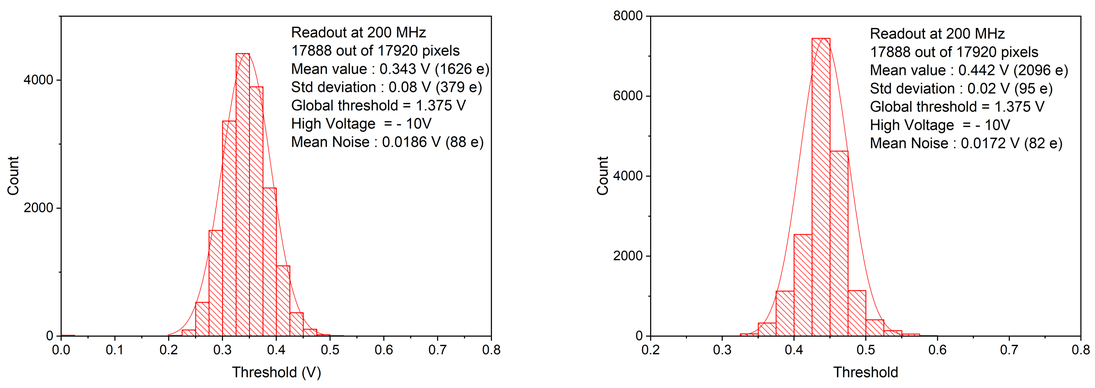
The static current consumption of the analog power, VSSA is measured. It follows an almost steady or a slight downward trend because PMOS devices dominate the design. Almost all NMOS in the analog part are enclosed. Total power consumption of the pixel matrix is measured to be 316.67 mW/cm^2.

Signal and noise plots for a single pixel for 500mV injection input

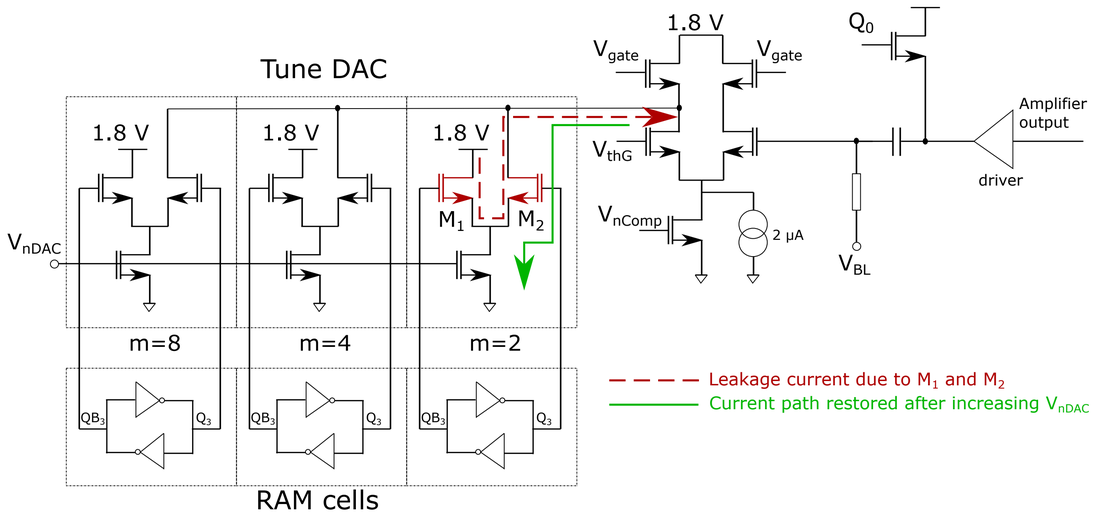


During each irradiation step, for an injection voltage of 500 mV, output SNR was measured after 45 minutes of annealing. The SNR degrades rapidly untill 5 MRad. It is believed to improve due to annealing, which degrades at higher doses. Most of the pixels follow this trend.

Threshold tuning



Threshold distribution of 17,888 pixels of irradiated ATLASpix1_M2 is shown before tuning (left) and after tuning (right). Threshold tuning was performed after a TID of 100 MRad. 16 noisy pixels were masked and 16 did not respond. The readout was performed at a rate of 200 MHz. The threshold dispersion was reduced by a factor of two after tuning as shown. The mean threshold was 2096 e^- with a standard deviation of 95 e^-. The mean value of noise distribution over the entire pixel matrix after tuning was 82 e^-. Due to the increase in noise after irradiation, the global threshold was set to 1.4 V and the baseline voltage was set to 0.9 V.



Threshold tuning was performed after 100 MRad TID and 8 hours of annealing. The tuning circuit is based on a current-mode DAC. Variation in Tune DAC current adds to offset of the first stage of comparator. The NMOS transitors, M_1 and M_2 suffer from radiation damage and starts leaking. This causes the current to flow in the direction indicated by dotted red arrows. It causes negative shift in the threshold of the comparator. To mitigate this, V_{nDAC} was increased, resulting in the restoration of current path shown in solid green line. It was observed that increasing of V_{nDAC} results in better tuning.

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