A Fully Integrated 10-bit 100 MS/s SAR ADC with Metastability Elimination for the High Energy Physics Experiments

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Introduction

- The demand of high speed, low power analog-to-digital converter (ADC) is growing fast in future high energy physics experiments or in upgrade of current detectors.
- The ADC implements 10-bit resolution and 100MS/s sampling-rate based on high-speed asynchronous successive approximation register (SAR) architecture.
- A non-binary weight capacitor digital-to-analog converter (C-DAC) network and a hybrid capacitor switching architecture are used to increase conversion accuracy and speed.
- A metastability elimination technique is employed to avoid comparator metastability, and then reduce the conversion error rate (CER) at a high-speed asynchronous operation.
- The ADC integrates an internal bandgap biasing circuitry, a high bandwidth reference buffer, a digital clock management unit, and 10-bit digital output buffers with unsigned binary format.
- The full custom logic cells without floating nets are designed to improve the performance of the radiation hardness.
- The ADC was designed and fabricated in a 40 nm CMOS process. It achieves a good dynamic performance with ENOB ~ 9.3bit at 100MS/s with 14.97MHz input signal. The measured power consumption of the ADC core is 1.32 mW and the total power consumption is 8.5 mW including reference generator under a 1.2V supply.

Non-Binary Weight C-DAC

- Top-plate Direct Sampling
  - The MSB capacitor and its switching can be eliminated
- Non-Binary Weight Algorithm
  - One extra redundant bit-cycle is added to alleviate the C-DAC setting accuracy
  - C9 = C1 Interpolated VCM-based Switching
    - One capacitor is split into two segments with one switching from Vrefp to Vrefp and another switching oppositely
    - Common-mode voltage of the C-DAC remains fixed voltage
  - C4 Monotonic Switching
    - Only the LSB capacitor switches monotonically
    - Common mode voltage variation can be reduced

Digital Error Correction

- The digital output can be expressed as:
  Dn = 2*[B(9:1)] + 2*[B(8:1)] + 2*[B(7:1)] + 2*[B(6:1)] + 2*[B(5:1)] + 2*[B(4:1)] + 2*[B(3:1)] + 2*[B(2:1)] + 2*[B(1:1)] + 2*[B(0:1)]
- The DEC converts the 11bit non-binary codes to 10bit binary code

Chip Micrograph

- The SAR was designed and fabricated in a 17nm 40 nm CMOS process. It occupies 0.078 mm² active area including reference generator and the core area is only 0.037 mm² before shrink.

References