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A fully integrated 10-bit 100 MS/s SAR ADC with metastability elimination for the high energy physics experiments

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The demand of high speed, low power analog-to-digital converter (ADC) is growing fast in future high energy physics experiments or in upgrade of current detectors. Also, the ADC becomes more and more critical in the front-end application specific integrated circuit (ASIC) design. Based on these considerations, a fully integrated, 10-bit 100MS/s successive approximation register (SAR) ADC with metastability elimination technique for the high energy physics experiments has been developed.

The ADC is composed of an internal bandgap biasing circuitry, a high bandwidth reference buffer, a digital clock management unit, and 10-bit digital output buffers with unsigned binary format. A non-binary weight capacitor digital-to-analog converter (C-DAC) network and a hybrid capacitor switching architecture are used to increase conversion accuracy and speed. A metastability elimination technique is employed to avoid comparator metastability, and then reduce the conversion error rate (CER) at a high-speed asynchronous operation. The full custom logic cells without floating nets are designed to improve the performance of the radiation hardness.

The ADC was designed and fabricated in a 40 nm CMOS process. It occupies 0.078 mm2 active area including references and the core area is only 0.037 mm2. The measured power consumption of the ADC core is 1.32 mW and the total power consumption is 8.5 mW including references under a 1.1V supply. The resulting figure-of-merit (FOM), for sampling rate 100 MS/s, is 135 fJ/conversion-step. The largest power goes to a robust reference buffer that comprise a fully integrated ADC ASIC. It achieves a good dynamic performance with ENOB ˜ 9.3bit at 100MS/s with 14.97MHz input signal. The measured spurious free dynamic range (SFDR), total harmonic distortion (THD) and signal-to-noise ratio (SNR) are 72dB, -69dB, 58dB, respectively. And the measured DNL and INL are +0.67/-0.54 LSB and +0.62/-0.4 LSB respectively.

Submission declaration

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