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Design of a low-noise, high-linearity, readout ASIC for CdZnTe detectors in gamma spectrometers

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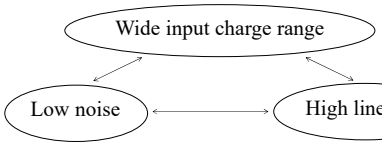
Abstract

The presented work aims to achieving low-noise and high-linearity in a wide range of measured energy, as well the input charge. In order to improve linearity, an active resistor and a high-linear analog buffer are employed. A CR−(RC)^2 shaper is proposed. Different types of resistances are utilized in the first stage and second stage of the shaper, to achieve low noise and high linearity at the same time. One channel of the proposed circuit is composed of a preamplifier, a shaper, a peak and hold circuit, which can automatically detect the peak of shaper output voltage. The output voltage is not read out, except a channel is hit. Therefore, power consumption is decreased.

A prototype chip with 8 channels has been designed and fabricated in a standard commercial 1P6M 0.18 μm CMOS process. Die area of one channel is about 650 μm × 110 μm. The input charge range is from 1.5 fC to 60 fC. Peaking time can be adapted from 3 μs to 5 μs. Measured ENC is about 180 e$^-$ at input capacitor of 0 F with the slop of 7.7 e$^-$/pF. The gain is 18 mV/fC at peaking time of 4 μs. Nonlinear error is less than 1%.

Motivation & Design Consideration

Element recognition REQUIRE Wide input charge range & High linearity
High energy resolution REQUIRE Low noise

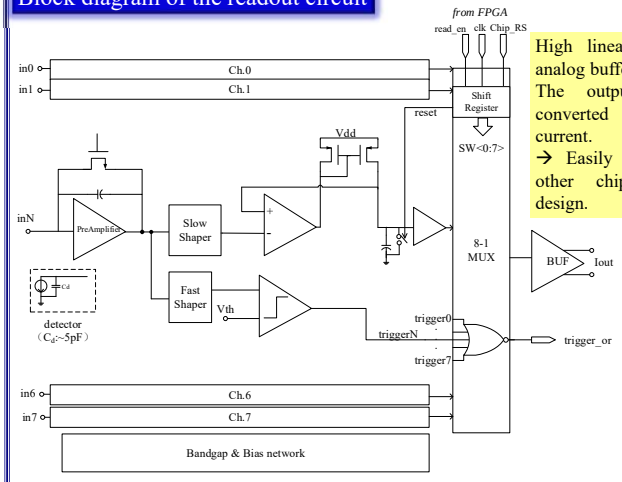


Conflicts should be solved.
Other conflicts?

- Feedback capacitance
- Shaper order
- Low noise shaper

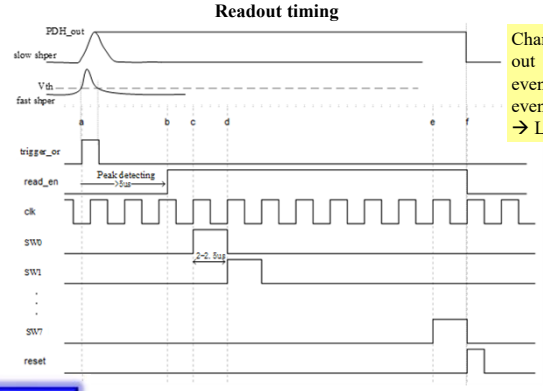
- Limited gain
- High linearity resistor
- High linearity buffer
- Acceptable area and power consumption

Block diagram of the readout circuit



High linearity differential analog buffer is employed. The output voltage is converted to differential current.
→ Easily connected with other chips in system design.

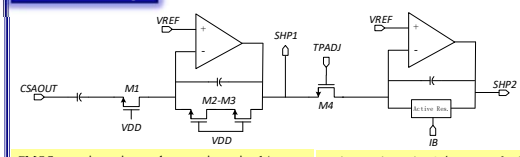
Readout timing



Channels are read out in turn, if an event happens. No event no output.
→ Low power

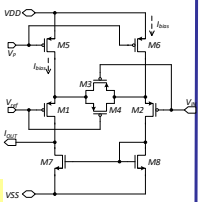
Circuit design

Proposed CR-(RC)^2 shaper

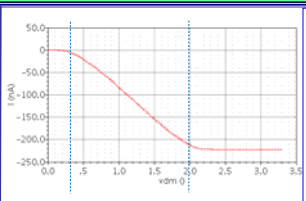


CMOS transistor is used as resistor in 1st stage. →Decrease noise & improve linearity (Vg=VDD)
Order is 2. → Increase SNR, Get fast pulse tail.

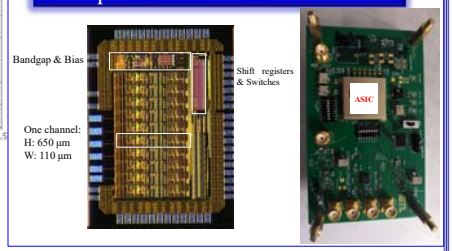
Active resistor in 2nd stage. → improve linearity
Peaking time is adjustable by Tpadj and IB.



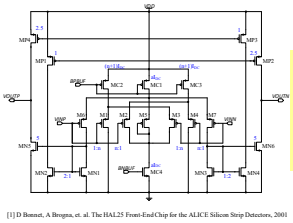
Schematic of the active resistor



Microphoto of the ASIC & test board

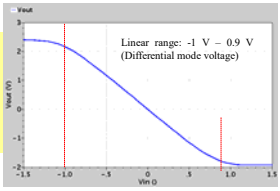


Analog buffer

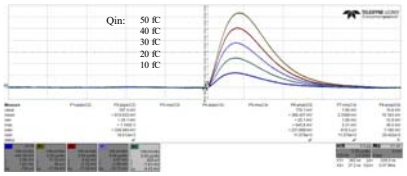


[1] D Bonnet, A Brogna, et. al. The HAL25 Front-End Chip for the ALICE Silicon Strip Detectors, 2001

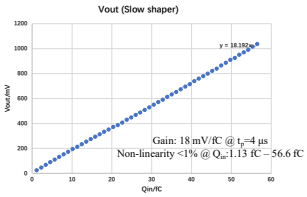
- High linearity.
- Push-pull provides high output current.
- The output of dummy channel is used as the reference voltage in order to compensate the influence of temperature.



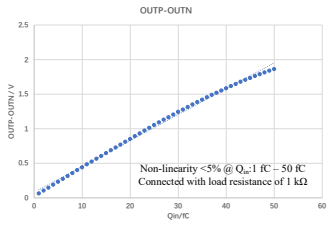
Experimental results



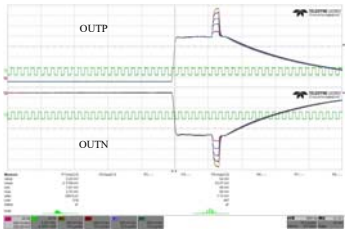
Measured oscilloscope wave of output voltage with different input charge



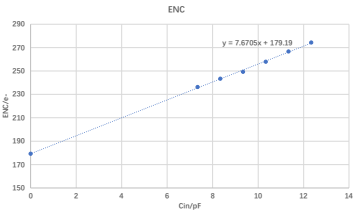
V_{out} VS Q_{in} (Slow shaper)



V_{out} VS Q_{in} (Analog buffer)

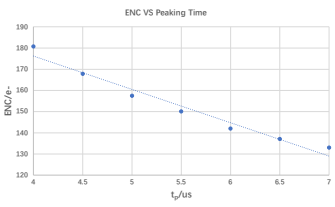


Measured oscilloscope wave of OUTP and OUTN



Measured ENC versus input capacitance @ peaking time: 4 μs.

The slop is about 7.7 e$^-$/pF, which is required by large input capacitance.



ENC VS Peaking time

Lower noise can be obtained with longer peaking time, since most of the noise is contributed by the thermal noise.

Summary

Performance parameter	Value
Channel number	8
Input charge range	-1.5fC — -60fC
Peaking time	3 — 5 μs
Gain	18 mV/fC @ t_p=4 μs
Nonlinear error	<1% @ t_p=4 μs, Q_{in}:1.13 fC – 56.6 fC
ENC (RMS.)	180e$^-$+7.7e$^-$/pF @ t_p=4 μs
Power supply	3.3 V
Power dissipation	< 4.62 mW/channel
Die area	1.75mm × 1.31 mm
Process	0.18um 1.8V/3.3V Mixed-Signal CMOS
Connection with detector	AC coupled
Bias and reference voltage	Built-in