**Testbeam measurements with passive CMOS pixel sensors in 150 nm LFoundry technology bump-bonded to the RD53A readout chip**

**Passive CMOS pixel sensor**
- 150 nm LFoundry technology
- 64 x 64 pixel matrix with 50 x 50 µm² pixels
- Thickness of 100 µm (>85 µm Si)
- Resistivity of bulk material: > 2 kΩcm
- Fully depleted @ ~20 V
- Mounted on RD53A readout chip
- Different sensor designs realized
  - Implant widths ranging from 15 – 30 µm
  - N-well (NW) and optional deep n-well (DNW)

**Signal and noise performance**
- ENC @ ~850 e threshold: ~75 e
- No difference across sensor flavors
- Low noise due to low capacitance (~40 ff)
- Charge signal of MIP (traversing ~85 µm silicon)
- Signal (MPV): ~6000 e @ 60 V (fully depleted)

**Efficiency measurements**
- All sensor flavors show high efficiency (> 99.5 %)
- No significant difference across sensor flavors
- Sensor already at low bias voltages (> 5 V) fully efficient

**Characterization in Testbeam**
- (Unirradiated) passive CMOS pixel sensor characterized using 2.5 GeV electron beam (ELSA, Bonn)
- High-resolution beam telescope used (Mimosa26)
- Fast timing reference plane for precise time-stamping (ATLAS FE-4)

**Cross-talk measurements**
- Cross-talk: Charge deposited in one pixel can induce a parasitic charge in neighboring pixels due to inter-pixel capacitance $C_p$ and $C_{pp}$
- Has impact on maximum hit rate and position reconstruction
- Cross-talk threshold estimated by injecting into neighboring pixels while reading the center pixel
- Overall cross-talk < 1 %
- DNW-flavors show slightly larger cross-talk compared to NW-flavors
- Pixels with larger implant widths show larger cross-talk compared to pixels with smaller implant widths

**ATLAS Phase-II Upgrade**
- New ATLAS pixel detector
- 5 layers of pixel detectors
- Hybrid pixel detectors with 3D (inner layer) and planar sensors (outer layers)
- Pixel size: 50 x 50 µm² (25 x 100 µm²)
- Thickness: 100 µm (150 µm thick)

**CMOS technology advantages**
- Multiple metal layers as re-distribution layers (avoids elongated inter-gap pixels)
- MIM-capacitors for AC-coupling (no leakage current compensation needed)
- High-resistive polysilicon as bias resistor (no punch through implantation needed)