Development of CdTe Hybrid Pixel ASIC for Hard X-ray Imaging

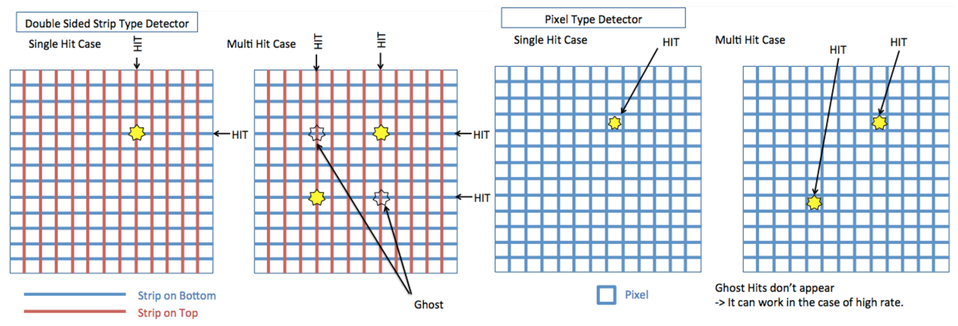
Tadashi Orita[1], Tenyo Kawamura[1], Kairi Mine[1], Shin'ichiro Takeda[1], Shin Watanabe[2], Hirokazu Ikeda[2], Tadayuki Takahashi[1]

[1]*Kavli IPMU, The University of Tokyo*

[2]The Institute of Space and Astronautical Science, Japan Aerospace Exploration Agency

Introduction

Thanks to its high atomic number, high detection efficiency and good energy resolution, cadmium telluride (CdTe) semiconductor has been regarded as a promising material for hard X-ray observation and applied to many fields [1, 2]. It can have a fine pitch structure that realizes a higher position resolution down to ~50μm needed for high quality imaging. There are two approaches to read out the large number of fine pitch channels. One is low noise micro strip type ASICs. The other is pixel type ASICs where circuit cells are two-dimensionally arranged to be directly connected to each pixel sensor. Pixel configuration has advantages of connectivity with low input stray capacitance. In the high count rate case, such as in medical applications, pixel type ASICs and detector could avoid ghost hits due to accidental coincidence in the same electrode. In this poster, we introduce a new 28 by 28 pixel type low noise front end ASIC based on the collection of analog blocks, we have developed in the series of prototype ASICs[3].



ASIC ARCHITECTURE

The pixel type ASIC (TOP01A784) is implemented with TSMC 0.35um CMOS technology. Fig.1 shows a micro-photograph of the ASIC itself. Fig.2 shows the schematic inside of the pixel. Each pixel has an 11-bit shift register which includes control bits for DACs bits, the test pulse disable bit (TPENB) and the comparator disable bit (KILLB). All pixel circuit's gate voltage (VGG) of a feedback MOS transistor for a CSA, threshold voltage (VTH) for a comparator, voltage for generating test pulses (TPDC) and initial voltage of the ramp voltage for AD conversion (VREF) are controlled with four 8-bit current DACs. The HOLD and TRACK signals are controlled from outside to keep flexibility of the operation sequence. If the TRACK bit is low, the hold circuit works as a peak-hold circuit. Otherwise, it works as a sample-hold circuit. The hit signals from the comparator (HITX, HITY) are summed over the entire chip and output to an external control box, while the signals are also summed in each row and column and recorded to provide X and Y hit information. The left side of peripheral area of the ASIC has digital buffers and the digital control circuit for each row. The top side of that has the circuits blocks generating bias voltages for all analog circuits, digital buffers, digital control circuits for each column, a shift register that can be controlled from outside and a 10-bit Wilkinson type ADC. The Wilkinson ADC consists of a ramp generator, gray-code counter, and latches for each column for a parallel AD conversion. We also can control the ramp signal's slope from outside.

UPPER SIDE BLOCK
- Bias Circuit
- Digital Buffers
- Digital Control Circuit for each column
- Shift Registers for Control Bits and DACs
- 10-bit Wilkinson type ADCs for all columns (ramp generator, gray-code counter, latch circuit)
- DAC for threshold voltage
- DAC for ramp signal slope
- DAC for reference voltage of ADC
- DAC for test pulse voltage
- Analog Buffer

LEFT SIDE BLOCK
- Digital Buffers
- Digital Control Circuit for each row

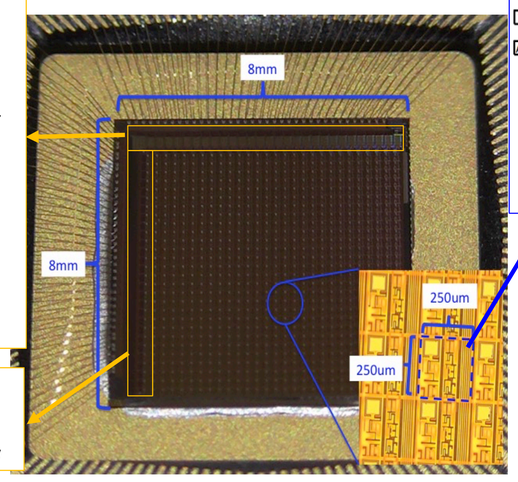


Fig.1 Bare Chip

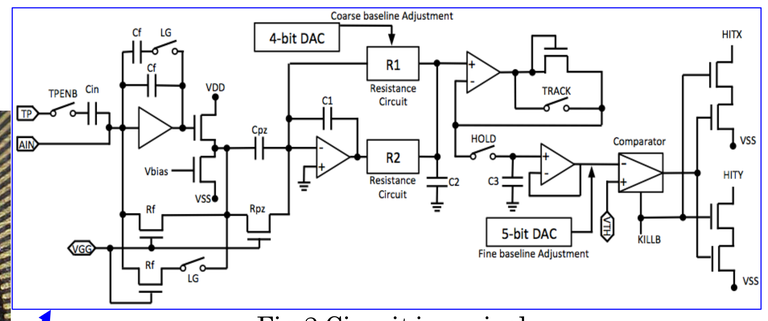
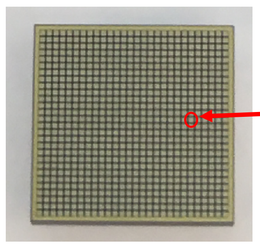


Fig.2 Circuit in a pixel



Pixel size : 250μm x 250μm
Thickness : 750μm

Fig.3 Pixel-type CdTe Sensor

Table.1 Properties of the TOP01A784

Chip Size	8.0 mm by 8.0mm
Pixel Area	7.0 mm by 7.0 mm
Number of channels	28 by 28 (Total : 784 ch)
Pixel Size	250 μm by 250 μm
Noise Performance	50 e^- (RMS) at 0 pF Load
Power Consumption	0.2 mW/channel
Peaking Time	~3.0 μs
Dynamic Range	~100,000 e^- (High Gain Mode) ~200,000 e^- (Low Gain Mode)

Experiment

Test Pulse Measurement

One of DACs in the peripheral area of the ASIC is for generating the test pulse and its one bit corresponds to 0.3 fC. With its test pulse signal, we conducted the equivalent noise charge (ENC) measurement experiment and linearity after offset adjustment. The ENC is 50 electrons, the integral non-linearity (INL) of the high gain mode is 1.1% and that of the low gain mode is 1.5% (Fig.4). Fig.3 shows the waveforms of analog signals. Each waveform is monitored via an analog buffer in the ASIC. Its pulse height gain is 80 mV/fC. The ADC clock from the external control box is 25MHz. The slope of the ramp signal for AD conversion is −25 mV/μs.

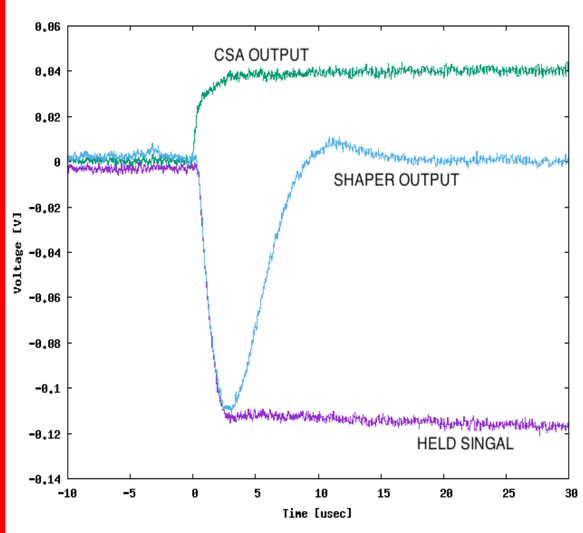


Fig.3 Waveforms

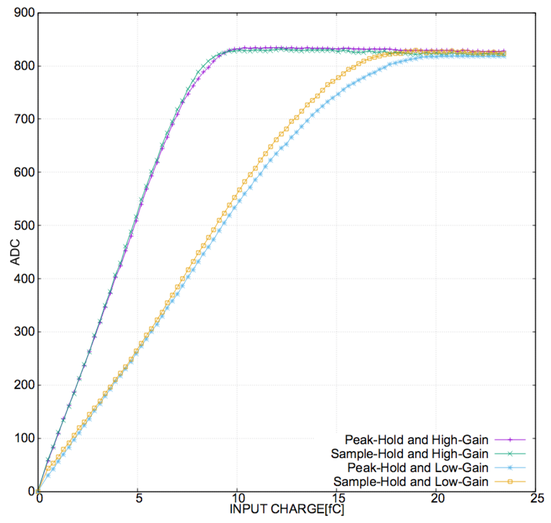


Fig.4 Linearity

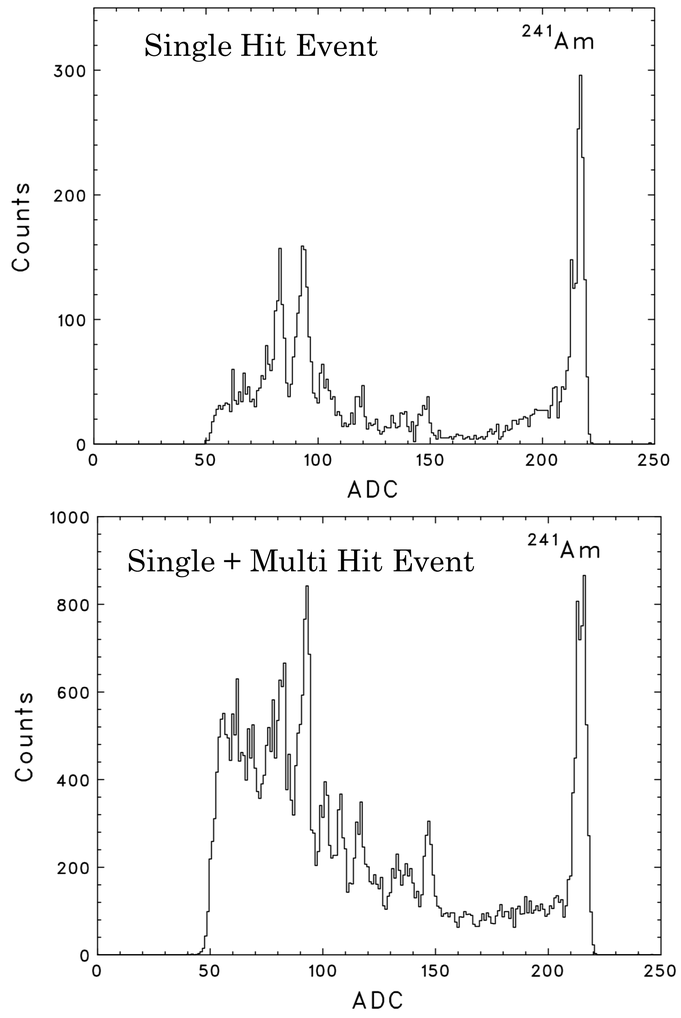


Fig.5 Spectra of ^{241}Am

Spectra Measurement

We measured the energy spectra of gamma-rays emitted by ^{241}Am with a pixel type Schottky CdTe diode (Fig.3) implemented on the TOP01A784. Pixelated Aluminium electrodes and Platinum common electrode are formed on the detector. It operated at −20 ℃. The bias voltage of −200 V was applied to the common electrode.

Fig.5 shows the spectra of ^{241}Am. The upper figure is a spectrum of single hit events. The bottom figure shows that of single and multi hit events. As these figures shows, the lower energy area below 59.5 keV in the bottom figure is contaminated by charge sharing effect between neighbor pixels.

The energy resolution at 59.5 keV is 1.0 keV (FWHM) in the single hit event spectrum.

Conclusion

Based on the collection of analog blocks, we have developed in the series of prototypr ASICs[3], we designed and fabricated 28 by 28 pixel type ASIC whose pixel size is 250 um by 250 um with TSMC 0.35-um process. The ASIC supports both of peak-hold mode and sample-hold mode with a capability of parallel AD conversion. We tested circuit performance and confirmed that its ENC was 50 electrons and its INL was about 1%. A CdTe pixel detector with a pixel size of 250 um by 250 um and a matrix of 28 by 28 pixels was assembled to examine the detector performance as a whole. The spectra measurement of ^{241}Am exhibited a good energy resolution of 1.0 keV (FWHM) at 59.5 keV.

Reference

[1]. Eisen, Y., A. Shor et al. "CdTe and CdZnTe gamma ray detectors for medical and industrial imaging systems.", NIMA 428.1 (1999): 158-170.
[2]. Takahashi, Tadayuki, and Shin Watanabe. "Recent progress in CdTe and CdZnTe detectors." IEEE Transactions on Nuclear Science 48.4 (2001): 950-959.
[3]. Sato, Goro, et al. "Development of low-noise front-end ASIC for hybrid CdTe pixel detectors." IEEE Transactions on Nuclear Science 58.3 (2011): 1370-1375.