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## Development of CdTe Hybrid Pixel ASIC for Hard X-ray Imaging

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Due to its high atomic number, high detection efficiency and good energy resolution, the cadmium telluride (CdTe) semiconductor has been regarded as a promising material for hard X-ray observation. We have developed a front-end ASIC for a CdTe pixel detector for future hard X-ray astronomy missions. The ASIC is designed for a hybrid configuration so that each CdTe pixel can be vertically bump-bonded to a corresponding pixel circuit. It was fabricated with a TSMC 0.35 um process CMOS technology. The total chip size is 8 mm by 8 mm and the pixel area is 7 mm by 7 mm and has a total of 784 channels. The pixel area consists of 28 by 28 identical cells with an area of 250 um by 250 um. The 10-bit Wilkinson ADC is implemented in each column of the pixel matrix and performs parallel AD conversion. The signals are processed and acquired either in the peak-hold or sample-hold mode before being fed into the ADCs which performs the parallel AD conversion. We tested the ASIC circuit performance and measured its Equivalent Noise Charge (ENC) of about 40 electrons, its integral non-linearity of about 1% and its power consumption was about 0.2 mW per pixel. The pixelated CdTe detector was successfully bump-bonded onto the ASIC and the characteristics and measurement results of the CdTe bump-bonded pixel ASIC will be discussed in this presentation.

## Submission declaration

Original and unpublished

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