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IHEP LGAD Sensor Design for ATLAS HGTD

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Introduction

The high-luminosity (HL) Phase-II of the Large Hadron Collider (LHC) at CERN is scheduled to start in 2026. This HL-LHC will deliver an integrated luminosity of up to 4000 fb^{-1} over the subsequent decade. The instantaneous luminosity of the HL-LHC will reach up to 7.5×10^{34} $cm^{-2}s^{-1}$, a large increase from the 2.1×10^{34} $cm^{-2}s^{-1}$ obtained during LHC Run-2. [1] The Low Gain Avalanche Detector (LGAD) structure, [2] plotted in figure 1, is based on the standard PiN diode architecture. n^{++} layer as cathode and p^{++} substrate as anode. The sensor will be biased by negative high voltage on anode.

Keywords: LGAD, sensor design, doping profile, structure optimization, layout mask

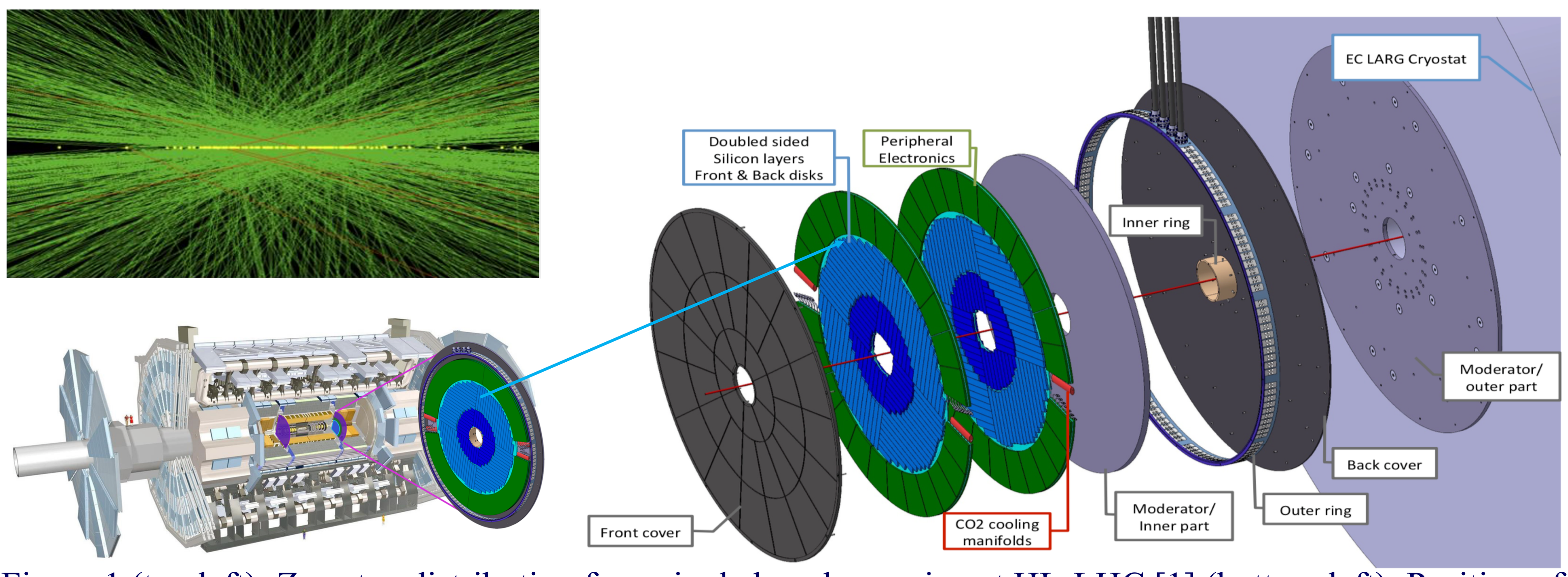


Figure 1 (top left): Z-vertex distribution for a single bunch crossing at HL-LHC.[1] (bottom left): Position of the two vessels for the HGTD within the ATLAS detector. (right): Various components of HGTD.[2]

LGAD Structure

LGAD structure based on n in p-type silicon which is similar to Silicon Photon Multiplier (SiPM) and Avalanche Photon Detectors (APD). **LGAD has a low gain (10~20)** which is different from SiPM (10^5 ~ 10^5) and APD (10^2) in orders.

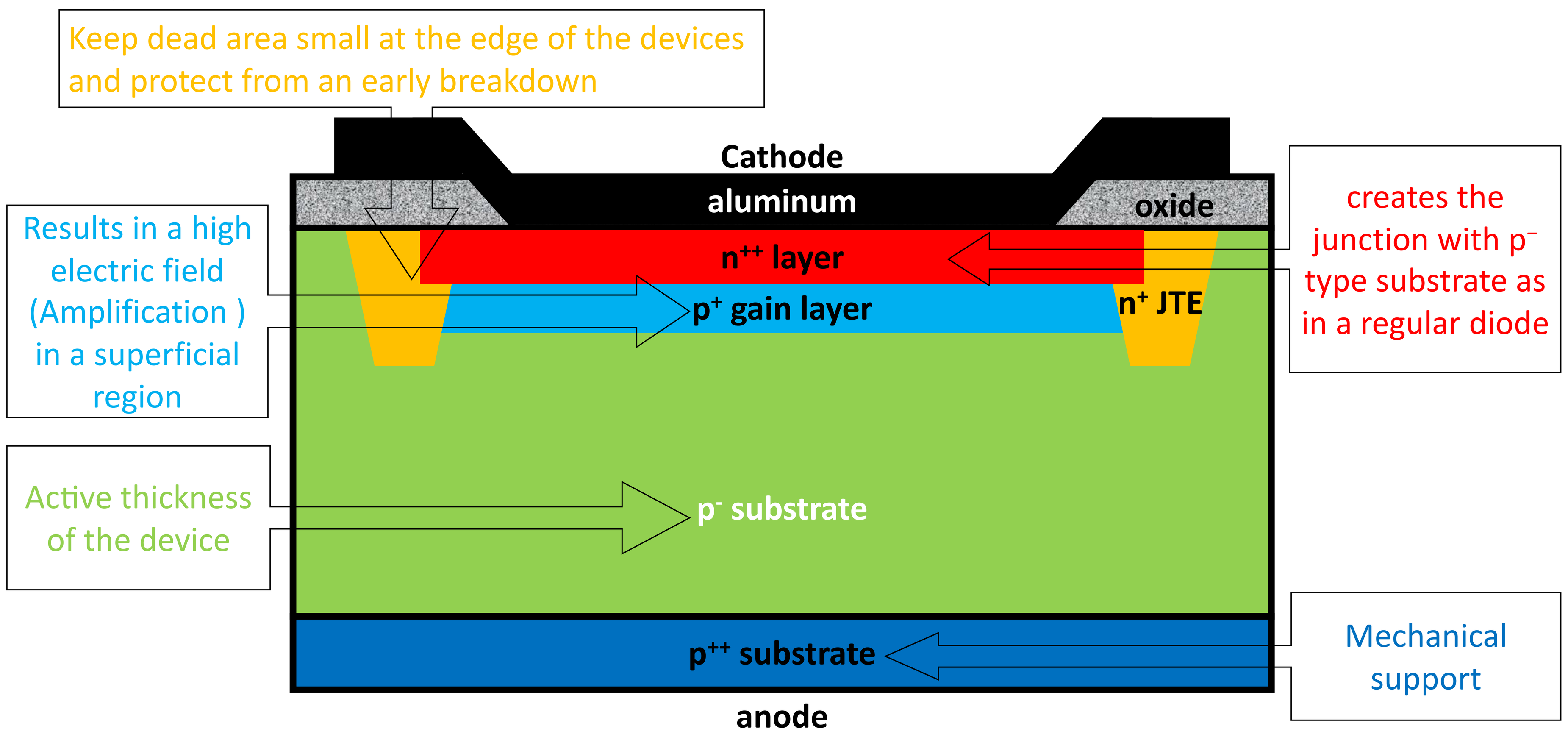


Figure 2: LGAD structure sketch (not to scale).

Structure Optimization

Dead Area and Fill factor From JTE to the edge of each sensor is the dead area figure 3 (left) which is not sensitive to signal but works as protection as well. Simulations had been done for optimizing JTE size, P-stop size and distance between each other. If LGAD sensor pad size was set to be 1.3 mm $\times$ 1.3 mm, which means the larger area JTE to the edge takes the less fill factor sensor has. If the distance between JTE and sensor edge is 20 um, the fill factor is shown as figure 3 (right).

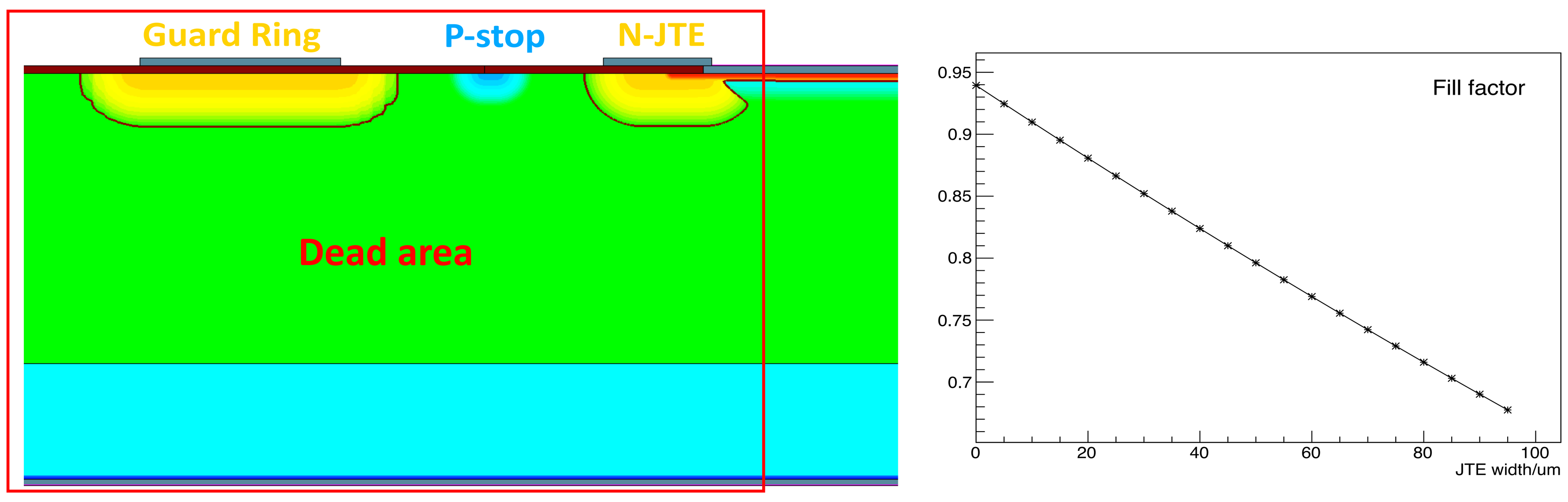


Figure 3 (left): Dead area in LGAD sensor. (right): Fill factor.

Dead Area Optimization Electrical simulations had been done for optimizing JTE size, P-stop size and distance between each other. Figure 4 shows the IV simulation result in different JTE width and JTE p-stop distance.

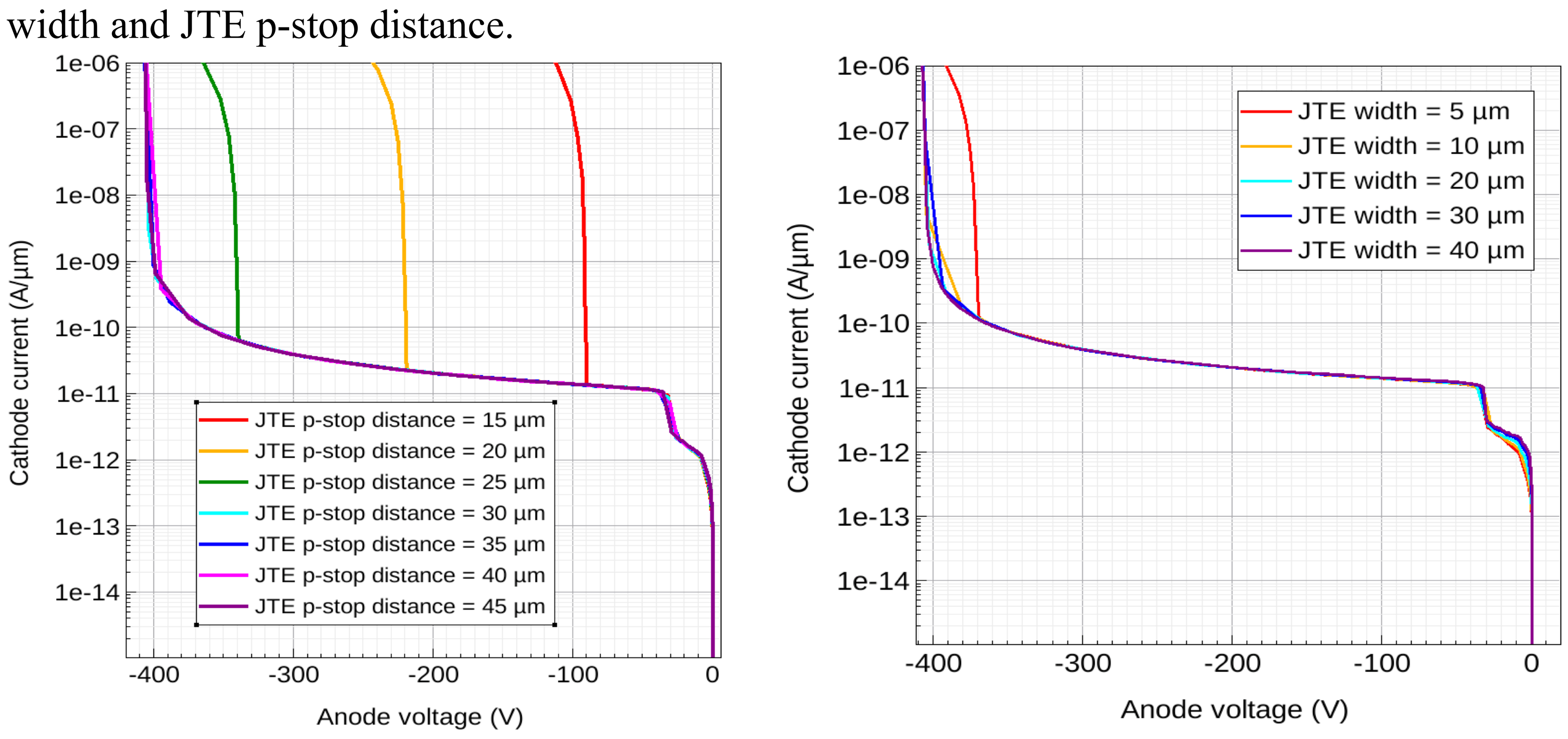


Figure 4 (left): IV simulation in different JTE p-stop distance and JTE width. (right): IV in different JTE width

Doping Profile Optimization

Time resolution vs Gain Three major effects determines the time resolution: time walk, jitter, and "Landau fluctuation". Time walk and jitter depend on the type of readout electronics chosen. Both depend inversely on the signal slope dV / dt:

$$\sigma_{TimeWalk} = \left[\frac{V_{th}}{S/t_{rise}}\right]_{RMS} \propto \left[\frac{N}{dV/dt}\right]_{RMS} \quad \sigma_{Jitter} = \frac{N}{(dV/dt)} \simeq \frac{t_{rise}}{(S/N)}$$

Thin sensors with small signals, fast electronics and a low noise will provide time resolution better than 30 ps.

Gain Layer Doping Optimization

The gain in silicon detectors is achieved by avalanche mechanism that starting in high electric fields ≈ 300 kV/cm. P-type doping concentration needs to be higher than 1×10^{16} cm^{-3}. Doping profile optimizations were mainly done for the active areas including n^{++} and p^{+} layer. Figure 5 (left) shows the n^{++} layer and p^{+} layer doping concentration in different depths. N^{++} layer work as a charge collection electrode which only needs to be highly doped at the shallow region. Most doping optimization work was done for p^{+} gain layer to get special gain.

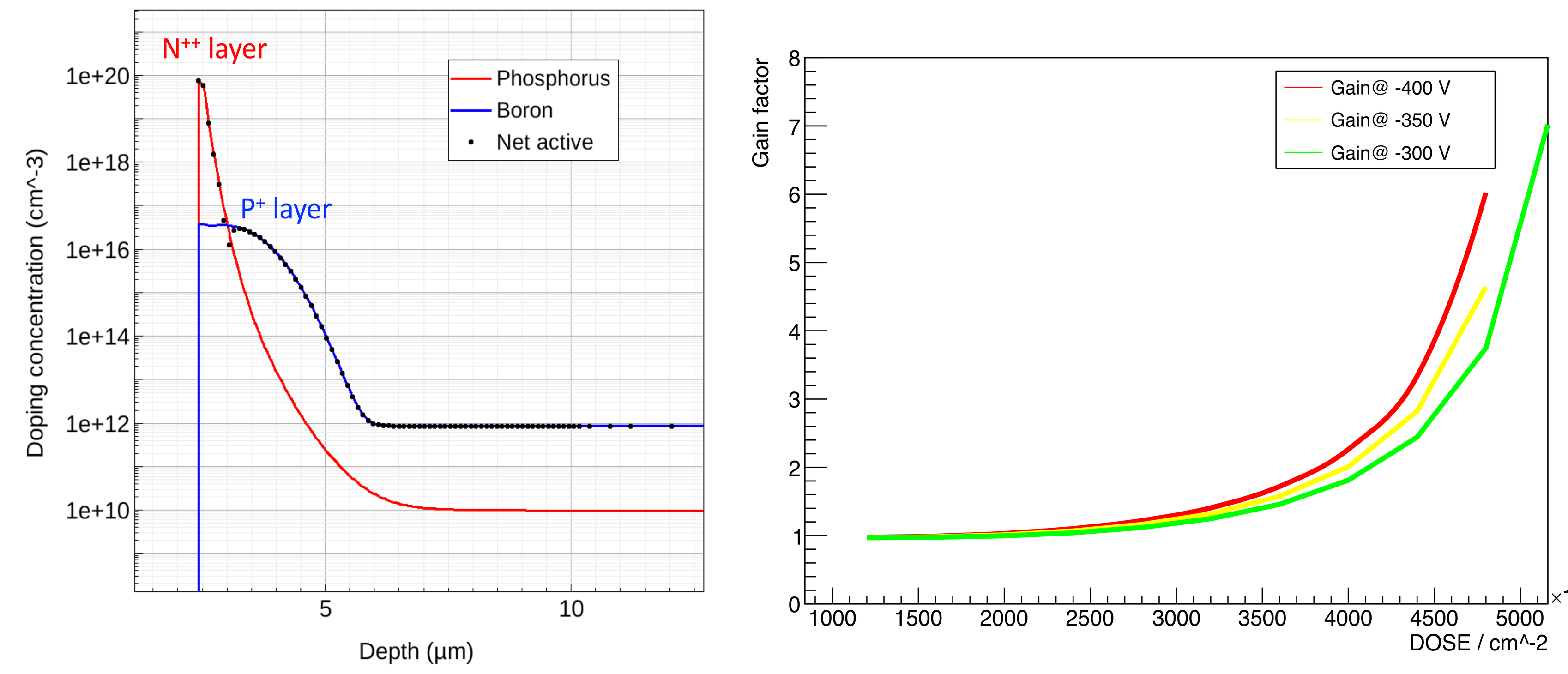


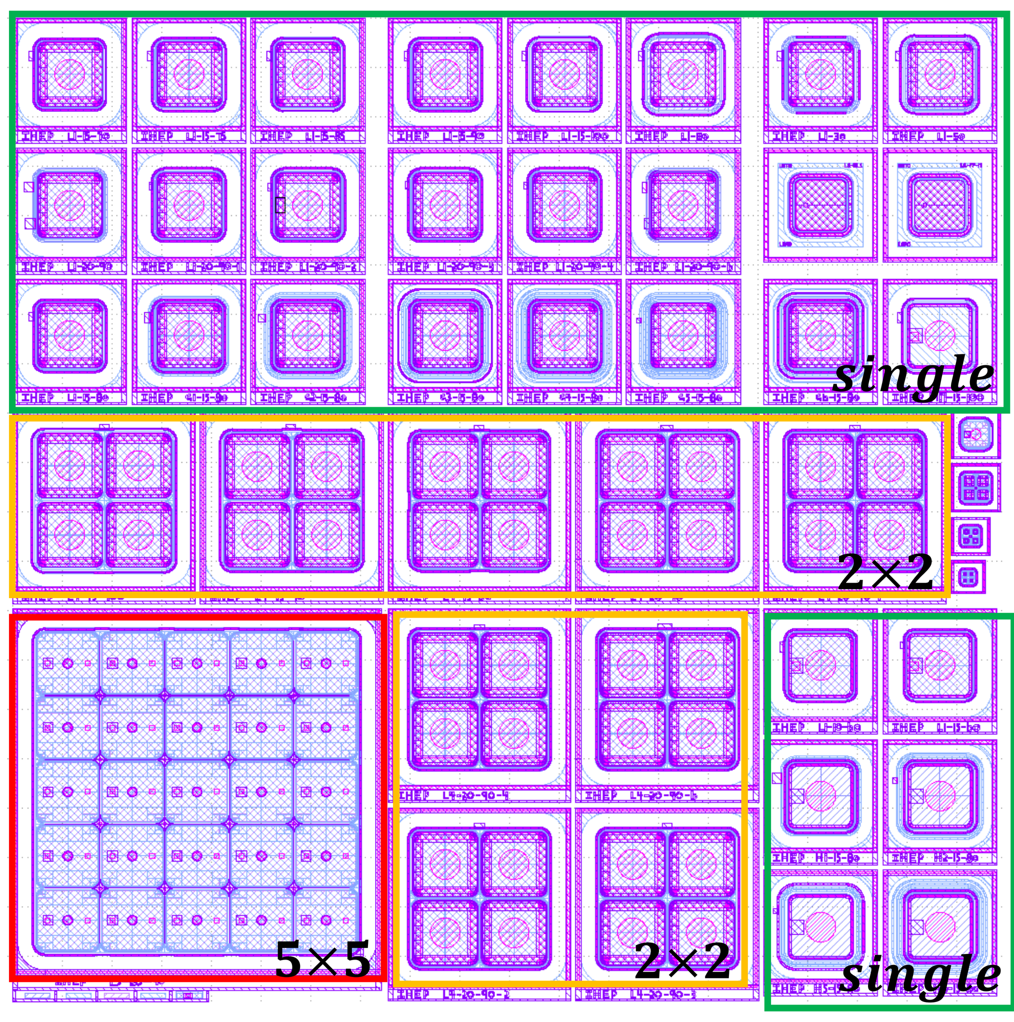
Figure 5 (left): N^{++} layer and p^{+} layer doping concentration in different depth. (right): Gain at different bias anode voltage vs different ion implantation dose.

Gain layer ion implantation process optimization

With maximum injection energy, injection dose dominates sensor electrical characterization mainly on gain factor and breakdown voltage. A highly doped gain layer will win gain factor but suffer early breakdown issue which in turn shrink work voltage area and lose gain. Figure 4 (right) shows the sensor gain factor at -300 V, -350 V and -400 V with different injection doses and indicates a reasonable dose range (4.8 - 5.2×10^{12} cm^{-2}) for the ion implantation fabrication process.

Layout mask

Several different structure designs were included the layout mask shown in figure 6. table 1 shows the details of different designs.



Pixel number	JTE width (μm)	JTE and Pstop distance (μm)	Field plate / guard rings
Single	15	15, 20.5, 23, 25.5, 28, 33	No / same
Single	20	23	5 types / same
Single	15, 20, 30, 50, 80	33	No / same
Single	15	25	5 / -
2×2	15	23, 28, 33	No / same
2×2	20	23	5 / same
5×5	20	23	no

Figure 6: IHEP first version LGAD sensor layout mask. Table 1: LGAD structure in mask.

Summary

This poster presents a new effort by IHEP, in collaboration with Zhonghuan Company, to design suitable LGAD sensors. After TCAD simulation, LGAD sensors designed with gain higher than 6 and breakdown voltage higher than 400 V are being fabricated. Time resolution and radiation performance measurements will soon follow.

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Reference

[1] Hartmut F.-W, 4-Dimensional Tracking with Ultra-Fast Silicon Detectors.
[2] ATLAS Collaboration, Technical Design Report: A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade.
[3] Gabriele Giacomini, Development of a technology for the fabrication of Low-Gain Avalanche Detectors at BNL.