

Development of Front-end ASIC



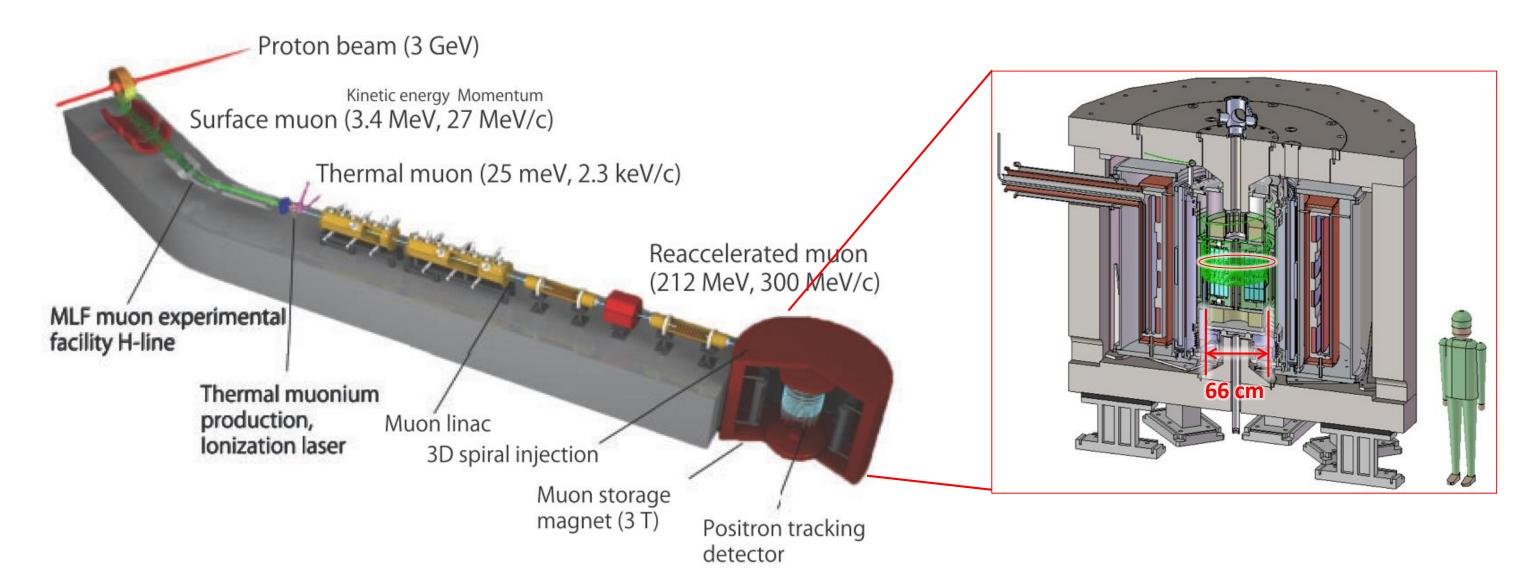
for Silicon-strip Detectors of J-PARC Muon g-2/EDM Experiment

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Abstract

We are developing a front-end ASIC for silicon-strip detectors of the J-PARC muon g-2/EDM (E34) experiment, which aims to measure the muon anomalous magnetic moment (g-2) and electric dipole moment (EDM) to search for new physics beyond the Standard Model. Since the timing of the muon decay is key information in the experiment, the front-end ASIC is required to tolerate a high hit rate of 1.4 MHz per strip and to be stable to the change of hit rate by a factor of 1/150. To accommodate the pulsed muon beam at J-PARC, the ASIC has large buffer memory to save the binary hit information. The prototype ASIC "SliT128B" was fabricated using the Silterra 180-nm CMOS process. We report the performance of SliT128B chip and future prospect.

1. J-PARC muon g-2/EDM experiment



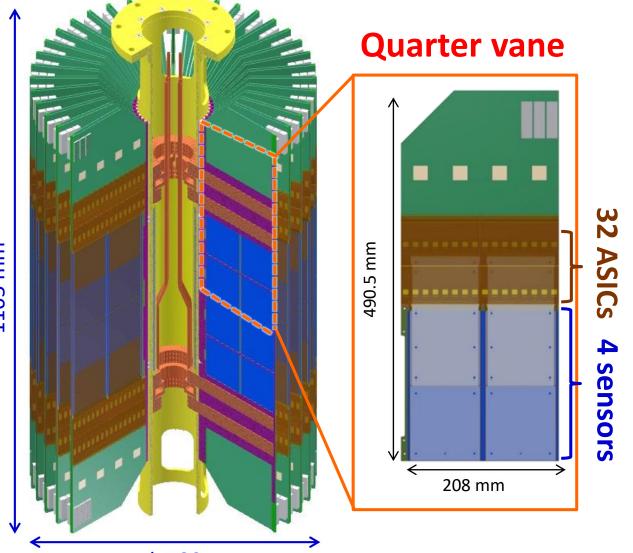
- There is 3.8 σ discrepancy between the measurement of muon g-2 by BNL E821 [1] and the SM prediction.
- J-PARC muon g-2/EDM experiment [2] aims to measure g-2 with a precision of 0.1 ppm and search for EDM with a sensitivity of 10⁻²¹ e · cm with a different method from BNL E821 and Fermilab E989 experiment.
 - Reaccelerated thermal muon beam with no strong focusing
 - MRI-type storage magnet with a good injection efficiency & high uniformity of local B-field
 - Full-tracking detector with large acceptance

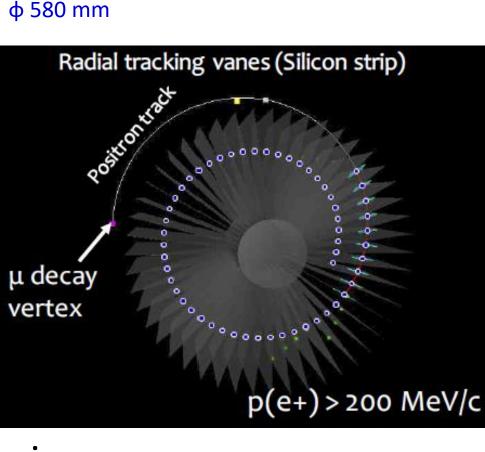
2. Silicon-strip Detector

- Positron tracks from muon decays are measured by silicon-strip detector. It consists of 40 vanes, and one vane consists of 4 quarter-vanes. Each quarter-vane has 4 single-sided silicon strip sensors. Twodimensional position is measured by the two layers of the silicon strip sensors.
 - 640 sensors
 - 5120 ASICs (=655,360 channels)

Requirements to detector

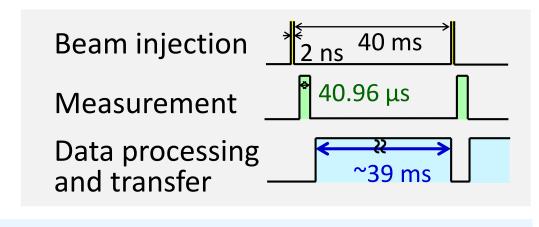
- High tracking efficiency for 100-300 MeV positrons
 - At most 30 muon decays per 5 ns
 - Event rate : 1.4 MHz per strip (max.)
- Stability to hit rate changes
 - Event rate: from 1.4 MHz to 10 kHz per strip.
- Operation in 3T magnetic field and vacuum and no contamination of EM field to the muon storage region.





3. Prototype Front-end ASIC "SliT128B"

- Timing stability is important for the measurement of the muon g-2. → Fast response to tolerate a high hit rate
- Readout sequence is designed for pulsed muon beam at J-PARC.
 - → Binary readout with 5 ns time stump and larger memory buffer, in which the data with a period of 40.96 µs can be stored.



History of development of ASIC "SliT"

- (16ch, analog) - 2012 **SlitA** : 1st prototype [4].
- : the pulse width was improved [5]. - 2013 **SlitA2013** (64ch, analog) (UMC CMOS 250-nm → Silterra CMOS 180-nm)
- (128ch, analog+digital): full-scale prototype with analog and digital part [6]. - 2015 **SliT128A**
- : time-walk was improved by differentiator [7]. - 2017 **SliT2017TEG** (64ch, analog)
- 2018 **SliT128B** (128ch, analog+digital): ← report in this poster

Slow control **Analog part** DAC DAC Digital part Serial output Comparator **Comparator**

Peaking time < 50 ns

Requirements to ASIC

- Pulse width < 100 ns
- Dynamic range > 4 MIP (1 MIP = 24,000e)
- Noise : ENC < 1600 e
- $@C_{det} = 30 pF$

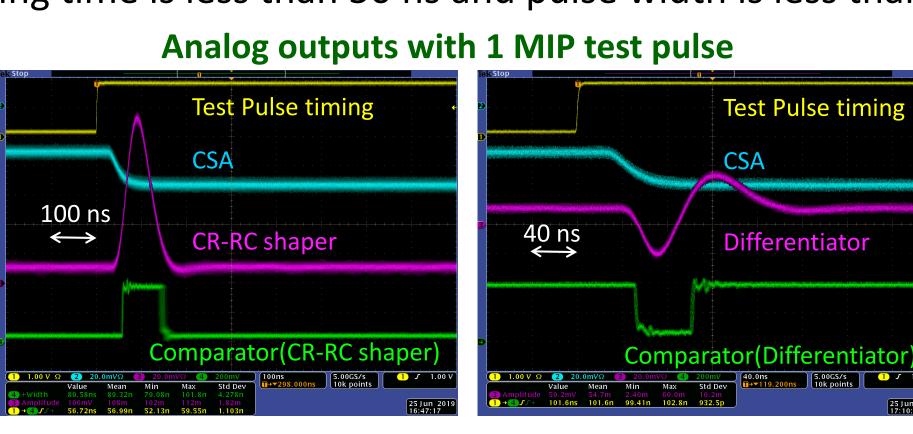
Photo of SliT128B and its evaluation board

- Time walk < 1 ns
- Power consumption : 5 mW/ch

4. Performance Test

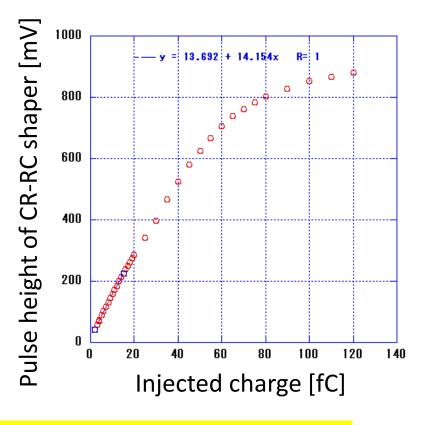
Peaking time and pulse width

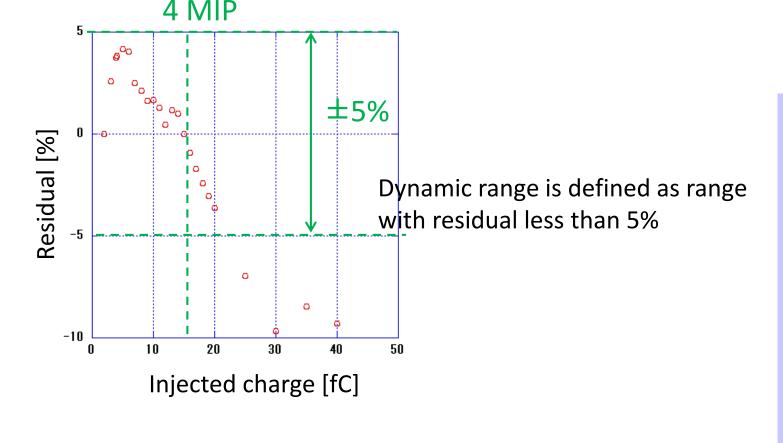
- Analog outputs from CSA, CR-RC shaper, differentiator, and their comparators are observed through monitor lines.
- Peaking time is less than 50 ns and pulse width is less than 100 ns.



Dynamic Range

 Dynamic range is derived to be more than 5 MIP from the pulse height of CR-RC-shaper as a function of injected charge. (•)





Power consumption

 Power consumption is estimated to be 0.44 W, which is less than the requirement (< 0.64W/chip).

al., "A new approach for measuring the muon anomalous magnetic moment and electric dipole moment", PTEP 2019, 053C02 (2019)

[1] G.W. Bennett et al, "Final report of the E821 muon anomalous magnetic moment measurement at BNL", PRD 73, 072003 (2006)

[3] T. Aoyagi et al., "Development of a silicon strip detector with high rate capability for pulsed beams", arXiv:1910.13087, submitted to JINST

Noise

"S-curve scan" is performed to estimate the noise.

A full-scale prototype ASIC "SliT128B" was

• SliT128B was mounted on an evaluation

aluminum wire. The evaluation board was

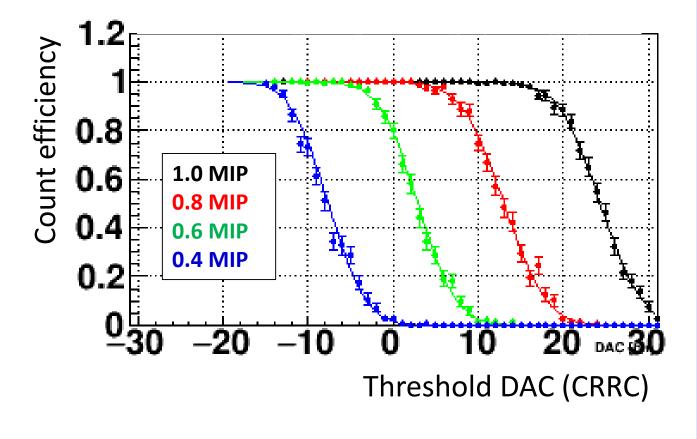
connected with commercial FPGA board

(Nexys video) through FMC connector.

board by wire-bonding with 25-µm

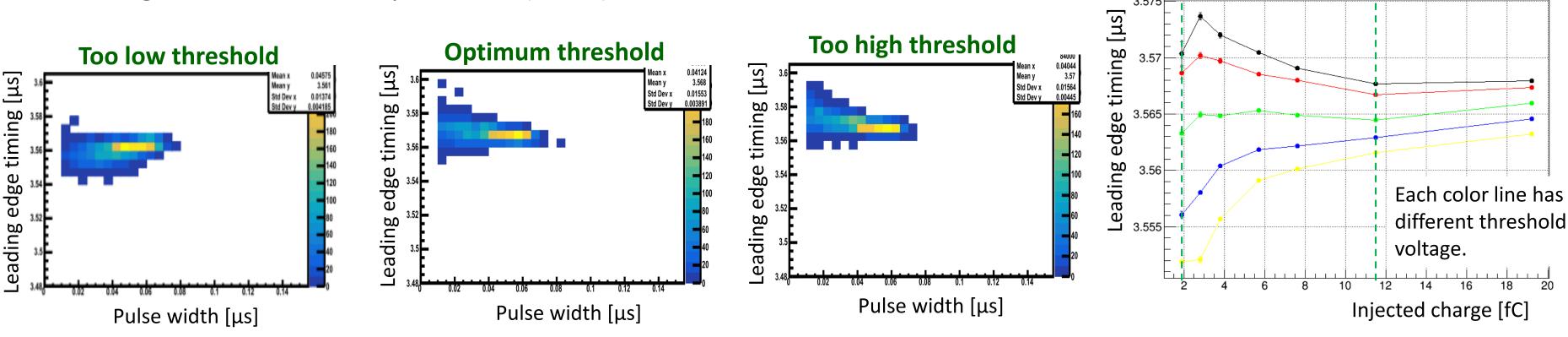
designed and fabricated.

- A fixed amount of charge is injected, changing the threshold voltage of comparator. Response function is error function, which is step function smeared by noise.
- Noise is estimated to be 1746 \pm 57 electrons with a detector capacitance of 33 pF.



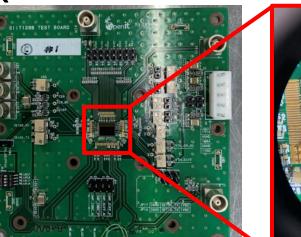
Time-walk

- Time-walk effect is reduced by adjusting the threshold voltage for differential circuit.
- \bullet Time-walk is about 2 ns between 0.5 MIP and 3.0 MIP with the optimum threshold voltage. It gets close to the requirement (<1 ns). 3 MIP



5. Summary and Prospect

- We are developing Front-end ASIC "SliT" for J-PARC muon g-2/EDM experiment.
- Prototype ASIC "SliT128B" has been fabricated and we confirmed most of the requirements are met. A little more improvement especially about time-walk will be done by minor optimization of the circuit design.
- Based on the result of SliT128B, we designed and fabricated next version of the ASIC "SliT128C". The performance test of SliT128C is starting.
- The production version of the ASIC will be fabricated next JFY.



SliT128C