DEPLETED MONOLITHIC ACTIVE PIXEL SENSORS IN 180 NM TOWERJAZZ AND 150 NM LFOUNDRY TECHNOLOGY


A COLLABORATION EFFORT OF UNIVERSITY OF BONN, CERN (GENEVA), CPPM (MARSEILLE) & IRFU (SACLAY)
- Combine sensor and readout on same wafer using commercial CMOS technologies
- Charge collection mainly by diffusion in epi-layer (typically low-resistivity)
  - Too slow and not-radiation hard for high radiation and high rate experiments like ATLAS ITk
- Need depleted sensor volume for fast charge collection and large signal → DMAPS
- Depletion depth $d \propto \sqrt{\rho V_{\text{bias}}}$
- High resistive substrate material ($\rho = 100 \, \Omega \cdot \text{cm} - \text{k}\Omega \cdot \text{cm}$)
- High voltage add-ons ($50 - 200 \, V_{\text{bias}}$)
- Multiple nested wells for full CMOS
- Backside processing (thinning)
- Fully depleted high-resistive bulk or epitaxial layer as charge sensitive volume
CMOS TECHNOLOGY

- Commercial processes with high resistive wafers available
  - Large production capabilities
  - Low cost per wafer
  - Fast turn around time
- Monolithic designs achievable
- Low module cost
- Thin modules
- Small pixel sizes (50 x 50 µm² or smaller)
- Crucial question: radiation hardness and fast charge collection possible?

For example:

16.12.2019  
bespin@physik.uni-bonn.de - HSTD12 2019
**DEPLETED MONOLITHIC ACTIVE PIXELS**

- Large collection electrode
  - Electronics inside charge collection well
  - Uniform field across pixel volume
  - Short(er) drift distances
    → radiation hard
  - Large(r) sensor capacitance
    → higher noise at given power

- Small collection electrode
  - Charge collection well separated from electronics
  - Longer drift distances & low field regions
    → radiation hard?
  - Small sensor capacitance
    → low noise and power (at given SNR)
**DEVELOPMENT LINES**

- **CCPD_LF**
  - Subm. Sep. 2014
  - Fast R/O coupled to FE-I4

- **ALICE ALPIDE**
  - Subm. 2016
  - 8 x 8 pixel submatrices

- **INVESTIGATOR**
  - Subm. 2016
  - 8 x 8 pixel submatrices

- **MALTA**
  - Subm. 2018, large matrices
  - Fast asynchr & col. drain R/O

- **MINI-MALTA**
  - Subm. Spring 2020
  - Full size 2x2 cm²
  - Improved sensor and front end

- **LF-CPIX (DEMO)**
  - Fast R/O coupled to FE-I4

- **LF-MONOPIX1**
  - Fast column drain R/O

- **LF-MONOPIX2**
  - Subm. Spring 2020
  - Full height chip

- **ALICE ALPIDE**
  - Subm. 2016
  - 8 x 8 pixel submatrices

- **TJ-MONOPIX2**
  - Subm. Spring 2020
  - Full size 2x2 cm²
  - Improved sensor and front end

- **MALTA (asynchronous) & TJ-MONOPIX (column drain)**
  - - Subm. 2018, large matrices
  - - Fast asynchr & col. drain R/O

- **MINI-MALTA**
  - Subm. Spring 2020
  - Full size 2x2 cm²
  - Improved sensor and front end
LF-MONOPIX AND TJ-MONOPIX

- Fully monolithic DMAPS prototype chips
- Complete digital logic inside the pixels
- FE-I3 like column-drain readout architecture that can cope with ATLAS ITk outer layer hit rate
LARGE COLLECTION ELECTRODE DESIGN:
LF-MONOPIX
- Large collection electrode design in LFoundry 150 nm CMOS technology
- High-resistive substrate (> 2 kΩcm)
- 250 x 50 µm² pixel size (129 rows / 36 columns), nine flavors
- Gain (unirradiated) between 10 and 12 µV / e⁻
- Noise (ENC) 180 – 240 e⁻, dispersion 30 – 70 e⁻
- Typical signal up to 25 ke⁻ and tuned threshold ca. 1400 e⁻ (dispersion 400 e⁻)
- No loss of gain and up to 150 e⁻ noise increase after irradiation to $10^{15}$ neq cm⁻²
Unirradiated: 99.6 % (200 V)

Neutron irradiated $10^{15}$ neq cm$^{-2}$: 98.9 % (130 V)

- 1700 e$^-$ threshold (not minimum achievable for unirradiated chip)
- High and homogeneous efficiency at 200 V bias voltage before irradiation

- Small loss of efficiency (1.8 \%) between pixels after irradiation due to a reduced signal shared between adjacent pixels
- Gain variation < 3 % for all tested flavours

- Noise increase of 15 % for CMOS flavors, 25 % for NMOS flavors due to leakage and changing of CSA bias condition, nominally ENC_{NMOS} < ENC_{CMOS}

- Irradiation without annealing before measurements
- Gain variation < 3 % for all tested flavours
- Noise increase of 15 % for CMOS flavors, 25 % for NMOS flavors due to leakage and changing of CSA bias condition, nominally ENC_{NMOS} < ENC_{CMOS}
- Irradiation without annealing before measurements
SMALL COLLECTION ELECTRODE DESIGN:
TJ-MONOPIX
- Small collection electrode design in 180 nm TowerJazz technology
- Low power consumption (≈ 120 mW/cm²)
- Modified process with additional n-layer for full depletion
- 36 µm x 40 µm pixel size arranged as 448 x 224 pixels in four flavors
## TJ-MONOPIX: THRESHOLD & NOISE

<table>
<thead>
<tr>
<th></th>
<th>Unirradiated Sample</th>
<th>Irradiated sample ((10^{15} \text{ neq cm}^{-2}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold</td>
<td>350 e(^{-})</td>
<td>570 e(^{-})</td>
</tr>
<tr>
<td>Threshold dispersion</td>
<td>34 e(^{-})</td>
<td>66 e(^{-})</td>
</tr>
<tr>
<td>ENC</td>
<td>17 e(^{-})</td>
<td>23 e(^{-})</td>
</tr>
</tbody>
</table>

### Threshold (RDPW)

![Threshold (RDPW) graph](image)

### ENC (RDPW)

![ENC (RDPW) graph](image)
- Testbeam measurement in 2.5 GeV electron beam in Bonn (ELSA)

Unirradiated: 97%

Irradiated \((10^{15} \text{ neq cm}^{-2})\): 69%
- High resolution in-pixel efficiency from MALTA chip

- Modification of sensor geometry (gap & additional p-well) show improved charge collection in pixel corners (homogenous)

Unirradiated (W6R6, S4)

Decreasing threshold, from ~600 e- to ~250(unir)/350( irr) e-

Irradiated 5x10^{14} n_{eq}/cm^2 (W6R21, S4)

Couldn't reach lower threshold

- Irradiated to 10^{15} neq cm^{-2}
- Homogenous efficiency of 97.9%

More on MALTA in previous talk (# 196) and poster session (# 343)

M. Dyndal et al., arXiv:1909.11987
- Irradiation without annealing before measurements
- Due to technical limitation HV diode reset flavor only up to 1 MRad

**PMOS RESET FLAVOR**

![Graph showing PMOS reset flavor response to dose and iron exposure](image)

**HV DIODE RESET FLAVOR**

![Graph showing HV diode reset flavor response to dose and iron exposure](image)
FUTURE MONOPIX DESIGNS
**LF-MONOPIX2**
- Chip size increased to $2 \times 1 \text{ cm}^2$
- Smaller pixels: $50 \times 150 \mu\text{m}^2$
- Larger matrix: $340 \times 56$ px
- Analog FE improvement
- Pixel layout improvement

**TJ-MONOPIX2**
- Full size chip of $2 \times 2 \text{ cm}^2$
- Pixel size: $33.04 \times 33.04 \mu\text{m}^2$
- Larger matrix: $512 \times 512$ px
- Analog FE improvement and threshold tuning
- Downstream data processing, e.g. data buffering and triggering
- Diode reset for good TID performance
- Sensor improvements for better NIEL and TID performance → see talk of H. Pernegger

Submission for both chips in spring 2020
CONCLUSION

- Promising results for monolithic active CMOS sensors in both large and small electrode design
- Fully functional fast read-out architecture in both chips
- Large collection electrode design radiation hard up to \(10^{15}\) neq cm\(^{-2}\) NIEL and 100 MRad TID damage
- Issues for low efficiency after neutron irradiation in small electrode design identified and solved (talk by H. Pernegger and poster from L. Flores)
- Modifications on front-end in small electrode design for better TID performance (talk by H. Pernegger)
- Full size prototypes in both technologies currently under development