

## Evaluation the first SOI pixel detector with 3D integration technology.

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In HSTD11, we reported a SOI pixel sensor, SOFIST Ver.4, for the International Linear collider using 3D integration technology. In SOFIST4, we had integrated preamplifier, comparator and 3-stage charge and timestamp memories all within  $20 \mu\text{m} \times 20 \mu\text{m}$  pixel area. This chip would satisfy the requirements for the linear collider vertex detector: the low hit occupancy, low material budget and high spatial resolution.

To integrate the complex functions within the small pixel area, a 3D integration technology was adopted. The functions, and the sensor were separated to two silicon chips. The lower chip consists of the pixel sensor, preamplifier and the comparator while the upper chip houses the logic circuits and analog memories. *Micro gold bumps* were produced on both the chips using photolithography method to combine both the chips. The analog and comparator outputs from the lower chip are connected to the upper chip in each pixel. The chip size can be thinned out to  $50 \mu\text{m}$  after the 3D integration.

In 2019, the first prototype was delivered and its intense evaluation is in progress.

In this presentation, we will review the 3D integration technology, SOFIST4 chip concept and results from the ongoing evaluation.

### Submission declaration

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**Author:** TSUBOYAMA, Toru (KEK, High Energy Accelerator Research Organization)

**Co-authors:** ISHIKAWA, Akimasa (Tohoku University (JP)); KURACHI, Ikuo (High Energy Accelerator Research Organization); HARA, Kazuhiko (University of Tsukuba (JP)); YANAGIMURA, Koki (Tohoku-MicroTec Co., Ltd (T-Micro)); MOTOYOSHI, Makoto (Tohoku-MicroTec Co., Ltd (T-Micro)); TOGAWA, Manabu (High Energy Accelerator Research Organization (JP)); IKEBE, Masayuki (Hokkaido University); YAMADA, Miho (TM-CIT); ONO, Shun (KEK); TAKAYANAGI, Takehiro (KEK); MIYOSHI, Toshinobu (KEK); ARAI, Yasuo (High Energy Accelerator Research Organization (JP)); IKEGAMI, Yoichi (High Energy Accelerator Research Organization (JP))

**Presenter:** TSUBOYAMA, Toru (KEK)

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