Data-acquisition system developments for ATLAS pixel QA/QC test toward High Luminosity LHC

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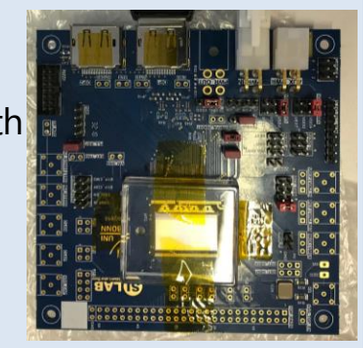
<introduction>

- The whole ATLAS inner tracker will be replaced by new silicon tracker, toward High Luminosity LHC (HL-LHC). The innermost layer is covered by silicon pixel detectors.
- DAQ system for QA & QC test have been developed (the YARR system)
- In HL-LHC, large parts of ALTAS DAQ system infrastructure for operation is going to be shared among all sub detectors. (FELIX system)
- In order to minimize the differences between the DAQ system for operation and QA & QC test, prototype FELIX system is introduced into DAQ path of YARR system.

<RD53A>

- The prototype of readout chip [1]
- Pixel size: 50 × 50 μm
- Channel: 192 × 400
- Output: up to 1.28 Gbps × 4 lanes with Aurora 64/66 Protocol

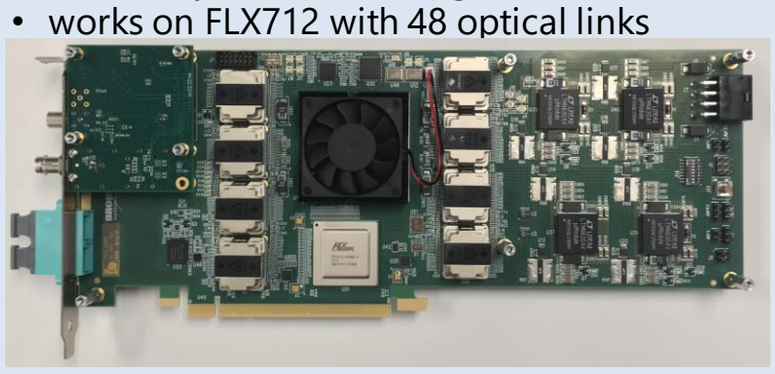


<YARR>

- Readout system for serval types of readout chips [2]
- Not only data analysis but also data processing and histogramming are performed on software, to keep flexibility and low latency

<FELIX>

- Infrastructure for ATLAS DAQ system for operation [3]
- The same system is going to be used for all sub detectors
  - Easy to support/upgrade
- works on FLX712 with 48 optical links



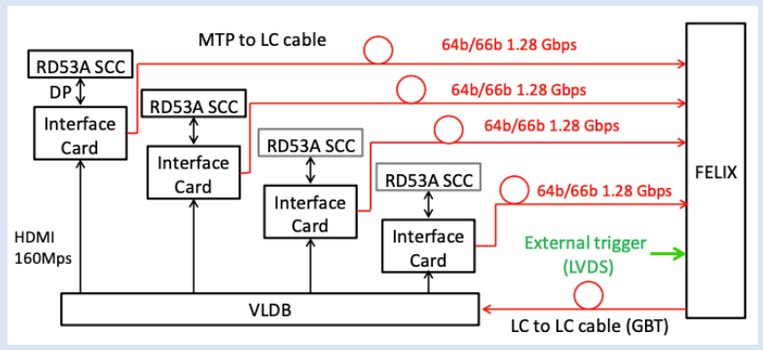
- Scaled down system with 4 optical links is also available with VC709

- Uplink: GBT protocol
- Downlink: GBT (4.8 Gbps) or Full mode (9.6 Gbps) protocol

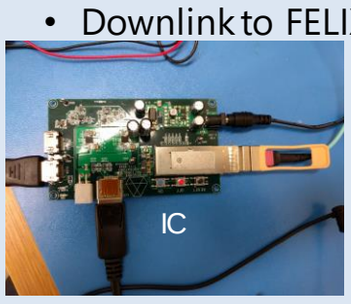
- Test of the setup has been done with VC709

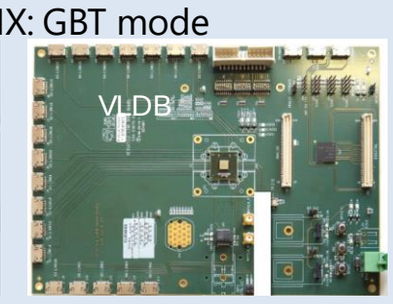
<YARR + FELIX readout chain>

- Two approaches:
- **PiLUP**
  - All protocol conversion between YARR and FELIX is done on PiLUP board
  - Downlink from RD53A: 160 Mbps × 4 lanes
  - **FELIX FW works without modification**
  - Downlink to FELIX: **Full mode**



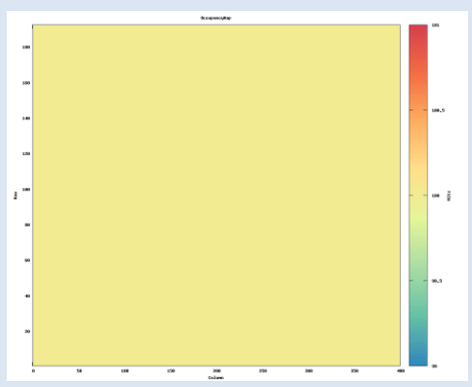
- **Versatile Link Demo Board + Interface Card**
  - VLDB: distributes command to ICs
  - IC: convert RD53A output only from electrical to optical
  - **Downlink from RD53A: 1.28 Gbps × 1 lane**
  - Aurora protocol to Full mode protocol converter has been added on FELIX FW
  - Downlink to FELIX: GBT mode



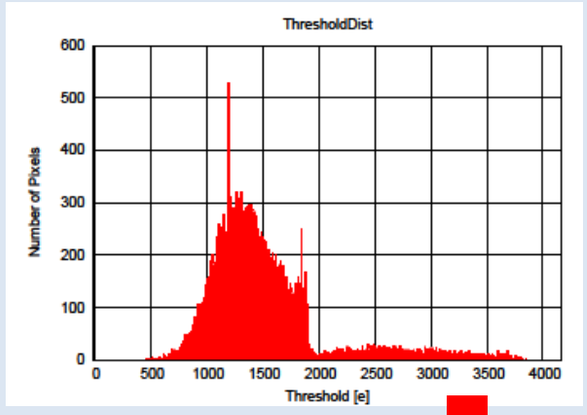


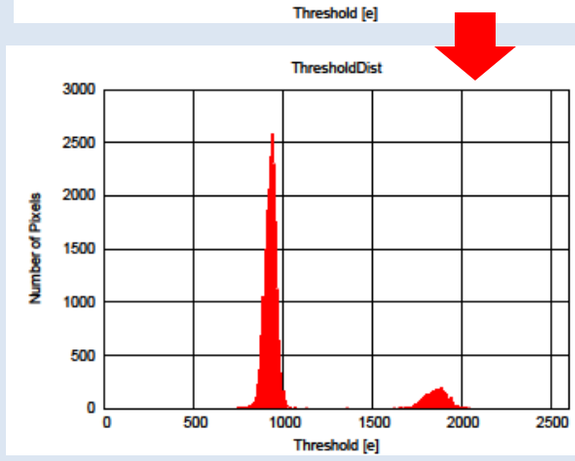
<Comunication>

- succeeded to communicate with RD53A



- **100% response is obtained with digital scan**

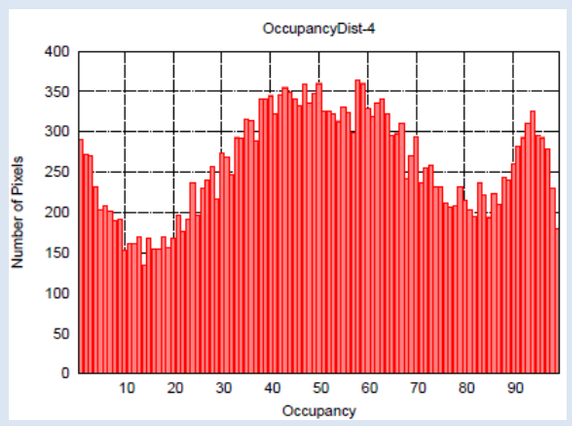




<basic tuning>

- **Basic tunings (analog, digital, threshold,…) have been operated**

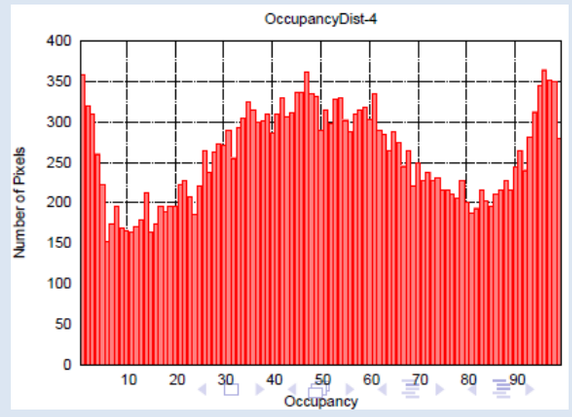
- Threshold distributions before & after tuning of threshold with **PiLUP setup**



<Multiple chip readout>

- **Simultaneous communication with Multiple chip has been succeeded**

- Occupancy distributions after tuning taken simultaneously with **VLDB + IC setup**



<References>
[1] RD53 Collaboration, The RD53A Integrated Circuit, CERN-RD-PUB-17-001
[2] Timon Heim, YARR - A PCIe based Readout Concept for Current and Future ATLAS Pixel Modules, J. Phys.: Conf. Ser. 898 032053 (2017).
[3] J. Anderson and K. Bauer et al., FELIX: a PCIe based high-throughput approach for interfacing front-end and trigger electronics in the ATLAS Upgrade framework, Journal of Instrumentation, vol. 11, pp. C12023,2016, 1748-0221-11-12-C12023.

ATLAS EXPERIMENT