Data-acquisition system developments for ATLAS pixel QA/QC test toward High Luminosity LHC
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<Introduction>
- The whole ATLAS inner tracker will be replaced by new silicon tracker, toward High Luminosity LHC (HL-LHC). The innermost layer is covered by silicon pixel detectors.
- DAQ system for QA & QC test have been developed (the YARR system)
- In HL-LHC, large parts of ATLAS DAQ system infrastructure for operation is going to be shared among all sub detectors. (FELIX system)
- In order to minimize the differences between the DAQ system for operation and QA & QC test, prototype FELIX system is introduced into DAQ path of YARR system.

<RD53A>
- The prototype of readout chip [1]
- Pixel size: 50 × 50 μm
- Channel: 192 × 400
- Output: up to 1.28 Gbps × 4 lanes with Aurora 64/66 Protocol

<YARR>
- Readout system for several types of readout chips [2]
- Not only data analysis but also data processing and histogramming are performed on software, to keep flexibility and low latency

<Comunication>
- succeeded to communicate with RD53A
- 100% response is obtained with digital scan

<YARR + FELIX readout chain>
- Two approaches:
  - PILOP
    - All protocol conversion between YARR and FELIX is done on PILOP board
    - Downlink from RD53A: 160 Mbps × 4 lanes
    - FELIX FW works without modification
    - Downlink to FELIX: Full mode
  - Versatile Link Demo Board + Interface Card
    - VLDB: distributes command to ICs
    - IC: convert RD53A output only from electrical to optical
    - Downlink from RD53A: 1.28 Gbps × 1 lane
    - Aurora protocol to Full mode protocol converter has been added on FELIX FW
    - Downlink to FELIX: GBT mode

<basic tuning>
- Basic tunings (analog, digital, threshold, ...) have been operated
- Threshold distributions before & after tuning of threshold with PILOP setup

<Multiple chip readout>
- Simultaneous communication with Multiple chip has been succeeded
- Occupancy distributions after tuning taken simultaneously with VLDB + IC setup

<References>

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