Karlsruhe Institute of Technology

Bundesministerium für Bildung und Forschung

KIT ASIC and Detector Laboratory

ATLASPix3 – a reticle size HVCMOS pixel sensor designed for construction of multi chip modules

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Apr.2019 **Submission** ATLASPix3 TSI 180 nm

Aug.2019 **Shipping** ATLASPix3

Aug.2019 **Start of Tests** CW 35

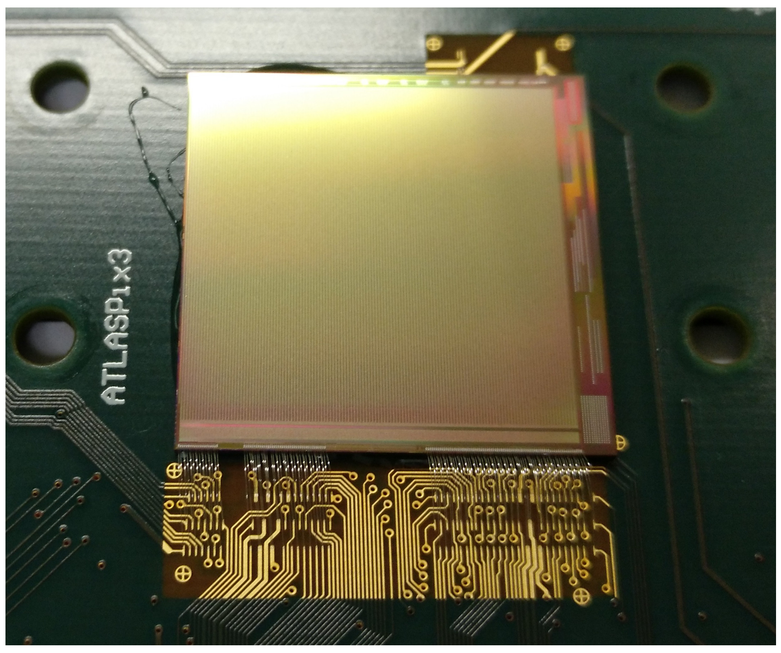
Nov.2019 **Start of Telescope System Development** CW 46

Dec.2019 **Start of Telescope Commissioning** CW 49

Dec.2019 **Beam Test with Telescope** CW 50

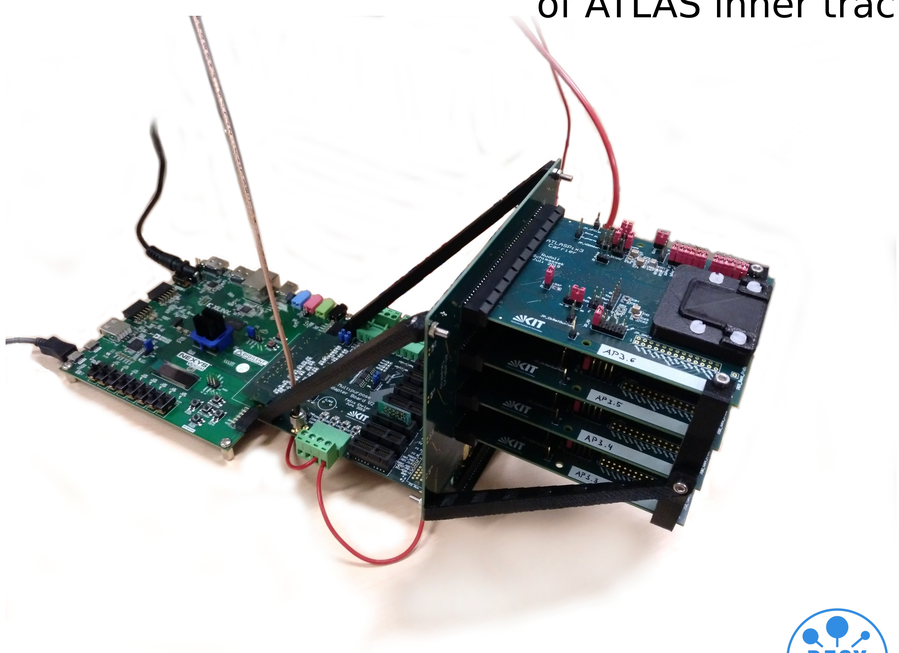
Jan.2020 **Further Tests and Irradiation Studies** CW 2 ...

2019 2020



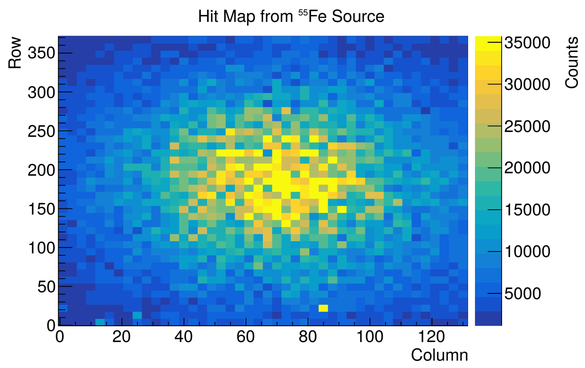
The ATLASPix3 Chip

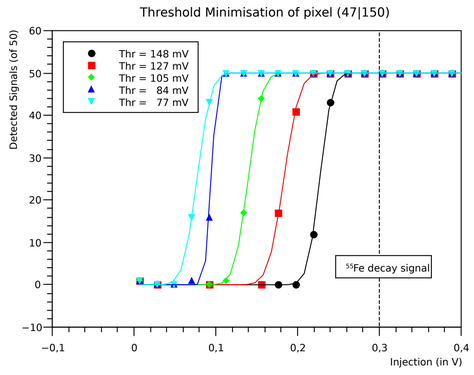
- Chip Size: 20.2 x 20 mm²
- Matrix Size: 132 x 372 pixel
- Pixel Size 150 x 50 µm²
- produced in 180 nm HV-CMOS process
- triggered and untriggered readout
- radiation hard design
- RD53 compatible with a one input and one output line
- capable of hit rates expected for Layer 4 of ATLAS inner tracker at HL-LHC

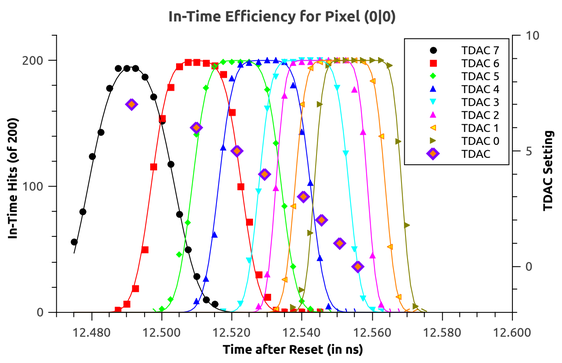


Lab Measurements

- Good Yield: 5 of 6 tested chips fully functional
- no dead or noisy pixels on tested samples
- small detection thresholds achievable
- timing correction possible using per pixel tuning DACs

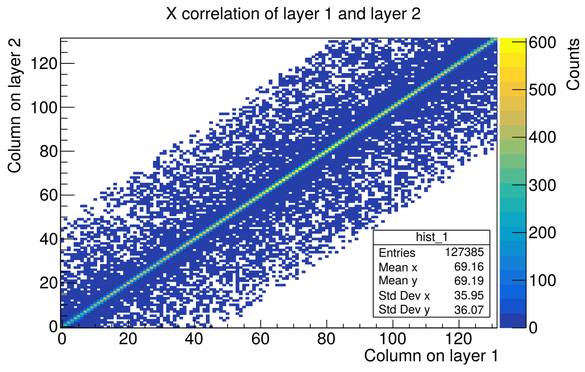


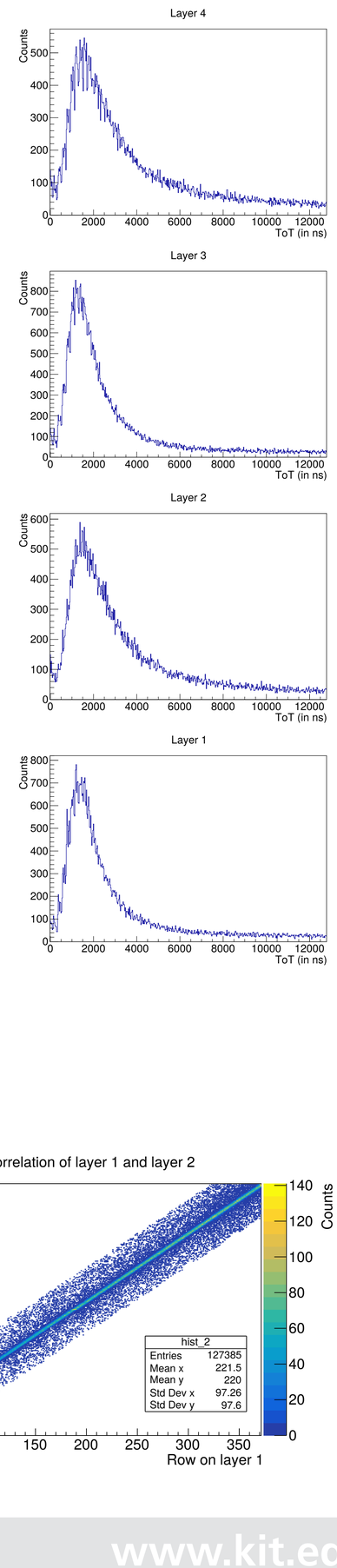




Beam Test Measurements

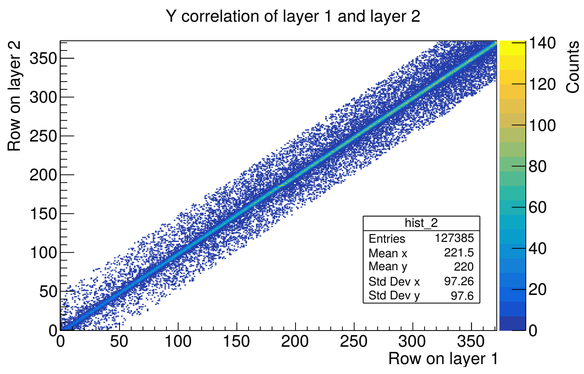
- telescope with four ATLASPix3 layers built and used in beam test
- Time over Threshold (ToT) measurement is working for all samples
- correlation visible between planes





Conclusions

- full reticle sized chip was submitted in April 2019
- Radiation hard design made for ATLAS ITk Layer 4 environment
- The chip is working and has a high yield
- 4-layer ATLASPix3 beam telesope has been developed and is operational
- Good Timing from design and corrections with ToT (offline) and Tuning DACs (online)



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