Performance Test of a Pixelated Silicon Sensor with Junction Field Effect Transistor

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In the previous Hiroshima symposium (HSTD11), we presented a detection concept of a pixelated silicon sensor integrated with junction field effect transistor (JFET), fabrication process flow charts of it, and simulation studies based on this detector concept. The JFET is designed to have the cylindrical structure and is used as a switch to readout charges accumulated in the pixelated sensor. We determine detector design parameters such as a distance between the source and the drain, a coverage region of the deep p-well implemented underneath the drain of the JFET, and doping concentration for the deep p-well. All pixels with one row are read in parallel and the next row is then selected by the gate voltage after finishing the reading one row. The photon detection efficiency of the silicon at low energy X-ray is very high so that this detection can be used for direct irradiation method, and the thickness of the active silicon should be twice of the absorption length of the silicon at that energy. We fabricate a pixelated silicon sensor integrated with JFET using a 650 μm-thick, high resistivity (> 5 kΩ ·cm) n-type and double-sided polished 6-in silicon wafer. In this poster we present electrical characteristics of the fabricated sensors and the drain currents as a function of the drain voltage for different the gate voltages. We also present the optimized design parameters of the prototype sensor to demonstrate the proper functioning of the switch.

Introduction

- Junction Field Effect Transistor (JFET)

- JFET is the simplest type of field effect transistors.
- Switches are electronically controlled in the pixelated silicon detector.
- By applying a reverse bias voltage to a gate, the channel is pinched, so that the current is switched off.
- JFET is on when there is no potential difference between its gate and source terminals.
- Electric charges flow through a N-channel between source and drain terminals.

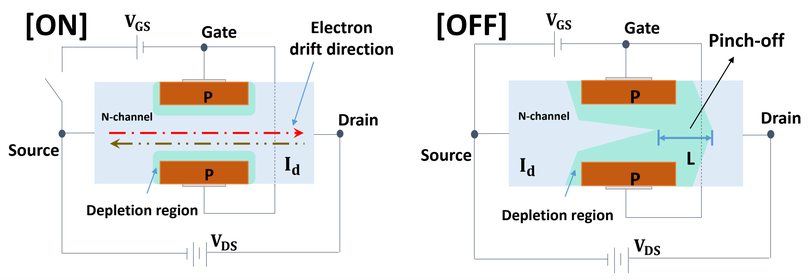
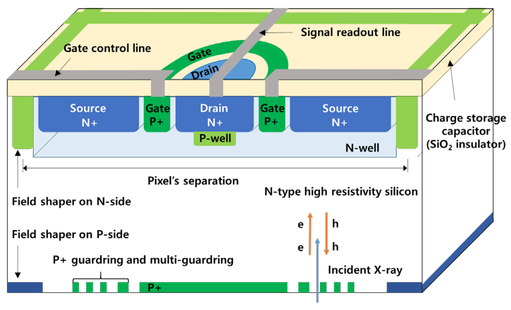


Fig. 1. A concept of JFET.

Design & Fabrication

- Pixel Sensor with JFET



- Substrate: <100>, > 5 kΩ•cm, n-type 6 in. silicon
- Thickness: (650 ± 25) μm
- Double-sided fabrication process
- Deep p-implantation (p-well) under drain for resistance when pixels are switched off
- Field shaper for pixel isolation on the JFET-side
- Field shaper for low leakage current on the rear-side
- Guard-ring for high breakdown voltage on the rear-side

Fig. 2. A cross-sectional view of the pixelated silicon detector integrated with JFET.

- Design

- A size of the single pixel is 100 x 100 μm^2, including the field shaper with 2 μm width.
- A 1x1 single pixel, 2x2 and 4x4 matrix, 1x16 array are designed.

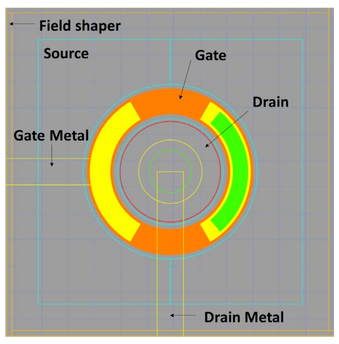


Fig. 3. (a) Single Pixel.

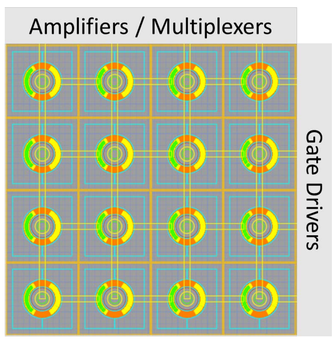


Fig. 3. (b) Pixel matrix.

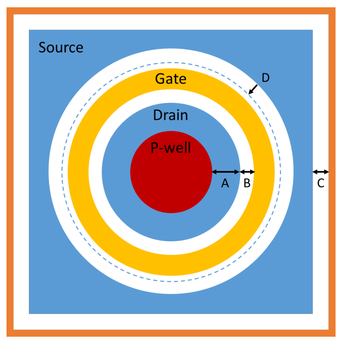


Fig. 3. (c) Design parameters.

Two major parameters highly affecting the drain current are
- A space = radius difference between drain and p-well
- B space = gap distance between drain and gate

(A: 0.5, 1.0, 1.4 μm) (B: 1.4, 1.8, 2.2 μm)

Two minor parameters
- C space = gap distance between source and field shaper
- D space = smaller inner radius of source

(C and D: 0, 5, 10 μm) ※ See "Results & Summary"

- The sensors are fabricated at ETRI (Electronics and Telecommunications Research Institute), Daejeon in S. Korea.
- A stepper photomask is used, which contains six layer patterns.
- Five aligner photomasks are used.

- Fabrication

Single-side [6 layers, 84 steps], 2018 **Double-side [11, 169], 2019** Double-metal [13, ~ 200], 2020

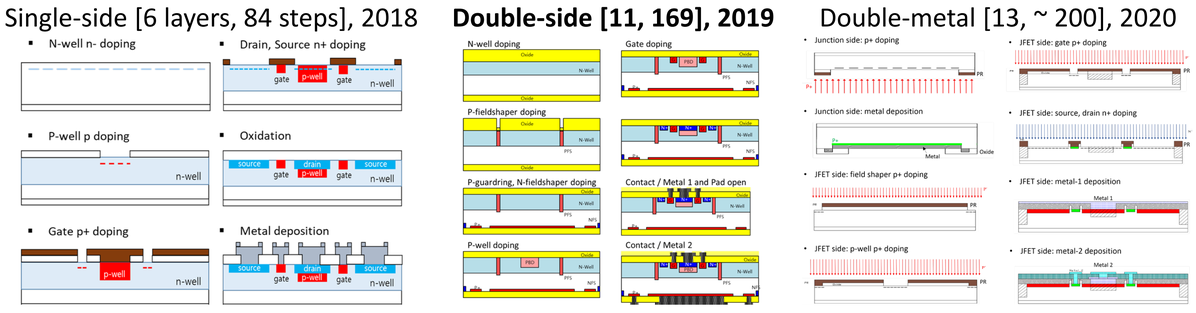
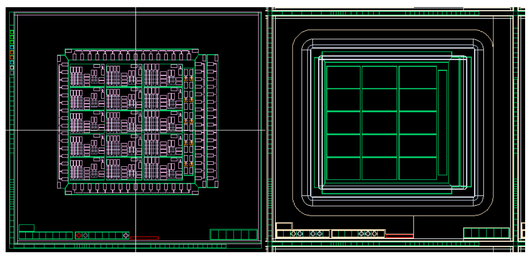
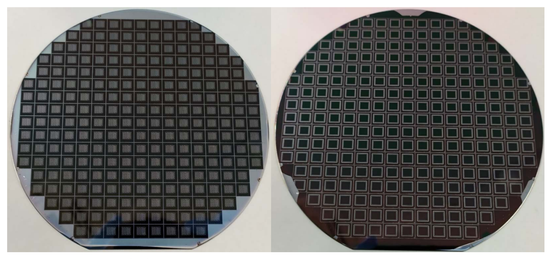


Fig. 4. Fabrication flow charts for (a) single-side, (b) double-side, and (c) double-metal structure.



(a) (b)

Fig. 5. Sensor designs for (a) JFET-side, (b) Junction-side.



(a) (b)

Fig. 6. Fabricated wafer for (a) JFET-side, (b) Junction-side.

Results & Summary

- Electrical characteristics of PIN structure

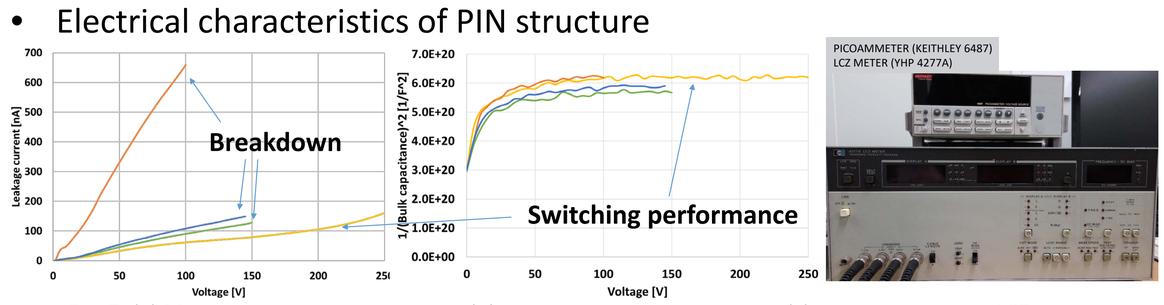


Fig. 7. (a) Measured leakage current and (b) capacitance of sensors using (c) picoammeter and LCZ meter.

- Switching performance

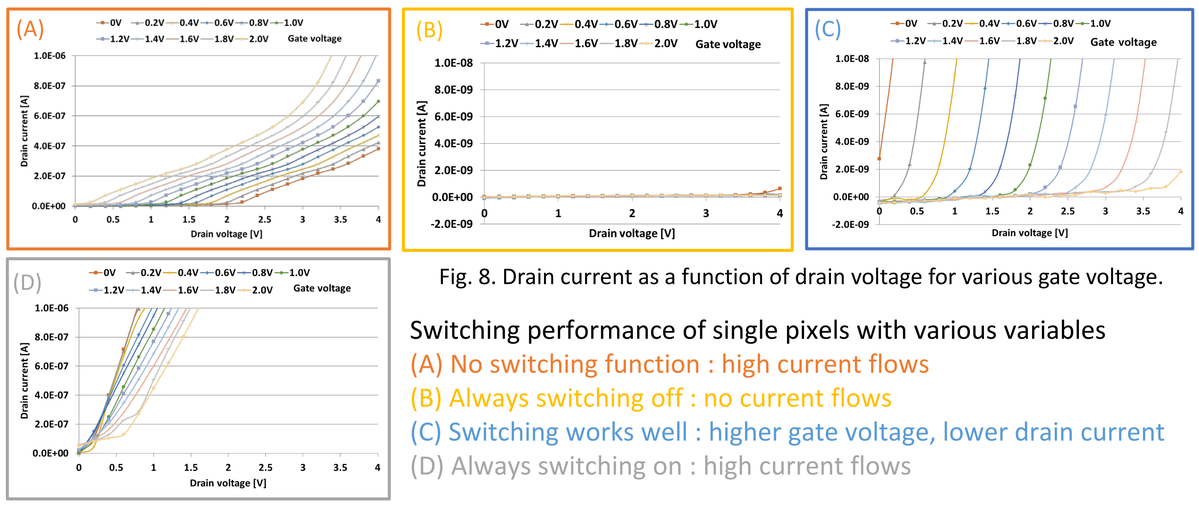


Fig. 8. Drain current as a function of drain voltage for various gate voltage.

Switching performance of single pixels with various variables
(A) No switching function : high current flows
(B) Always switching off : no current flows
(C) Switching works well : higher gate voltage, lower drain current
(D) Always switching on : high current flows

B space [um]

A space [um]	1st run	1.0	1.2	1.4	1.6	1.8
	0.2					
	0.3					
	0.5					

- In the '2018 run' sensor, five designs have proper switching capability as shown in (C).
- As A, B spaces become larger, pixels have good switching performance.
- For the '2019 run', we decided to design A, B spaces to be larger considering switching performances and align margin

Fig. 9. Switching performances of '2018 run' sensors.

B space [um] — D space 0 um

A space [um]	2nd run	1.4	1.8	2.2
	0.5			
	1.0			
	1.4			

C space 0 / 5 / 10 um

B space [um] — C space 0 um

A space [um]	2nd run	1.4	1.8	2.2
	0.5			
	1.0			
	1.4			

D space 0 / 5 / 10 um

Switching performance shows,
- if A space ≤ 0.3 μm, type (B) and (C) because of the P-well is so large to cover the drain.
- if A space ≥ 1.0 μm, type (D) because of the P-well is too small to meet the gate.
- in case of small B space, type (A) because of interference between drain and gate.

Fig. 10. Switching performances of '2019 run' sensors with difference A, B, and (a) C space / (b) D space.

- LED test **(LED Pulse variables: Amp. 1.3 V, Freq. 1 kHz, Width 100 - 400 μs)**

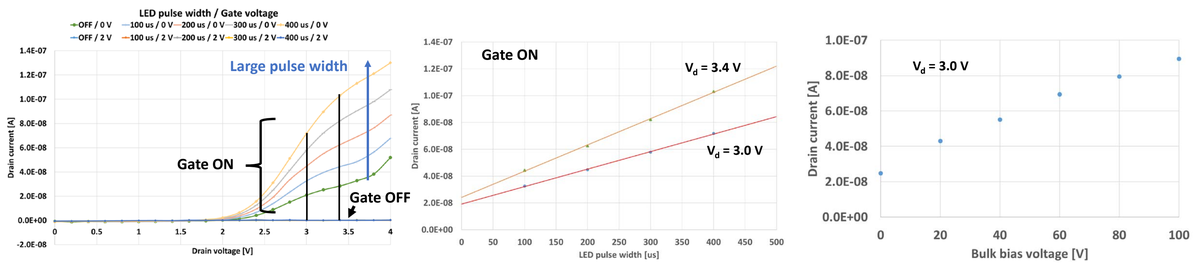


Fig. 11. Drain current for (a) with various LED pulse widths and (b) its linearity, and (c) various bulk bias voltages.

- As the LED pulse width increases, the photo-current increases and shows good linearity.
- As the bulk bias voltage increases, the depletion width increases, and this prevents signal loss in non-depleted layer.

- X-ray test **(x-ray generator COOL-X with intensity of 2~5 m cycle and energy of ~8 keV, AMPTEK)**

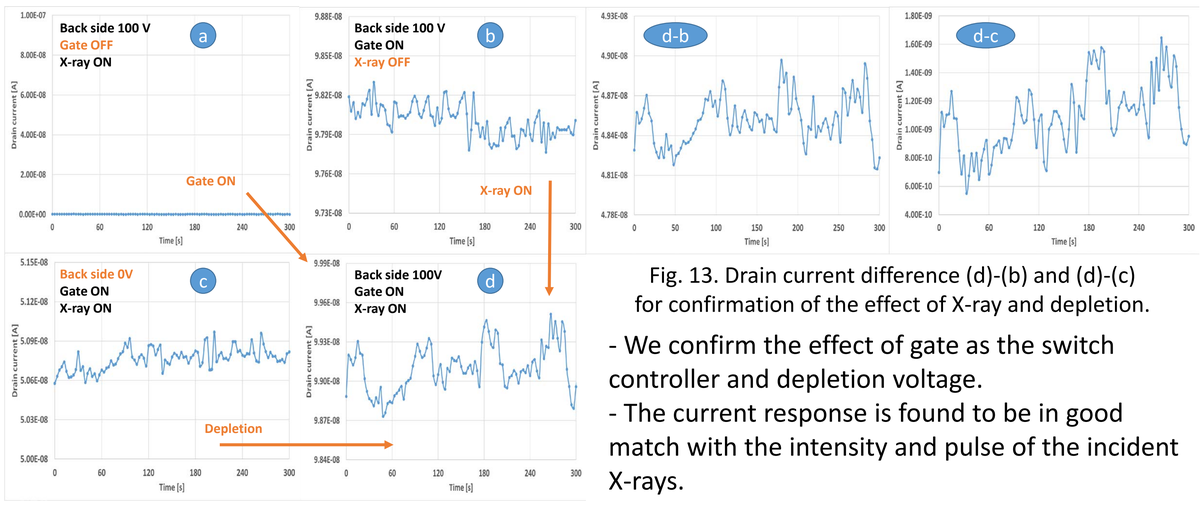


Fig. 13. Drain current difference (d)-(b) and (d)-(c) for confirmation of the effect of X-ray and depletion.

- We confirm the effect of gate as the switch controller and depletion voltage.
- The current response is found to be in good match with the intensity and pulse of the incident X-rays.

Fig. 12. Drain current (a) w/ gate OFF, (b) w/o X-ray, (c) depletion, and (d) w/ depletion, Gate ON, and X-ray.

- Fabrication process for double sides is hard to make perfect align and keep the sides clean.
- Based on the '2018 and 2019 run' studies, we are planning to design and fabricate a prototype of the JFET pixelated silicon sensor with the double metal structure.