

Fabrication and its Performance of a Pixelated Silicon Sensor Integrated with JFET

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In the previous Hiroshima symposium (HSTD11), we presented a detection concept of a pixelated silicon sensor integrated with junction field effect transistor (JFET), fabrication process flow charts of it, and simulation studies based on this detector concept. The JFET is designed to have the cylindrical structure and is used as a switch to readout charges accumulated in the pixelated sensor. We determine detector design parameters such as a distance between the source and the drain, a coverage region of the deep p-well implemented underneath the drain of the JFET, and doping concentration for the deep p-well. All pixels with one row are read in parallel and the next row is then selected by the gate voltage after finishing the reading one row. The photon detection efficiency of the silicon at low energy X-ray is very high so that this detection can be used for direct irradiation method, and the thickness of the active silicon should be twice of the absorption length of the silicon at that energy. We fabricate a pixelated silicon sensor integrated with JFET using a 625 μm -thick, high resistivity ($> 5 \text{ kohm}\cdot\text{cm}$) n-type and double-sided polished 6-in silicon wafer. In this poster we present electrical characteristics of the fabricated sensors and the drain currents as a function of the drain voltage for different the gate voltages. We also present the optimized design parameters of the prototype sensor to demonstrate the proper functioning of the switch.

Submission declaration

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