

Serial powering for the Phase 2 upgrade of the CMS pixel detector

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The Compact Muon Solenoid (CMS) silicon tracker will be replaced at the High Luminosity Large Hadron Collider (HL-LHC) upgrade by a new radiation-hard detector capable of handling higher pileup, higher data rates, and longer trigger latency. RD53A prototype chip in a 65 nm feature size CMOS technology has been developed by RD53 Collaboration to meet these requirements. Meeting the performance specifications requires higher granularity which leads to a higher power consumption. In addition, the smaller feature size leads to lower operating voltage, thus further increasing the current. This cannot be satisfied with the current parallel powering scheme, without significantly increasing the cable mass. Therefore a serial powering scheme will be used. A chain of modules will be powered by a constant current while the necessary internal rails will be provided by the special on-chip voltage regulators called Shunt Low Drop-Out (SLDO) regulators. The SLDO regulator also ensures that the chip sinks a constant input current independent of the internal circuit consumption. In addition, this scheme is less susceptible to voltage transients and noise, while improving the powering efficiency. Four chips on each module are powered in parallel to prevent a single failure from compromising the chain. Optimisation of this mixed scheme will be discussed light of the different failure modes. The first four-chip RD53A modules have been built to test the powering scheme in a realistic system. I will present the challenges of the module design and assembly. Furthermore, the performance of the individually powered modules will be compared to the serially powered chain.

Submission declaration

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