

**12th International  
"Hiroshima" Symposium on  
the Development and  
Application of Semiconductor  
Tracking Detectors (HSTD12)  
at Hiroshima, Japan**

**Report of Contributions**

Contribution ID: 196

Type: ORAL

## Radiation hard monolithic CMOS sensors with small electrodes for HL-LHC

*Monday, December 16, 2019 11:00 AM (20 minutes)*

The upgrade of the tracking detectors for the HL-LHC requires the development of novel radiation hard silicon sensors. The development of Depleted Monolithic Active Pixel Sensors (DMAPS) target the replacement of hybrid pixel detectors with radiation hard monolithic CMOS sensors. We designed, manufactured and tested DMAPS in the TJJ180nm CMOS imaging technology with small electrodes pixel designs. These designs can achieve pixel pitches well below current hybrid pixel sensors (typically  $50 \times 50 \mu\text{m}$ ) for improved spatial resolution. Monolithic sensors in our design allow to reduce multiple scattering by thinning to a total silicon thickness of only  $50 \mu\text{m}$ . Furthermore monolithic CMOS sensors can substantially reduce detector costs. These well-known advantages of CMOS sensor for performance and costs can only be exploited in pp-collisions at HL-LHC if the DMAPS sensors are designed to be radiation hard, capable of high hit rates and have a fast signal response to satisfy the 25ns bunch crossing structure of LHC.

Through the development of the MALTA and MiniMALTA sensors we will show the necessary steps to achieve radiation hardness at  $1\text{E}15$   $1\text{MeV}\cdot\text{neq}/\text{cm}^2$  for DMAPS with small electrode designs. The sensors combine high granularity (pitch  $36.4 \times 36.4 \mu\text{m}^2$ ), low detector capacitance ( $< 5\text{fF}/\text{pixel}$ ) of the charge collection electrode ( $3 \mu\text{m}$ ), low noise ( $\text{ENC} < 20\text{e}^-$ ) and low power operation ( $1 \mu\text{W}/\text{pixel}$ ) with a fast signal response (25ns bunch crossing). The sensors feature arrays of  $512 \times 512$  (MALTA) and  $16 \times 64$  (MiniMALTA) pixels. To cope with high hit rates expected at HL-LHC ( $> 200\text{MHz}/\text{cm}^2$ ) we have implemented a novel high-speed asynchronous readout architecture.

The presentation will show the optimization of the pixel implant structures and front-end to achieve radiation hard pixel designs with full efficiency after irradiation. Beam tests results will be presented to show the overall efficiency ( $> 98\%$  after  $1\text{E}15$   $1\text{MeV}\cdot\text{neq}/\text{cm}^2$ ) and timing properties of the sensors in recent measurements before and after irradiation.

### Submission declaration

Original and unpublished

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**Presenter:** PERNEGGER, Heinz (CERN)

**Session Classification:** Session6

**Track Classification:** Pixel sensors for tracking

Contribution ID: 197

Type: POSTER

## Studies for low mass large area monolithic silicon pixel detector modules using the MALTA CMOS pixel chip

*Saturday, December 14, 2019 3:07 PM (1 minute)*

Monolithic silicon pixel sensors combine the electronics and sensing layer in one silicon element and are produced in commercial CMOS processing lines without the need for a fine pitch interconnection technology as used for hybrid silicon pixel detectors. This reduces the overall cost, but also the complexity of the module assembly procedure. The sensors can be thinned to typical thicknesses of 100 microns or less, thus reducing the contribution of the silicon to the material budget. In present pixel detectors each pixel sensor is connected to a flexible circuit providing the necessary data and power connections. The flexible circuit contributes to the overall material budget in addition to the silicon and the mechanical support and cooling structures. Finally, all connections need to be routed within the narrow space available particularly in the innermost areas of the experiments.

The MALTA monolithic silicon pixel sensors have been used to study dicing and thinning of monolithic silicon pixel detectors for large area and low mass modules. Dicing as close as possible to the active circuitry will allow to build modules with very narrow inactive regions between the sensors. Inactive edge regions of less than 5 microns to the electronic circuitry could be achieved for 100 um thick sensors. The MALTA chip also offers the possibility to transfer data and power directly from chip to chip. Tests have been carried out connecting two MALTA chips directly using ultrasonic wedge wire bonding. Results from lab tests will be presented that show that the data accumulated in one chip can be transferred correctly via the second chip, without the need of a flexible circuit. The concept of chip to chip data and power transfer to achieve low mass modules has also been studied on prototype wafers using Cu-stud interconnection bridges. First mechanical results are presented, outlining technical challenges and possible future steps to achieve a low mass large area monolithic pixel sensor module.

### Submission declaration

Original and unpublished

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**Presenter:** RIEDLER, Petra (CERN)

**Session Classification:** POSTER

**Track Classification:** Large scale applications

Contribution ID: 198

Type: POSTER

## Development of Ultra-Radiation Hard 3D-Trench-Electrode Silicon Micro-Nano Detectors

*Saturday, December 14, 2019 2:19 PM (1 minute)*

This work develops a 3-Dimensional trench electrode (3D-Trench-Electrode) Si micro-nano detector with micron separation in electrodes and sub-micron (nano) electrode sizes for applications in extremely harsh radiation environments. Such extreme environments include CERN's Large Hadron Collider (LHC), nuclear explosion or radiation sites, and in deep space. The target total radiation fluence (or dose) is  $1 \times 10^{16}$  neq/cm<sup>2</sup> (neq = 1 MeV neutron equivalent) and higher. For the 3D-Trench-Electrode Si micro-nano detector, we use a cylindrical symmetry the one dimensional Poisson equation to obtain detector electric potential and field in a cylindrical coordinate [1].

In this work, we calculated the detector induced current and collected charges for a detector irradiated to various neutron fluences up to the extremely high value of  $1 \times 10^{17}$ /neq/cm<sup>2</sup>. We compare these results with those for conventional planar (2D) Si detectors to evaluate the radiation hardness of the 3D-Trench-Electrode Si micro-nano detector.

For a 3D-Trench-Electrode Si micro-nano detector with a cylinder outer diameter of  $R = 5$   $\mu$ m irradiated to a fluence of  $1 \times 10^{17}$ /neq/cm<sup>2</sup>, the induced current decrease somewhat. In fact, the charge collection efficiency (CCE) is now about 70.8%, about 31% reduction. However, as compared to that of an irradiated 2D planar detector with <1% in at  $1 \times 10^{17}$ /neq/cm<sup>2</sup> [2], it is indeed ultra radiation hard. The charge collection times are 32.1 ps and 11.3 ps for electrons and holes, respectively. its CCE is over 95% at  $1 \times 10^{16}$ /neq/cm<sup>2</sup>.

### Submission declaration

Original and unpublished

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**Presenter:** Ms KUANG, fenglan (xiangtan university)

**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 199

Type: POSTER

## Measured Effectiveness of Deep N-well Substrate Isolation in a 65nm Pixel Readout Chip Prototype

*Saturday, December 14, 2019 2:40 PM (1 minute)*

The same charge sensitive preamplifier and discriminator circuit with different isolation strategies has been tested to compare the isolation of both analog and digital circuits from the substrate of a 65 nm bulk CMOS process to the isolation of only digital circuits, tying analog ground locally to the substrate. This study will show that the circuit with analog on the substrate and digital in deep N-well has better noise isolation between analog and digital.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** ASICs

Contribution ID: 201

Type: ORAL

## Vertex and Tracking Detector R&D for CLIC

*Sunday, December 15, 2019 12:00 PM (20 minutes)*

The physics aims at the proposed future CLIC high-energy linear e+e- collider pose challenging demands on the performance of the detector system. Precise hit-time tagging with ~5 ns resolution is required for the vertex and tracking detectors, to mitigate the impact of beam-induced background on the measurement accuracy. Moreover, a low mass of ~0.2% X<sub>0</sub> per layer for the vertex and ~1% X<sub>0</sub> per layer for the tracker is needed, combined with a single-plane spatial resolution of a few micrometers. To address these requirements, an all silicon vertex and tracking system is foreseen at CLIC. To this end, a broad R&D program on new silicon detector technologies is being pursued. For the ultra-light vertex detector, different small pitch (25 um) hybrid technologies with innovative sensor concepts are explored. A dedicated 65 nm readout chip (CLICpix2) has been developed and interconnected via fine pitch bump-bonding to thin planar sensors. Furthermore, alternative interconnects such as bonding using anisotropic conductive films (ACF) are explored. Adapted to the low duty cycle of CLIC, pulsed power operation has been implemented in CLICpix2 and experimentally tested. Moreover, various Silicon On Insulator (SOI) test chips are under study. For the large-scale silicon tracker, fully monolithic CMOS technologies are considered. CMOS sensors with a large collection electrode have been extensively studied in various test-beam campaigns. Using 3D TCAD simulations, innovative sensor concepts have been developed for CMOS sensors with a small collection electrode, and implemented in various prototype chips targeting CLIC and other future projects. A dedicated tracker prototype chip using a 180 nm CMOS process with a high-resistivity epitaxial layer and an innovative sub-pixel segmentation scheme has recently been produced and is currently under evaluation. To predict the performance of the various prototype technologies, a fast and versatile Monte Carlo Simulation Tool (Allpix-Squared) has been developed. This contribution gives an overview of the R&D program for the CLIC vertex and tracking system, highlighting new results from measurements and simulations of recent prototypes.

### Submission declaration

Original and unpublished

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Contribution ID: 203

Type: ORAL

## State-of-the-art and evolution of UFSD sensors design at FBK.

Wednesday, December 18, 2019 12:00 PM (20 minutes)

In the past few years, there has been growing interest in the development of silicon sensors able to simultaneously measure accurately the time of passage and the position of impinging charged particles. In this contribution, I will review the progress in the design of UFSD (Ultra-Fast Silicon Detectors) sensors, developed for tracking charged particles in 4 dimensions, manufactured at the FBK (Fondazione Bruno Kessler) Foundry. The state-of-the-art UFSD sensors, with excellent timing capability, are planned to be used in the detector upgrade for the HL-LHC (High Luminosity Large Hadron Collider), in both ATLAS and CMS experiments, in order to reduce the background due to the presence of overlapping events in the same colliding bunch crossing.

The latest results on the sensors characterization, including time resolution, radiation resistance and uniformity of the response, will be presented, pointing out the interplay between the design of the gain layer and the UFSD performances. The current understanding of how the co-implantation of carbon and boron is affecting the characteristics of the gain layer will be reported. The research is also focusing on the maximization of the sensor fill factor, exploring the implementation of shallow tranches for the pixel isolation and the development of resistive AC-coupled UFSD sensors. I will conclude the review outlining different research paths which are tailored for other applications, such as the detection of low energy X-rays or the realization of low-power tracking detectors for space satellites.

### Submission declaration

Original and unpublished

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**Session Classification:** Session12

**Track Classification:** New ideas and future applications

Contribution ID: 204

Type: ORAL

## A new generation of radiation hard 3D pixel sensors for the HL-LHC era

*Monday, December 16, 2019 9:00 AM (20 minutes)*

The ATLAS experiment at Large Hadron Collider (LHC) will replace its inner tracker system to cope with the extreme particle fluence expected after the High Luminosity upgrade of the accelerator (HL-LHC).

The 3D silicon sensor technology has been selected as baseline to instrument the innermost layers of the pixel detector in the future ATLAS Inner Tracker (ITk).

A new generation of 3D pixel sensors with thin active substrates and small pixel cells of  $50 \times 50 \mu\text{m}^2$  and  $25 \times 100 \mu\text{m}^2$  produced at CNM in Spain, have been interconnected to the RD53A chip, the first prototype of ASIC for the HL-LHC.

Performance of these new 3D RD53A modules have been studied before and after uniform proton irradiations up to  $10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ , i.e. a particle fluence close to the one required for the innermost layer of ITk.

The first results of the power dissipation and hit efficiency for 3D RD53A devices uniformly irradiated will be presented. The measurements revealed a superior radiation hardness of these novel pixel sensors with respect to previous generation of 3D devices.

### Submission declaration

Original and unpublished

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**Session Classification:** Session5

**Track Classification:** Pixel sensors for tracking

Contribution ID: 205

Type: POSTER

## Analysis of multiple cell upset characteristics for logical circuits in radiation environment

*Saturday, December 14, 2019 2:57 PM (1 minute)*

With the design and fabrication of integrated circuits entering the deep-submicron and nano-scale era, the possibility of radiation induced multiple cell upset (MCU) increases noticeably. Extracting the MCU characteristics (size, proportion, etc) from the observed radiation-induced upsets can provide useful information for designing hardening strategies and fault injection experiments, which is of great importance for both storage circuits and logical circuits. For logical circuits composed of storage cells (DFF, etc) and combination logic gates (inverter, NAND, etc), the recorded information during irradiation only consist of upset counts but without the corresponding addresses. It is not easy to identify the MCU size and the corresponding proportion information as storage circuits.

In this work, a statistical analysis procedure of MCU characteristics in logical circuits was proposed. Our contributions focus on extending MCU feature extraction from storage circuits to logical circuits. Meanwhile, besides the geometrical progression distribution proposed in the reference, Gaussian distribution was proposed, verified, and implemented in MCU study to describe the condition when more than 1-bit upset dominates. When developing the model, a lot of data from references were adopted, with the Device under Test (DUT) of 150nm, 90nm, 65nm, and 25nm feature sizes. The choice of average upset counts in each read cycle was recommended, to reach an estimation accuracy within 20%. In this way, we may evaluate the MCU characteristics in logical circuits, both upsets due to cells and burst upsets due to global resources.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 206

Type: POSTER

## Analysis of CSNS neutron-induced displacement damage effects on top illumination planar InGaAs p-i-n photodetectors

*Saturday, December 14, 2019 2:58 PM (1 minute)*

Indium gallium arsenide (InGaAs) photodiodes have been widely used in space domain, such as satellite attitude control, optical communications, and satellite remote sensing. But when used in these environment, they will be damaged by particles or rays, which would lead to the parameter degradation or even functional failure. The mainly radiation damage induced by particles or rays of InGaAs photodiodes are ionizing effects and displacement damage effects.

In this work, the displacement damage effects on InGaAs p-i-n photodetectors induced by neutron at China Spallation Neutron Source (CSNS) are analyzed. The InGaAs p-i-n photodetector under investigated were fabricated with top illumination structure. The active diameter is about 60  $\mu\text{m}$ , and the response spectrum are ranging from 900 nm~1700 nm. The experiment were carried out at CSNS. The neutron energy are ranging from 1eV to 200MeV. The forward and reverse bias current-voltage (I-V) and capacitance-voltage (C-V) under the dark environment are measured before and after neutron radiation at room environment. The frequency of the C-V measurement are ranging from 10 kHz to 5 MHz. The mechanism of displacement damage effects on the I-V and C-V characters of InGaAs p-i-n photodetectors are analyzed.

### Submission declaration

Original and unpublished

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**Presenter:** Mr XUE, Yuanyuan

**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 208

Type: POSTER

## Charge transfer inefficiency degradations of the CCD detector induced by proton and neutron radiation

*Saturday, December 14, 2019 2:59 PM (1 minute)*

Charge coupled devices (CCDs) have been widely used as detectors for particle detection and space applications for their merits of low cost, small size and high sensitivity. Charge transfer inefficiency (CTI) degradations of the CCD detector used in harsh radiation environments are one of the main concerns of the detector performance. The CTI degradations are very sensitive to the displacement damage induced by proton or neutron radiation and usually not sensitive to the ionization damage induced by gamma ray or X-ray radiation.

The proton radiation experiments were carried out at the cyclotron accelerator (at China institute of atomic energy, Beijing, China) with energies of 60 and 90 MeV. The neutron radiation experiments were carried out at the back-streaming white neutrons at China Spallation Neutron Source (CSNS) (at institute of high energy physics, Dongguan, China) and at Xi'an pulse reactor (XAPR) (at Northwest Institute of Nuclear Technology, Xian, China). The CTI degradations were measured at the saturation and half saturation illumination.

The research reported herein examines the CTI degradations of the CCD detectors induced by proton and neutron radiation. The CTI degradations versus the proton or neutron fluences are presented. The annealing tests after radiation are also performed to observe the CTI recovery. The degradation mechanisms of the CTI induced by proton and neutron radiation damage are demonstrated in details. The research will provide the basis of the theories and experiment techniques to evaluate the CTI degradations of the CCD detectors induced by proton or neutron displacement damage.

### Submission declaration

Original and unpublished

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**Presenter:** Prof. WANG, Zujun

**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 210

Type: POSTER

## The effects of trapped charge on the signal formation and on the detection efficiency for subsequent pulses in irradiated silicon sensors at operating temperature

*Saturday, December 14, 2019 3:00 PM (1 minute)*

Envisaged high energy physics experiments like the Future Circular Collider require unprecedented radiation hardness of the detectors, as well as short readout time due to high luminosity and occupancy. Silicon has proven to be extremely radiation hard, clear and fast signals can be recorded even at fluences close to  $1 \cdot 10^{16} n_{eq}/\text{cm}^2$ .

The signal formation in silicon strip sensors, irradiated and annealed until the phenomenon of charge multiplication occurred, was studied. ATLAS12EC R0 mini sensors were tested by means of Edge TCT measurements at temperatures around  $-20^\circ\text{C}$ .

It was observed that the flow of generated charge changes the signal pulse in time, especially in charge multiplication regime. Moreover, it was observed that the detection of subsequent signals separated even several microseconds is altered by the charge trapped during the first pulses.

The effects of trapped charge on the electrical configuration of a sensor is well known as a pumping effect in larger band-gap materials like diamond, but is often neglected for silicon at this relatively high temperature.

The investigation of the effect created by trapped charges in silicon sensors using subsequent pulses allows to gain information on important parameters such as de-trapping times. Furthermore, it shows a severe impact on the sensor performance in a pile-up scenario. The irradiation fluence and hence the effective doping concentration, the temperature and the amount of initially created charge have a large impact on this phenomenon.

The presented measurements help to characterize this phenomenon and particular attention was paid at the application point of view.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 211

Type: ORAL

## 4D tracking systems at future hadron colliders

Wednesday, December 18, 2019 11:20 AM (20 minutes)

In the present design of the ATLAS and CMS silicon trackers for the HL-LHC, the silicon sensors are exposed to fluences above  $1E16$  n/cm<sup>2</sup>. These systems foresee the replacements of the inner layers once or twice during the HL-LHC lifetime.

On the other hand, the design of future high-intensity hadronic machines, such as FCC-hh, foresee a much higher level of radiation, above  $1E17$  neq/cm<sup>2</sup>, that, with the present tracker design, implies a replacement of a large part of the tracker almost every year.

Given that the physics requirements at FCC-hh require excellent 4D tracking capability, or the order of 10 microns and 10 picoseconds, a strong research development effort is required.

In this contribution, we propose a possible approach to the design of the tracker systems for FCC-hh that employs very thin silicon sensors (20-30 micron) with moderate gain (gain 3-5) in the internal layer, where the radiation is the highest (up to radii  $\sim 20$  cm), for position measurement, and slightly thicker sensors (40-50 micron) for 4D measurement (with gain 10-15) at a radius where the fluence drops below  $\sim 1E16$  neq/cm<sup>2</sup>

For the inner layer, this design relies on the fact that very thin sensors are intrinsically radiation resistance (almost absent trapping, low depletion voltage, low leakage current), and that the interplay of the gain mechanisms, either in the gain layer and/or in the bulk, provides enough charge (the present ASIC designs require a signal of  $\sim 1fC$ ) for a fully efficient detection. In the external layers, an evolution of the present state-of-the-art 4D UFSD (Ultra-fast Silicon Detector) design will ensure enough charge to make possible the accurate measurement of position and time.

### Submission declaration

Original and unpublished

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**Session Classification:** Session12

**Track Classification:** New ideas and future applications



Contribution ID: 212

Type: POSTER

## Mapping the in-plane electric field inside irradiated diodes

*Saturday, December 14, 2019 3:02 PM (1 minute)*

A significant aspect of the Phase-II Upgrade of the ATLAS detector is the replacement of the current Inner Detector with the ATLAS Inner Tracker (ITk). The ATLAS ITk is an all-silicon detector consisting of a pixel tracker and a strip tracker.

Sensors for the ITk strip tracker have been developed to withstand the high radiation environment in the ATLAS detector after the High Luminosity Upgrade of the Large Hadron Collider at CERN, which will significantly increase the rate of particle collisions and resulting particle tracks.

During their operation in the ATLAS detector, sensors for the ITk strip tracker are expected to accumulate fluences up to  $1.5 \cdot 10^{15}$  neq/cm<sup>2</sup> (including a safety factor of 1.5), which will significantly affect their performance.

One characteristic of interest for highly irradiated sensors is the shape and homogeneity of the electric field inside its active area.

For the results presented here, diodes with edge structures similar to full size ATLAS sensors were irradiated up to fluences comparable to those in the ATLAS ITk strip tracker and their electric fields mapped using a micro-focused X-ray beam (beam diameter  $2 \times 3 \mu\text{m}$ ).

This contribution shows the extension and shape of the electric field inside highly irradiated diodes over a range of applied bias voltages. Additionally, measurements of the outline of the depleted sensor areas allow a comparison of the measured leakage current for different fluences with expectations for the corresponding active areas.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 213

Type: ORAL

## Commissioning and performance of Belle II pixel detector

*Sunday, December 15, 2019 9:20 AM (20 minutes)*

The Belle II experiment at the SuperKEKB energy-asymmetric  $e^+e^-$  collider has completed a series of substantial upgrades and started collecting data since Mar.2019. The designed peak luminosity is  $8 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$  and the experiment is expected to accumulate a data set of  $50\text{ab}^{-1}$  by 2027, to explore new physics beyond the Standard Model at the intensity frontier. The pixel detector (PXD) of Belle II plays a key role in the vertex determination. It has been developed using the DEpleted P-channel Field Effect Transistor (DEPFET) technology, which combines low power consumption in the active pixel area and low intrinsic noise with a very small material budget. In this talk, commissioning and performance of PXD measured with first collision data will be presented.

### Submission declaration

Original and unpublished

**Primary author:** Dr YE, Hua (DESY)

**Presenter:** Dr YE, Hua (DESY)

**Session Classification:** Session1

**Track Classification:** Pixel sensors for tracking

Contribution ID: 214

Type: ORAL

## WERPAD: a CdTe pixel detector for wide energy range X-ray diffractions

*Sunday, December 15, 2019 3:20 PM (20 minutes)*

The synchrotron radiation facility provides monochromatic X-rays but the beams have higher harmonics contamination. We proposed multi-energy X-ray diffractions using the primary and higher harmonics beams. This method could acquire larger Q information with the same exposure time of monochromatic beam measurement. Furthermore, the white X-ray Laue diffraction could determine the lattice spacing by measuring the angle and energy of diffraction patterns. According to this concept, we developed a Wide Energy Range Pixel Array Detector (WERPAD) combined with a CdTe sensor and photon-counting ASICs. A single platinum-electrode (X-ray irradiation side) and 190 × 200 matrix of aluminum-electrodes (readout side) were processed on a high resistivity p-type CdTe single crystal of 0.75 mm in thickness. A high Schottky barrier was formed on the Al/CdTe interface and this condition leads us to operate an electron-collecting diode pixel detector. SP8-04F10K ASICs have been fabricated with the TSMC 180 nm technology. Each pixel has a preamplifier, a shaper, 3-level window-type comparators and a 24-bits counter. WERPAD2 was designed with a pixel size of 0.2 mm by 0.2 mm and an area of 38.2 mm by 40.2 mm. Simultaneous X-ray diffraction measurement with 61.4 keV and 122.8 keV X-ray beams was performed with a carbon steel specimen by the dual window comparator mode. The phase transformation process was measured with conical nozzle levitation. White X-ray Laue diffractions has investigated to measure strains of coarse-grained materials. The diffraction spot energies were determined by the threshold scans. The strains of the bending specimen were measured, and the results corresponded to the applied strains estimated with the strain gauge.

### Submission declaration

Original and unpublished

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**Presenter:** TOYOKAWA, Hidenori (Japan Synchrotron Radiation Research Institute)

**Session Classification:** Session3

**Track Classification:** Pixel sensors for imaging

Contribution ID: 215

Type: POSTER

## ATLAS17LS - Large-format prototype silicon strip sensors for the long-strip barrel section of the ATLAS ITk strip detector

*Saturday, December 14, 2019 2:33 PM (1 minute)*

A new inner tracker (ITk) is to be installed inside the solenoid magnet of the upgraded ATLAS detector, to measure tracks of charged particles produced in the proton-proton collisions at the high-luminosity large hadron collider (HL-LHC) at CERN. Silicon strip detectors cover outer layers of ITk with  $\sim 165 \text{ m}^2$  of silicon sensors, composed of “short strips” (2.41 cm long) and “long strips” (4.83 cm long) sections in the inner and outer layers, respectively, split at a radius of  $\sim 75 \text{ cm}$  to cope with the density of tracks.

A prototype silicon strip sensor for the “long strips” in the barrel section, ATLAS17LS, was laid out having the largest sensor in the 6-in. silicon wafer, with an outer dimension of 9.80 (width) $\times$ 9.76 (length)  $\text{cm}^2$ , two rows of strip segments, strip pitch of 75.5  $\mu\text{m}$ , and an edge space of 450/550  $\mu\text{m}$  in the longitudinal/lateral direction to the strips (slim edge), as well as miniature sensors and test structures in the wafer periphery for validating and monitoring the sensors. The sensor is a single-sided n-in-p AC-readout strip sensor, made of  $\text{n}^+$  implant strips for signal collection in p-type wafer material, AC-coupled to readout electronics, and implementing knowledge for high voltage operation up to 1000 V, to have good signal-to-noise ratio until the end of life of the HL-LHC operation.

The ATLAS17LS sensors had two purposes: (1) qualification of the sensor itself, technology and capability of fabricating vendors, and (2) serving for prototyping the building block of the strip detector, the strip modules. Hamamatsu Photonics (HPK) was one of two vendors participating in the evaluation along with Infineon Technologies (IFX). The sensors at HPK were fabricated in 3 batches: 1<sup>st</sup> with the silicon wafer (320  $\mu\text{m}$  physical thickness) and the active thickness of standard or as thin as 250  $\mu\text{m}$ , 2<sup>nd</sup> with a small number of supplementary sensors of special passivation to investigate humidity sensitivity of passivation, and 3<sup>rd</sup> with a dicing scheme of structures in the wafer periphery in the series-production style.

### Submission declaration

Original and unpublished

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**Presenter:** UNNO, Yoshinobu (High Energy Accelerator Research Organization (JP))

**Session Classification:** POSTER

**Track Classification:** Strip sensors

Contribution ID: 216

Type: POSTER

## Design, electrical properties and fabrication method study of a novel 3D-Compound-Shell-Electrode silicon detector

*Saturday, December 14, 2019 2:20 PM (1 minute)*

In this work, a novel three-dimensional (3D) structure of silicon detector: 3D-Compound-Shell-Electrode detector (3DCSED), based on the 3D-Trench-Electrode detector and 3D-Open-Shell-Electrode detector (3DOSED), is proposed. In a 3DCSED, an open trench electrode will be etched about 10% of the detector thickness from the bottom side of the detector to meet the close trench electrode etched about 90% of the detector thickness from the top side. This ensure not only the unit structure be stable in the fabrication process, but also the detection efficiency can be guaranteed through the optimization of the electrode structure comparing to the conventional 3D-Trench-Electrode detector. In order to optimize the 3DCSED structure, it is important to study 3DCSED's electrical properties to determine the detector's working performance by full 3D technology computer-aided design (TCAD) simulations. From the electric field distribution results, detector charge collection efficiency has been improved by optimization of the detector trench electrode, and the trapping problem in the detector bulk has been solved. Due to the highly doped trenches, each pixel cell is isolated to ensure a uniform electric field distribution, but electrically and physically connected with each other through the remaining silicon bulk between broken electrodes. Furthermore, the current-voltage (I-V) characteristics, capacitance-voltage (C-V) characteristics, charge collection property, and full depletion voltage have been analyzed to study the detector's properties under heavy radiation environment for high energy application. Last but not least, in this work, we propose a method to fabricate the 3DCSED. In this method, the deep etching is processed by Deep Reacting Ion Etching (DRIE) or laser wit respective processing procedures.

### Submission declaration

Original and unpublished

**Primary authors:** Dr LIU, Manwen; Prof. LI, Zheng

**Presenter:** Dr LIU, Manwen

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for tracking

Contribution ID: 217

Type: ORAL

## Development of Planar Pixel Sensors for the CMS Inner Tracker at the High-Luminosity LHC

*Tuesday, December 17, 2019 9:20 AM (20 minutes)*

The LHC is planning an upgrade program which will bring the luminosity up to about  $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  in 2027, with the goal of an integrated luminosity of  $3000 \text{ fb}^{-1}$  by the end of 2037. This High Luminosity scenario, HL-LHC, will present new challenges of higher data rates and unprecedented radiation levels for the pixel detector ( $2 \times 10^{16} \text{ n}_{eq} \text{ cm}^{-2}$ , or equivalently 1 Grad, is expected for the inner layer of the CMS Inner Tracker (IT) for  $3000 \text{ fb}^{-1}$  integrated luminosity).

To maintain or even improve the performance of the present system, new technologies have to be exploited for the so-called Phase-2 upgrade. Among them is the future version of front-end chips in 65-nm CMOS by the CERN RD53 Collaboration which supports small pixel sizes of  $50 \times 50$  or  $25 \times 100 \mu\text{m}^2$  and low pixel charge thresholds ( $\sim 1000 \text{ e}^-$ ).

Thin planar n-in-p type silicon sensors with a thickness of the active layer of  $150 \mu\text{m}$ , segmented into pixel sizes of  $25 \times 100 \mu\text{m}^2$  or  $50 \times 50 \mu\text{m}^2$  will be used throughout most of the IT. They have been shown to allow for a good detector resolution that is much more stable with respect to radiation damage compared to the Phase-1 detector. CMS has launched several R&D submissions for the development of suitable planar silicon sensors at HPK photonics, FBK Trento and LFoundry. We will present results for measurements on such prototype sensors bump bonded to the RD53A prototype chip developed by the RD53 collaboration at CERN. The presentation will concentrate on planar sensors manufactured by Hamamatsu and FBK. Different pixel cell designs are compared and evaluated in testbeams at CERN, DESY and FNAL for spatial resolution and hit efficiency at various track angles before and after irradiation. As an example, hit efficiencies of 99% at vertical incidence were reached after irradiation to  $5 \times 10^{15} \text{ n}_{eq} \text{ cm}^{-2}$  which corresponds to the layer 2 lifetime fluence of the CMS IT.

### Submission declaration

Original and unpublished

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**Presenter:** STEINBRUECK, Georg (Hamburg University (DE))

**Session Classification:** Session7

**Track Classification:** Pixel sensors for tracking

Contribution ID: 219

Type: POSTER

## Measuring the borders of the active area on silicon strip sensors

*Saturday, December 14, 2019 2:38 PM (1 minute)*

Silicon strip sensors for the ATLAS Inner Tracker (ITk) have been designed to provide reliable particle detection in the high-radiation environment of the High-Luminosity Large Hadron Collider. One important design criterion for their development is the minimisation of inactive sensor area (bias ring, guard ring and edge implant surrounding the active sensor area), as inactive sensor areas impact the hermeticity of particle detection inside the detector.

In previous measurements of ATLAS silicon strip sensors, the charge collecting area of individual strip implants has been mapped and found to agree well with the sensor strip pitch and strip length. For strip implants next to the sensor bias ring, the extent of their charge collecting area towards the inactive sensor area was previously unknown, which limited the accuracy of both overall detector hermeticity estimates and the position resolution for particle detection at the sensor edge. Therefore, measurements were conducted to map the area of charge collection for sensor strips at the edge of the active sensor area. Using a 1micro-focused X-ray beam has made it possible to map this shape both within the sensor plane as well as inside the sensor volume.

This contribution presents measurements showing the extent of charge collection in the edge strips (with a condition where the AC metal of a strip between the bias ring and the edge strips is being floated) of silicon strip sensors. The edge regions of two generations of ITk strip sensor modules were studied: one module with a short strip (ATLAS12 with 2.5 cm strip length) sensor and ABC130 readout chips and one module a long strip (ATLAS17LS with 5 cm strip length) sensor and ABCstar readout chips.

### Submission declaration

Original and unpublished

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**Presenter:** SANTPUR, Sai Neha (Lawrence Berkeley National Lab. (US))

**Session Classification:** POSTER

**Track Classification:** Strip sensors



Contribution ID: 220

Type: POSTER

## Optical transceivers for event triggers in the ATLAS phase-I upgrade

*Saturday, December 14, 2019 3:12 PM (1 minute)*

The ATLAS phase-I upgrade aims to enhance event triggers in the Liquid Argon (LAr) calorimeter and the forward muon spectrometer. The trigger signals are transmitted with customized optical transceivers at ~5 Gbps per channel in a radiation hazard. We report on the design, quality control in production and ageing tests of the transceivers fabricated with the LOClD laser driver circuits and multi-mode 850 nm vertical-cavity surface-emitting laser (VCSEL). The modules are packaged in customized miniature formats of dual-channel transmitter (MTx) and transceiver (MTRx) for the LAr. The transmitters are also packaged in the commercial small form-factor pluggable (SFP) format for the muon spectrometer. The LOClD is configurable for laser bias and modulation of outputs. In production, the LOClD chips, the 10 Gbps VCSELs and photodiodes in TOSA/ROSA format were measured and selected for uniformity in quality. Each channel is tested for 10 Gbps Bit-Error with the eye-diagrams recorded for analysis. The average light power and modulation amplitude of transmitters are distributed with standard deviations in 5 %. The production yield is better than 99 % for the total of about 5k modules. Ageing effects are monitored in burn-in of a small batch of transmitter modules in room condition. The eye-diagrams are measurements periodically and the observables are stable within the 5% systematic uncertainty over a period of more than 4k hours.

### Submission declaration

Original and unpublished

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**Presenter:** LI, Jia-Hao (National Taiwan University (TW))

**Session Classification:** POSTER

**Track Classification:** Technologies

Contribution ID: 221

Type: ORAL

## Test beam studies of barrel and endcap modules for the ATLAS ITk strip detector before and after irradiation

*Tuesday, December 17, 2019 2:20 PM (20 minutes)*

In order to cope with the occupancy and radiation doses expected at the High-Luminosity LHC, the ATLAS experiment will replace its Inner Detector with an all-silicon Inner Tracker (ITk), consisting of pixel and strip subsystems. The strip subsystem will be built from modules, consisting of one  $n^+$ -in-p silicon strip sensor, manufactured by Hamamatsu Photonics, and one or two PCB hybrids containing the front-end electronics glued directly to the sensor. A powerboard, containing an HV switch, a monitoring and control ASIC, and a DC-DC converter, is also glued to the sensor.

In the last two years, several prototype ITk strip modules have been tested using beams of high energy electrons and charged pions produced at the DESY-II and CERN SPS testbeam facilities. Tracking was provided by EUDET telescopes, consisting of six Mimosas26 pixel planes, giving a resolution around  $2\ \mu\text{m}$ . The modules tested are built from two sensor types: the rectangular ATLAS17LS, which will be used in the central barrel region of the detector, and the annular ATLAS12EC, which will be used in the innermost ring (R0) of the forward endcap region. Each sensor geometry has been tested using both the final prototype version of the front-end electronics, known as “star” chipset, as well as a previous prototype chipset developed for lower trigger rate specification. Additionally, a structure with two R0 modules positioned back-to-back has been measured, demonstrating space point reconstruction using the stereo angle of the strips. Finally, two R0 modules, one with each chipset, have been measured after irradiation to 50% beyond the expected end-of-lifetime fluence.

The data obtained allow for thorough tests of the module performance, including charge collection, noise occupancy, detection efficiency, and tracking performance. Additionally, the excellent tracking resolution allows for detailed studies of various sensor features. The results give confidence that the ITk strip detector will meet the requirements of the ATLAS experiment.

### Submission declaration

Original and unpublished

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**Presenter:** RUEHR, Frederik (Albert Ludwigs Universitaet Freiburg (DE))

**Session Classification:** Session9

**Track Classification:** Strip sensors

Contribution ID: 222

Type: ORAL

## Development of high resolution low power CMOS pixel sensor for the CEPC vertex detector

*Monday, December 16, 2019 11:40 AM (20 minutes)*

Circular Electron Positron Collider is proposed as the future higgs factory. There are two different detector concepts and their variants being in the process of optimization. In either concepts, the vertex sub-detector is important for the flavor tagging. The relevant physics cases require high spatial resolution, low occupancy and low material budget; and the operation condition requires low power consumption and high radiation tolerance. These specifications have to compromise with each other. In particular the specifications of spatial resolution and power consumption are contradictory in terms of pixel pitch. For a spatial resolution of 3  $\mu\text{m}$ , the pixel pitch needs to reach 16-18  $\mu\text{m}$ . In the development of CMOS pixel sensor for the CEPC vertex, an in-pixel signal discrimination and a sparsified readout are identified as the key points for low power design, while keeping focus on the reduction of pixel pitch.

Based on the above design choices, a CMOS pixel sensor has been designed and submitted for tape-out. The pixel matrix is 512 rows by 192 columns, divided into 4 sectors with 48 columns per each sector. The vertical pitch is 16  $\mu\text{m}$  for each sector, which is assumed to be the  $r\phi$  direction in the vertex sub-detector. The horizontal pitch is increased to be able to accommodate the complete pixel circuit, 26  $\mu\text{m}$  for sector 0, 1, 3 and 23.11  $\mu\text{m}$  for sector 2 due to different configuration of circuit blocks. Hit information is scanned one row after another (rolling shutter) at 200 ns/row and then feed into the asynchronous encoders at the end of column. These encoders and associated buffers are organized for each sector independently, so that the matrix can be expanded to a full size by increasing the number of sectors in the future. Total power consumption is estimated to be < 100 mW/cm<sup>2</sup>.

### Submission declaration

Original and unpublished

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**Presenter:** LU, Yunpeng (Chinese Academy of Sciences (CN))

**Session Classification:** Session6

**Track Classification:** Pixel sensors for tracking

Contribution ID: 223

Type: POSTER

## Prototyping of a 25 Gbps optical transmitter for applications in high-energy experiments

*Saturday, December 14, 2019 2:41 PM (1 minute)*

Development of optical links with 850 nm multi-mode vertical-cavity surface-emitting laser (VCSEL) has advanced with the transmission rate achieving beyond 25 Gbps. For applications in high-energy experiments, the transceivers are required for tolerance in ionizing and particle radiation fields. We report on prototyping of a transmitter developed for high speed transmission with the dual-channel LOC65 laser driver and the 850 nm VCSELs of types qualified for 10 Gbps and 25 Gbps in TOSA assembly. The LOC65 chips fabricated by the TSMC 65 nm process are packaged in QFN-40 format. The modules and test kits were first made with PCB of FR-4 material, and the performance reached 14 Gbps. The speed exceeds the expected and therefore the electronic design was revised for higher performance. The PCB material is replaced by the Megtron-6 and the circuit layout is optimized for 25 Gbps data transmission. To differentiate the performance dragged by slow components, the test samples are also made with 10 Gbps TOSA and the eye-diagram observed is qualified for 15 Gbps. The best equipped transmitters have achieved high speed performance with the eye-diagrams showing a 20% margin with a 25 Gbps mask.

### Submission declaration

Original and unpublished

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**Presenter:** HOU, Suen (Academia Sinica (TW))

**Session Classification:** POSTER

**Track Classification:** ASICs

Contribution ID: 224

Type: POSTER

## A Readout Network ASIC for High-Density Electrode Array Targeting Neutrinoless Double-Beta Decay Search in TPC

*Saturday, December 14, 2019 2:42 PM (1 minute)*

Among the current and planned experiments of neutrinoless double-beta decay ( $0\nu\beta\beta$ ), the high-pressure gaseous TPC stands out for its excellent energy resolution, low radioactive background and good scalability. Moreover, high position resolution can be maintained with an appropriate charge readout scheme for TPC to further suppress the background through ionization imaging. A low noise sensor, Topmetal-S, is being developed which, even without gas gain, the energy resolution requirement could be met. Since  $0\nu\beta\beta$  tracks are extended to tens of cm in high-pressure gas, Topmetal-S is designed to have a mm-sized electrode, followed by an amplifier and an ADC in the first prototype. To realize a ton-scale TPC, approximately one hundred thousand Topmetal-S need to be laid on a meter-sized plane. The greatest challenge is reliable high-density sensor readout. A distributed, self-organizing and fault-tolerance readout network ASIC is implemented and will be integrated into Topmetal-S as a router. The scheme establishes local connection between nearby sensors to form a network. Each sensor not only generates and transmits their own data, but also forwards data from nearby sensors, and data are finally received by a computer connected to the edge of the network. 2D-Mesh is chosen as the topology of the network. A distributed routing algorithm, Fault-Tolerance-XY (FT-XY), is implemented. The routing algorithm relies only on local information. The algorithm is also fault-tolerant, so that failed sensors will not disable a large section of the network. By sending fault detection packets, the computer will form a set of rectangular region called faulty blocks to contain detected faults. The FT-XY routing follows the regular XY routing until the packet reaches faulty block. Then, the packet will be routed around the block to pass through. The throughput and latency of the readout network reaches 11641 Mbit/s and 120  $\mu$ s. The design is implemented on a 130-nm CMOS process and submitted in June 2019. The details of the routing algorithm, the fault detection scheme, the micro-architecture of the router, and preliminary test results will be presented.

### Submission declaration

Original and unpublished

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**Presenter:** XIAO, Le (Central China Normal University)

**Session Classification:** POSTER

**Track Classification:** ASICs

Contribution ID: 225

Type: ORAL

## PulseDL: A reconfigurable deep learning array processor dedicated to pulse characterization for high energy physics detectors

Wednesday, December 18, 2019 10:00 AM (20 minutes)

CR-RCn shaping circuits and analog-to-digital converters (ADCs) are widely used to process the front-end pulse from detectors in high energy physics. Recovering the information from ADC sampling points can be formulated as a regression problem. Traditional methods (least square fitting, Kalman filtering, etc.) are statistically optimal with linear model and Gaussian noise, whereas non-ideal characteristics of the shaped pulse and detector-dependent drift and fluctuations pose challenge to these methods. In contrast, neural networks exhibit great advantages because of its universal approximation property and its insensitivity to system bias and non-Gaussian noise, which gives a 20% increase in accuracy compared to curve fitting according to a recent paper. In this work, we implemented a multi-functional neural computing chip for pulse shaping in high energy physics. We adopted a structure of RISC CPU and customized Processing Units (PEs) for balanced power and performance. A  $4 \times 4$  PE array was proposed to perform neural computation with concurrency, and each PE performed multiply-accumulate operations with minimum area and latency. A structure combining the spatial and the temporal adder tree for post-PE operations reduced off-chip efforts. Buffers were inserted in the pipeline, and the global control distributed configuration signals. The entire chip was interfaced with the ICB bus as a standalone IP core. Based on the chip, we co-designed the network architecture to best utilize the logic functions. The network was made up of a ten-layer denoising autoencoder and a three-layer fully-connected network. Convolution, transpose convolution and fully-connected operations were fitted into the hardware with on-chip reconfiguration. This network architecture could effectively suppress non-ideal characteristics of the input time series and improve the precision of extracted information. Finally, we designed the chip layout following the standard digital ASIC flow. The automatic placement and routing were made under the GSMCR013 130nm process, with  $4.9mm \times 4.9mm$  area, at least 25MHz working frequency and 1.2V core voltage. Measured by post-layout simulations, the power efficiency of the chip was estimated to be about 7GOPS/W.

### Submission declaration

Original and unpublished

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**Presenter:** AI, Pengcheng (Central China Normal University)

**Session Classification:** Session11

**Track Classification:** ASICs



Contribution ID: 226

Type: POSTER

## A SEL Sensitive Area Testing System for Integrated Circuits Based on the MAPS Detector

*Saturday, December 14, 2019 3:03 PM (1 minute)*

Many electronic systems are designed to work in the environment of radiation and should have the radiation tolerance ability. Particularly the Single Event Effect (SEL) could induce the latchup of CMOS Integrate Circuits (IC) and degrade the device functionality. Therefore, the study of test methods for SEL sensitive area of integrated circuits becomes an important subject which helps us analyze the ability of anti-radiation and guides radiation hardening.

The traditional position systems for latchup are mainly based on microbeams or lasers and need mechanical devices with high precisions to move the injection spot of particles or the position of the device to be radiated. However, the system has some drawbacks: difficult to manufacture, expensive, time-consuming and inefficient. The Monolithic Active Pixel Sensor (MAPS) has advantages of high spatial resolution, thin materials, strong anti-radiation and mature fabrication technology, which make it a suitable candidate for particle tracking. We developed a camera based on MAPS to obtain a latchup map that reveals the distribution of SEL sensitive areas of integrate circuits. The MAPS detector records the incident position of the particles and the system determines the time when latchup occurs. The statistical method is used to calculate the probability of latchup of each small area. The TOPMETAL-III, used in this system, is a MAPS detector designed independently by Central China Normal University and its core functional block is a matrix composed of (512 rows x 256 columns) pixels, with 40  $\mu\text{m}$  pitch, for a chip size of 2.3 cm x 1.2 cm. It has 300 kRad anti-radiation capabilities, with thickness less than 50 $\mu\text{m}$ , and is manufactured with the GSMC 0.13 $\mu\text{m}$  process. The system will be tested on the Heavy Ion Research Facility at Lanzhou, China (HIRFL) by particles of  $^{86}\text{Kr}$  with 25MeV/u energy. Meanwhile other related subjects have been researched: mechanism of protecting the MAPS, algorithm of generating probability density of latchup, the influence of beam type and strength on the test precision, the detection method of latchup and so on.

### Submission declaration

Original and unpublished

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**Presenter:** Mr SHEN, Fan (Central China Normal University)

**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 227

Type: ORAL

## Readout demonstrator for a Large-Scale Pixel-Detector conforming to the ATLAS Phase-II Upgrade

*Tuesday, December 17, 2019 9:00 AM (20 minutes)*

After a long design and development, a prototype of the pixel detector front-end chip that will be proposed for the ATLAS and CMS experiments at CERN during HL-LHC has been recently available. It provides data streams using up to four lanes running at 1.28 Gbps each. This paper describes in detail the implementation of a first readout chain of this chip, namely the RD53A, using the current the main ATLAS Phase-II readout board. For this work the readout chain has required dedicated electronics as a hardware interface between the front-end chip and the readout board. Moreover, to maximize the efficiency of testing the chip and to realize the Data AcQuisition (DAQ) chain to be used by Phase-II ATLAS, it is extremely important that, even for the first prototypes, the DAQ chain is as similar as possible to the final one. The implemented chain has been left available at CERN for further tests and developments for the entire ATLAS TDAQ collaboration. This readout chain is proposed as a general readout for Large-Scale Application of pixel detectors. Full details of the prototype and testing performed to date will be presented.

### Submission declaration

Original and unpublished

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**Session Classification:** Session7

**Track Classification:** Large scale applications

Contribution ID: 228

Type: ORAL

## First characterisation of 3D pixel sensors irradiated at extreme fluences.

*Tuesday, December 17, 2019 3:20 PM (20 minutes)*

During the last decade at the Large Hadron Collider, the 3D pixel sensors have been widely used as particle tracking detectors for several experiments such as the Insertable B-Layer (IBL), ATLAS Forward Proton (AFP) in ATLAS and the TOTal cross section, Elastic scattering and diffraction dissociation Measurement (TOTEM) in CMS.

In this talk, we present for the first time, the 3D pixel sensors irradiated with neutrons up to a fluence of  $3 \times 10^{17} n_{eq}/cm^2$ . TCT measurements and charge collection efficiency showed that the sensors remain operative despite the unprecedented levels of irradiation similar of those estimated in the Future Circular Collider (FCC).

### Submission declaration

Original and unpublished

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**Session Classification:** Session9

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 229

Type: POSTER

## A novel Pinned Depleted Diode design for the CEPC vertex detector

*Saturday, December 14, 2019 2:21 PM (1 minute)*

The Circular Electron Positron Collider (CEPC) has been proposed in China as a Higgs and/or Z factory. Pixel sensors with high spatial resolution, low material budget and low power consumption are required for the inner most layer of vertex detector. As a part of R&D activities, a prototype of SOI pixel sensor with a novel Pinned Depleted Diode (PDD) design has been developed accordingly, to explore the small pixel pitch and low noise level.

The PDD structure has the same feature as the Double-SOI does, which realizes the shielding between the sensing node and electric circuit. Besides, the PDD structure has the advantages of very low leaking current and very high charge collection efficiency. However, due to the large area of shielding layer adjoining the sensing node, it suffers from large diode capacitance. A TCAD simulation has shown that at least -4V biased voltage must be applied between sensing node and shielding layer to maintain the capacitance below 6fF. On the other hand, the shielding layer cannot be connected to a very low voltage, as this will cause the circuit to work improperly. A traditional solution is adding -2V to the shielding layer and using HV\_P MOS (3.3V) as the signal input transistor. In this way, at most -6V can be biased. A novel bias method is adopted in our design. We add the positive voltage to the sensing node through a diode and the signal is ac-coupled with the front-end circuit. By using this structure, a biased voltage as low as -10V may be applied to achieve much small diode capacitance.

As for the in-pixel circuit, on one hand, a traditional 3T structure is chosen for the test of sensor performance. On the other hand, a complex circuit including amplifier, CDS and discriminator is developed to explore the low noise front-end circuit. The characterization of sensor and circuit will soon be performed in the lab and experimental results will be presented in our report.

### Submission declaration

Original and unpublished

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**Presenter:** Mr WU, Zhigang (IHEP)

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for tracking

Contribution ID: 230

Type: ORAL

## Humidity Sensitivity of Large Area Silicon Sensors: Study and Mitigation

*Tuesday, December 17, 2019 2:40 PM (20 minutes)*

The production of large area sensors is one of the main challenges that the ATLAS collaboration faces for the new Inner-Tracker (ITk) full-silicon detector. During the prototype fabrication phase for the High Luminosity Large Hadron Collider (HL-LHC) upgrade, several ATLAS institutes observed indications of humidity sensitivity of large area sensors, even at relative humidities well below the dew formation. Specially, barrel and end-cap silicon strip sensors fabricated in 6-inch wafers manifest a prompt decrease of the breakdown voltage when operating under relative humidity above a threshold, adversely affecting the performance of the sensors.

This work presents an extensive study of this behavior on large area sensors. The locations of the hotspots at the breakdown voltage for different humidity levels are revealed using different infrared thermography techniques. Several palliative treatments are attempted, proving the influence of sensor cleaning methods or baking on the device performance, but no influence on the humidity sensitivity. Furthermore, an extensive study of the incidence of the sensitivity is presented, showing the time evolution and radiation influence. In addition to the investigation of these prototype sensors, a specific fabrication batch of large sensors with special passivation is also studied and complemented with simulations, allowing for a deeper understanding of the responsible mechanisms.

Finally, a summary of the actions to be taken during sensor production and assembly is derived from this work, in order to minimize the impact of humidity sensitivity on the performance of large area silicon sensors for High Energy Physics (HEP) experiments.

### Submission declaration

Original and unpublished

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**Presenter:** FERNANDEZ-TEJERO, Javier (CNM-Barcelona (ES))

**Session Classification:** Session9

**Track Classification:** Strip sensors

Contribution ID: 231

Type: ORAL

## Process quality control strategy for the Phase II upgrade of the CMS tracker and endcap calorimeters

*Tuesday, December 17, 2019 11:40 AM (20 minutes)*

The CERN Large Hadron Collider (LHC) will undergo a major upgrade between 2024 and 2026, to increase the collision rate by a factor of about 5 compared to the present. Some existing components of the CMS detector - most notably the Tracker and Endcap Calorimeters - will have to be replaced in order to cope with the conditions of the high luminosity (HL-LHC) era: instantaneous peak luminosity up to  $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  and integrated luminosity up to  $3000 \text{ fb}^{-1}$  by 2037. Over 50,000 new silicon sensors covering a total area of about  $800 \text{ m}^2$  will comprise the CMS tracker and parts of the CMS endcap calorimeters. The quality of the sensors and the production process must be monitored constantly during production time to facilitate stable operation under HL-LHC conditions. This presentation introduces the process quality control strategy for the sensor series production. Each manufacturing wafer contains at least two instances of a set of test structures designed to provide fast and easy access to critical process parameters. These include parameters not directly accessible on the sensors (e.g. oxide charge concentration and interface trap density) and parameters requiring potentially destructive measurements (e.g. dielectric strength). The set is divided into test structures for initial evaluation of the most relevant process parameters and structures for in-depth analysis in case of problems. All structures can be contacted using a 20-needle probe card and an automated positioning stage. With this system, the initial analysis of one wafer is possible in under 30 minutes. We present the finalized layout of the set that will be implemented in the production runs for the CMS outer tracker and the endcap calorimeters, and report on measurements illustrating the functionality of the included test structures.

### Submission declaration

Original and unpublished

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**Co-author:** ON BEHALF OF THE CMS COLLABORATION

**Presenter:** HINGER, Viktoria (Austrian Academy of Sciences (AT))

**Session Classification:** Session8

**Track Classification:** Technologies

Contribution ID: 232

Type: POSTER

## A low-power small-area 6T sram cell for tracking detector applications

*Saturday, December 14, 2019 2:43 PM (1 minute)*

This paper presents a low-power small-area six-transistor (6T) SRAM cell, which uses only one bit line and applies an additional switch to cut the competition path during the write access. The proposed 6T SRAM cell has been applied in a pixel array detector to configure a Digital-to-Analog Converter (DAC) in each pixel to improve the charge threshold uniformity. Compared to the conventional 6T SRAM cell, simulation results show the power consumption is reduced by about 44% and the area is decreased by about 25% without the performance degradation. The measurement results show that the novel 6T SRAM cell works very well.

Pixel detectors have been widely used for high energy particle physics and medical applications, which play a role of energy measurement, tracking detection and time of arrival measurement. They are developed toward the trend of large scale, high resolution and low power consumption. To improve detection efficiency, it is necessary to reduce the threshold and improve the threshold uniformity. An effective method is tuning the threshold of each pixel, which is composed of coarse and fine adjustment. As usual, the fine adjustment is realized by in-pixel DAC with registers of the corresponding bit number. The conventional D-type Flip Flop (DFF) register can be competent to store the input data of the DAC. However, DFF registers have large area and power consumption, especially for more bits. Compared to DFF registers, the conventional six-transistor (6T) SRAM cell reduces both area and power consumption. The proposed 6T SRAM cell reduces more power consumption compared to the conventional 6T SRAM cell.

In the conference, we will introduce the structure and performance of the proposed 6T SRAM cell in detailed. We will also show the improvement of the threshold uniformity of a pixel detector after the proposed 6T SRAM cell is applied.

### Submission declaration

Original and unpublished

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**Presenter:** Dr GAO, chaosong (Central China Normal University)

**Session Classification:** POSTER

**Track Classification:** ASICs



Contribution ID: 233

Type: POSTER

## Strip sensor performance in prototype modules built for ATLAS ITk

*Saturday, December 14, 2019 2:35 PM (1 minute)*

The ATLAS Phase-II Upgrade for the High-Luminosity LHC features replacement of the Inner Detector with an all-silicon Inner Tracker (ITk). The majority of the instrumented area in ITk is occupied by strip modules covering  $165 \text{ m}^2$ . A vigorous R&D program has been on-going for many years to prepare for the scale of the project and to work out technical issues at all key components of the system, including the strip sensors, readout ASICs, hybrids, modules, and staves.

In this submission we report on the performance of silicon strip sensors used in the last completed round of module prototyping. Over 80 modules were built and tested with electrical readout on the per-channel basis and the sensor performance was assessed. In general, an excellent performance was observed, consistent with previous ASIC-level and sensor-level tests. However, the lessons learned included two phenomena important for the future phases of the project. First was the need to store and test the modules in a dry environment due to humidity sensitivity of the sensors. The second was a rare observation of high noise on some channels, at the rate of about 3%.

The high noise regions were tested further in several ways, including monitoring the performance as a function of time and bias voltage. Additionally, direct sensor-level tests were performed on the affected channels. The inter-strip resistance and bias resistance tests showed low values, indicating a temporary loss of the inter-strip isolation. A subsequent recovery of the noise performance was observed. We present the test details, an analysis of how the inter-strip isolation affects the module noise, and relationship with sensor-level quality control tests.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Strip sensors

Contribution ID: 234

Type: POSTER

## A simple identification of multiple-hit events to improve the image quality of fine-pixel scintillation detector

*Saturday, December 14, 2019 2:01 PM (1 minute)*

Scintillation detectors are widely used in various imaging techniques in the fields of medicine, astronomy, and environment. In general, large-area and fine-pixel scintillation arrays are needed to improve the sensitivity and image quality of detectors. However, a large scintillation array requires a huge number of read-out channels, which makes the detector system complex and expensive. The use of a resistive charge-division network can effectively reduce the number of read-out channels. However, the disadvantage is that such detectors are insensitive to “multiple-hit” events, in which gamma rays interact multiple times within the same scintillator array. In this paper, we propose a simple method to identify multiple-hit events to improve the image quality of fine-pixel scintillation detectors. As a first demonstration, we obtained the flood map of a 42 times 42 Ce:GAGG scintillator array coupled with 8 times 8 MPPC of 3 times 3mm<sup>2</sup> pixels. Using a 2D charge division network, 64 ch signals from MPPCs are compiled into four analog signals from the corners, S0, S1, S2, and S3. Then, the centroid of X and Y can be calculated in two ways by different groupings of S<sub>i</sub>. We assume that mismatched position (either X or Y) may be due to multiple-hit events that occurred within the scintillator. By rejecting such multiple-hit events, which accounts for ~10% of the total, we confirmed that the peak-to-valley rate of the flood map improved from 6.00 to 8.79 at 350-550 keV with irradiated <sup>137</sup>Cs. In general, multiple-hit events tend to occur during high-energy events. We also confirmed that the rejection rate was higher in the high-energy range compared with the low-energy range as expected by drawing spectral of rejected events. Our method is easy to use and can be applied to existing data for improving the image quality of fine-pixel scintillation detector.

### Submission declaration

Original and unpublished

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**Presenter:** SATO, Shogo (Waseda University)

**Session Classification:** POSTER

**Track Classification:** Technologies

Contribution ID: 235

Type: **ORAL**

## **ATLAS ITk Pixel endcap demonstrator construction and testing**

*Tuesday, December 17, 2019 10:00 AM (20 minutes)*

The ATLAS upgrade programme for the high-luminosity large hadron collider (HL-LHC) includes the replacement of the inner tracking detector with an all-silicon system. The outer layers of the new tracker consist of strip sensors and the inner region is made up of pixel sensors. This paper describes the development of the endcaps for the pixel system. The endcaps are built from half-rings carrying the pixel modules and the services. A prototype half-ring populated with pixel modules read out using FEI4 front-end ASICs in serial powering chains was constructed. The half-ring mechanical and electrical structure and the assembly process will be described. The electrical measurements of the modules will be presented, focusing on their performance in the serial powering chain.

### **Submission declaration**

Original and unpublished

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**Session Classification:** Session7

**Track Classification:** Large scale applications

Contribution ID: 236

Type: POSTER

## Thermal management issue in module assembly for the ATLAS ITk pixel upgrade

*Saturday, December 14, 2019 3:10 PM (1 minute)*

The ATLAS upgrade programme for the high-luminosity large hadron collider (HL-LHC) includes the replacement of the inner tracking detector with an all-silicon system. The outer layers of the new tracker consist of strip sensors and the inner region is made up of pixel sensors. The harsh radiation environment requires the pixel system to run at low temperature to minimise damage to the silicon sensors. The pixel system runs at a coolant temperature of -35C and the sensors at the end of life will operate at around 0C, but the modules are constructed at room temperature, around 20C. The large difference in temperatures leads to stresses in the pixel modules due to mismatches in the coefficients of thermal expansion of the different materials making up the module. These stresses can result in failure of the solder bumps used to connect the front-end ASICs to the sensors. The stresses in the module have been studied using Finite Element Analysis (FEA), which has identified a number of key factors that contribute to the stresses in the module. The predictions of the FEA model have been compared to the results of thermal cycling measurements on prototype modules.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Large scale applications

Contribution ID: 238

Type: POSTER

## Results from the CBC3.1 readout ASIC for CMS 2S-modules

*Saturday, December 14, 2019 2:44 PM (1 minute)*

The CBC3.1 is the final version of the CMS Binary Chip for readout of the outer radial region of the upgraded

CMS Tracker at the High Luminosity LHC. The development began a decade ago.

The 254-channel, 130 nm CMOS ASIC is designed to be bump-bonded

to a hybrid substrate to which sensors will be wire-bonded. It will instrument double-layer 2S-modules, containing two

overlaid silicon microstrip sensors, aligned with a parallel orientation. On-chip logic identifies Level-1 trigger

primitives from high transverse-momentum tracks by selecting correlated clusters in the two sensors.

The CBC3.1 was delivered in September 2018, and ~6000 chips from 13 wafers have been studied in detail using an automatic wafer probing setup. A high yield of good chips was observed but also patterns possibly characteristic of manufacturing variations, similar to some which had been noticed following manufacture of other chips in the same process. The process has since been optimised and 48 further wafers are expected imminently which will allow evaluation of production yields.

As the tracker will be operated at very low temperatures, of  $-20^{\circ}\text{C}$  to  $-30^{\circ}\text{C}$ , other measurements have been carried out to evaluate the CBC performance under expected operating conditions. Prototype modules are now being assembled and studied so that construction of the new tracker can begin in 2020.

The main features of the measured CBC3.1 performance will be summarised and detailed results from recent studies will be reported.

### Submission declaration

Original and unpublished

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**Presenter:** UCHIDA, Kirika (Imperial College (GB))

**Session Classification:** POSTER

**Track Classification:** ASICs

Contribution ID: 239

Type: ORAL

## Single Event Upset evaluations of CBC readout chips

*Tuesday, December 17, 2019 5:20 PM (20 minutes)*

The CMS Binary Chip (CBC) is the front-end ASIC to be used by the CMS tracker following its upgrade for High Luminosity LHC operation. It will instrument modules known as 2S-modules to read out silicon microstrip sensors which are intended to identify high transverse momentum particles in real time so that tracking data can be used for the first time in the L1 trigger. The CBC should be robust against Single Event Upsets and various design features have been incorporated to achieve that. The CBC development is now complete.

The SEU rate has been measured several times using different versions of the CBC in a series of tests in a 62 MeV proton beam to evaluate its sensitivity for use in the CMS tracker. Each version of the chip (CBC2, CBC3.0, CBC3.1) has increased the digital circuitry, and hence the SEU susceptibility, and has also been subject to design improvements which affect the SEU tolerance. The relevant design features are explained and SEU measurements are reported. The expected SEU rates in CMS 2S-modules at the HL-LHC are estimated.\

### Submission declaration

Original and unpublished

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**Session Classification:** Session10

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 240

Type: POSTER

## Measurements and simulations of surface and bulk radiation damage effects in silicon detectors for phase II CMS outer tracker

*Saturday, December 14, 2019 3:04 PM (1 minute)*

Radiation damage effects at High Luminosity LHC (HL-LHC) expected fluences at the outer tracker layers greater than  $1 \times 10^{15} \text{ n/cm}^2$  1 MeV equivalent, as well as total ionising doses on the order of 70 Mrad, will impose very stringent constraints in terms of radiation resistance of solid-state detectors, from both silicon substrate and silicon oxide.

In this contribution we address the effects of bulk and surface damage on detectors fabricated on Hamamatsu standard FZ p-type material with an active thickness of 290  $\mu\text{m}$  or thinned to 240  $\mu\text{m}$ . The planned irradiation and measurement campaigns focuses specifically on disentangling the effects of the two main radiation damage mechanisms, ionization effects and atomic displacement, highlighting any device weak points for improvements, aiming at more radiation resistant solutions.

To this purpose, the interface trap state density and the oxide charge can be extracted from standard test structures for each substrate before and after irradiation with X-rays with doses ranging from 0.05 to 70 Mrad(SiO<sub>2</sub>), aiming at the surface damage characterization.

Neutron irradiations in the range of  $1 - 10 \times 10^{14} \text{ n/cm}^2$  1 MeV equivalent will be also performed. Measurements on the very same structures will be repeated after both irradiations, allowing the combined surface and bulk damage to be investigated.

TCAD simulation tools will be used to validate a previously developed radiation damage model.

These complementing simulation results could give further insight in the underlying mechanisms. The model can be also used as a predictive tool to optimize the design and the operation of novel silicon detectors in the HL-LHC scenario.

In this contribution the obtained measurements will be shown and discussed in view of the underlying model of the simulation reproducing these results.

### Submission declaration

Original and unpublished

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**Presenter:** MARIANI, Valentina (Universita e INFN, Perugia (IT))

**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials



Contribution ID: 242

Type: POSTER

## Design and hardware evaluation of the optical-link system for the ATLAS Liquid Argon Calorimeter Phase-II Upgrade

*Saturday, December 14, 2019 3:13 PM (1 minute)*

An optical link system based on lpGBT and VTRx+ is being developed for the ATLAS Liquid Argon Calorimeter Phase-II upgrade. The optical link system is responsible to transmit the detector data and clocks/control signals for 1524 Front-End Boards (FEBs) through 26 optical fibers per FEB over 150 meters.

The optical links can be divided into two categories, data links and control links. For data links, each FEB has 22 simplex optical links, each operating at 10.24 Gbps. The detector data come from 640-Mbps e-ports of 8-analog-channel ADCs. In order to recover the ADC word boundary, which is lost after optical links, each ADC implements two dedicated output channels with a special data format. For control links, each FEB employs 2 duplex optical links for the following functions. Firstly, control links provide recovered clocks for ADCs. Secondly, we offer a bunch crossing reset signal for each ADC via an e-port. Thirdly, we utilize the I2C masters of lpGBTs to access remotely the internal registers of all ASICs. Fourthly, control links remotely control and monitor ASICs via the Digital Input and Output (DIO) ports. Finally, temperatures and power supply voltages/currents are monitored via the intrinsic ADC of lpGBTs.

A printed circuit board has been designed to evaluate the major functions of the optical link system. The board has an lpGBT, a VTRx+, and two FMC connectors interfacing with an FPGA. The uplink and the downlink data transmissions have been successfully verified. The word boundary recovery has been demonstrated. The initial evaluation of the recovered clocks, the DIOs, the I2C interface, and the intrinsic ADC of the lpGBT have been done and extensive evaluation is still ongoing. The evaluation results will be presented in the symposium and the future paper.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Technologies

Contribution ID: 245

Type: ORAL

## Charge Collection of the ATLAS ITk Prototype Silicon Strip Sensors ATLAS17LS for the HL-LHC

*Tuesday, December 17, 2019 12:00 PM (20 minutes)*

The inner tracker of the ATLAS detector will be replaced by a silicon-based completely new inner tracker (ITk) for the Phase 2 of the CERN LHC (HL-LHC). The silicon strip detector covers the volume  $40 < R < 100$  cm in radial and  $|z| < 300$  cm in longitudinal directions. The silicon sensors for the detector will be fabricated on n+-on-p 6-inch wafer technology, for the total of 22 thousand wafers. Intensive studies were carried out on the final prototype sensors ATLAS17LS fabricated by Hamamatsu Photonics. The charge collection properties were examined using penetrating  $^{90}\text{Sr}$   $\beta$ -rays and ALIBAVA fast readout system for the miniature sensors of  $1\text{cm} \times 1\text{cm}$  in area. The samples were irradiated by protons in the 28 MeV Birmingham cyclotron, 70 MeV CYRIC at Tohoku University and 24 GeV CERN-PS, and by neutrons at Ljubljana TRIGA reactor up to  $2 \times 10^{15}$  neq/cm<sup>2</sup> fluence. The change in the charge collection with fluence was found to be similar to the previous prototype ATLAS12, and acceptable for ITk. The sensors with two active thicknesses 300  $\mu\text{m}$  (standard) and 240  $\mu\text{m}$  (thin) were compared and difference in the small charge collection after irradiation between them was observed to be in the operation bias voltage range up to 500 V. This was also verified by the studies of the changes in the charge collection as a function of the depth measured by an edge-TCT technique. Some samples were also irradiated with gammas up to 2 MGy, and the full depletion voltage was found to decrease with the dose, indicating acceptor removal caused by  $^{60}\text{Co}$  irradiation. In summary, the ATLAS17LS design and fabrication technology have been verified for implementation in the ITk. We are in the stage of sensor pre-production with the first sensors scheduled to be delivered at the end of 2019.

### Submission declaration

Original and unpublished

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**Presenter:** HARA, Kazuhiko (University of Tsukuba (JP))

**Session Classification:** Session8

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 246

Type: ORAL

## Electrical characterization of surface properties of the ATLAS17LS sensors after neutron, proton and gamma irradiation

*Tuesday, December 17, 2019 12:20 PM (20 minutes)*

The high luminosity upgrade of the Large Hadron Collider, foreseen for 2026, requires the replacement of the ATLAS Inner Detector with a new all-silicon Inner Tracker (ITk). After an integrated luminosity of  $4000 \text{ fb}^{-1}$  the ITk Strip Detector will have been exposed to a large radiation fluence, corresponding to a 1 MeV neutron equivalent fluence of up to  $\Phi_{\text{neq}} = 1.6 \times 10^{15} \text{ cm}^{-2}$ , and an ionising dose of  $\approx 66 \text{ Mrad}$ , including the safety factor of 1.5. A radiation hard  $n$ -in- $p$  micro-strip sensor for the use in the ITk has been developed by the ATLAS ITk Strip Sensor collaboration and produced by Hamamatsu Photonics. In this talk, the results obtained from the electrical characterization of the latest barrel ATLAS17LS sensor prototype before and after irradiation will be shown.

Surface properties of the barrel long strip full-sized and miniature sensors have been studied before and after proton, neutron and gamma irradiation up to the maximal fluences and radiation doses specified for ITk Strip Tracker. Sensors have been irradiated by protons at CYRIC, Tohoku University (Japan) and at CERN IRRAD proton irradiation facility, by neutrons from Ljubljana TRIGA reactor (Slovenia) and by gamma rays from  $^{60}\text{Co}$  source in UJP Praha (Czech Republic).

It has been verified, that the surface radiation damage does not influence the sensor stability. The breakdown voltage is well above the maximum operational voltage. All the tested surface parameters, such as the interstrip resistance and capacitance, coupling capacitance and bias resistance satisfy the ATLAS ITk specifications for strip sensors.

### Submission declaration

Original and unpublished

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**Session Classification:** Session8

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 247

Type: ORAL

## Results of the TIMESPOT project on sensors and electronics developments for future vertex detectors

*Wednesday, December 18, 2019 11:40 AM (20 minutes)*

The TIMESPOT project aims at the construction of a mini-tracker demonstrator implementing both high space and time resolutions at the single pixel level. The pixels have a pitch of  $55 \times 55 \mu\text{m}^2$ . Specified r.m.s. time resolution is equal or better than 50 ps.

Sensors are based both on 3D silicon and diamond technologies, whose layout and fabrication process have been suitably optimized for best time resolution. Read-out pixel electronics is developed in 28-nm CMOS technology. The single pixel circuit contains one charge sensitive amplifier, one discriminator and one TDC per pixel.

The first batch of 3D silicon sensors, containing several test structures based on different geometries of the electrodes, has been delivered in June 2019 and is currently under characterization and tests. Among the different structures being tested and compared, a high density trench-type layout has been realized, being particularly promising about timing performance.

I-V curves show a general good behavior of the sensors. Dynamic tests using a pulsed laser beam have evaluated the sensor performance in terms of charge collection efficiency and timing.

A first prototype of 3D column-type diamond sensor with optimized timing performance has been also realized and tested with encouraging results.

The first prototype of the 28-nm CMOS ASIC has been delivered in Spring 2019 and is under test. One of the important results is the feasibility of integrating a high performance TDC (about 20 ps r.m.s. time resolution) inside a total pixel circuit area of  $55 \times 55 \mu\text{m}^2$ .

In the present paper, the output of measurements on sensor and readout electronics tests will be presented. They represent an important step forward in the development of pixels with timing operating at extremely high interaction rates and fluences, as required in the next generation of upgraded colliders.

### Submission declaration

Original and unpublished

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**Presenter:** LAI, Adriano (Universita e INFN, Cagliari (IT))

**Session Classification:** Session12

**Track Classification:** New ideas and future applications

Contribution ID: 248

Type: POSTER

## FAST: a 30 ps time resolution front-end ASIC for a 4D tracking system based on Ultra-Fast Silicon Detectors

*Saturday, December 14, 2019 2:45 PM (1 minute)*

The UFSD group of Turin is working at the development of custom front-end electronics for the read-out of thin silicon sensors with moderate internal gain (the so called Ultra-Fast Silicon Detectors- UFSD), aiming at applications that require very precise time tagging. The activity of the group is mainly focused on meeting the requirements of the next generation of HEP colliders where the main role is played by the LHC High-Luminosity upgrade, with the expected challenging pile-up factor of 150-200 events per bunch crossing. In this context, time tagging is one of the fundamental tools which can be exploited to distinguish events overlapping in space but separated in time by a few tens of pico-seconds: both ATLAS, with the High Granularity Timing Detector and CMS, with the MIP Timing Detectors, are pursuing time tagging projects with a 30 ps time resolution.

The measurement of the Time of Arrival of a particle is affected by uncertainties coming both from the sensor used to detect particles and from the readout electronics used to measure the weak signals generated by the sensor. In order to increase the time resolution, signals with high amplitudes and small rising time are key points. In this context, UFSD sensors are proposed as a good candidate for time measurements, due to their capability to generate signals with the properties listed above. For what concerns the contribution of the readout electronics, the slew rate and the front-end noise are mainly influencing the timing performances.

In this paper we present **FAST**, a 20 channels novel low power front-end electronics for UFSD, devoted to timing resolution with a **jitter lower than the 30 ps** target. In order to map different solutions, we designed three flavors of FAST differing in the amplification stages and component-level technical choices. During the design phase, extensive simulation considered the intrinsic sensor signal shaping, including radiation damage effects.

The ASIC tape-out is foreseen for September 2019 and on-silicon characterization results will be shown at the conference.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** ASICs



Contribution ID: 249

Type: POSTER

## First demonstration of real-time in-situ dosimetry of x-ray microbeams using a large format CMOS sensor

*Saturday, December 14, 2019 3:19 PM (1 minute)*

Microbeam radiotherapy is a novel type of radiotherapy in which narrow beams of radiation (typically less than 500  $\mu\text{m}$ ) are spatially fractionated, delivering a non-uniform distribution to the target tumour volume. Due to the very high dose gradients involved, new dosimetric techniques are required for translation into clinical practise. Current real-time beam monitoring is typically performed using 1 dimensional silicon strip detectors or wire chambers, with 2D beam information measured offline using radiochromic film (requiring a minimum of 24 hours to self-develop).

Using a bespoke x-ray microbeam generator at the Technical University of Munich, Germany, the newly developed vM1212 detector was exposed to a variety of microbeams (220 kV, nominal slit widths 0 - 100  $\mu\text{m}$ ) for evaluation for in-vivo real time verification. The sensor evaluated is a large format CMOS sensor with a 50  $\mu\text{m}$  pixel pitch and an active area of approximately 6 x 6  $\text{cm}^2$ , and was chosen for the investigation due to its predicted radiation tolerance and high spatial resolution. 1 cm of water equivalent bolus build-up was placed on top of the sensor to make the results clinically relevant for comparison with other measurement techniques.

The vM1212 detector was assessed by changing the collimator slit width (and thus microbeam FWHM) mid-irradiation. For each frame that was captured, a Python script identified each of the fifty-one microbeam peaks, allowing a Gaussian function to be fitted in order to extract the relevant beam parameters. Microbeam FWHMs of 130 - 190  $\mu\text{m}$  could be measured in this manner in addition to temporally monitoring other basic parameters such as the radiation intensity. More advanced parameters could be calculated as the tungsten slits within the microbeam collimator opened and closed such as the rate of change of FWHM; the peak-valley-dose-ratio (PVDR); and the sub-pixel movement of each microbeam peak.

This work demonstrates the potential of radiation hard CMOS sensors for 2D in-vivo real-time monitoring of FWHM, intensity and position in x-ray microbeam radiotherapy.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Applications in biology, medicine, medical equipments

Contribution ID: 250

Type: POSTER

## Comparative characterisation of nitrogen doped highly irradiated silicon sensors

*Saturday, December 14, 2019 3:01 PM (1 minute)*

Envisaged circular hadron colliders challenge the existing silicon detector technologies in terms of unprecedented radiation doses and set stringent limits on the resolution and the material budget. Since 2002 the RD50 Collaboration is dedicated to the development of radiation tolerant silicon detectors for high energy collider experiments. One promising approach for more radiation hard silicon sensors is the so-called defect engineering, where foreign atoms are introduced to the silicon bulk material, to alter the defect formations after irradiation. Previous investigations of nitrogen enriched material indicated a superior radiation tolerance.

The NitroStrip project is a common RD50 effort to investigate the effect of nitrogen doping on silicon strip sensors in comparative measurements. For this purpose sensors and diodes were produced from standard floatzone, deep oxygenated, Magnetic Czochralski and nitrogen enriched wafers.

Within this presentation, an overview on the various results obtained from the measurement campaign is given. The devices were electrically tested and irradiated to fluences between  $1 \cdot 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2$  and  $1 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$  with either protons at Karlsruhe, 23 MeV/c, and CERN PS, 24 GeV/c, or reactor neutrons in Ljubljana. The sensor behaviour after irradiation was then evaluated in terms of their charge collection using a beta source, measurements of the electric field distribution using an edge- and top-Transient Current Technique (TCT) setup, electrical measurements and measurements of the thermally stimulated currents (TSC) for defect characterisation. For a thorough understanding of the long term behaviour of the nitrogen enriched sensors, dedicated annealing studies were performed with annealing times corresponding to more than a year at room temperature. The various measurements of the irradiated sensors revealed no superior radiation hardness of the nitrogen enriched sensors. Hence additional SIMS measurements were performed, which concluded that the level of nitrogen in the processed sensors is below the detection limit. This indicates that the nitrogen content of the wafer is reduced during the sensor processing, which is currently under further investigation.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 252

Type: ORAL

# Commissioning of the upgraded ALICE Inner Tracking System

*Sunday, December 15, 2019 10:00 AM (20 minutes)*

Svetlana Kushpil on behalf of the ALICE Collaboration

The ALICE Inner Tracking System detector is undergoing a major upgrade in order to cope with the increased data rates and to meet the requirements as set out by the physics goals of the experiment after Long Shutdown 2. The new ITS will be completely made up of monolithic active pixel sensors based on a CMOS 180nm process. A single sensor measures 15mm x 30mm and contains half a million pixels distributed over 512 rows and 1024 columns. These 50um thick sensors, with 27um x 29um pixel pitch, are mounted on ultra-lightweight carbon composite support structures with an embedded cooling system. This results in a considerable reduction of the material budget (down to 0.35%  $X_0$  for the inner layers and ~1%  $X_0$  for the outer layers) and a significant improvement of the impact parameter resolution and tracking efficiency. The innermost ITS layer will be moved as close as 23mm to the interaction point. The integration of the ITS detector assembly, made of the three innermost and four outermost layers, has been almost completed and the commissioning, first in the laboratory, is ongoing. The detector will be installed in ALICE in 2020. This talk will give a brief overview of the motivation for the upgrade and will present the first results of the detector performance obtained during the commissioning.

## Submission declaration

Original and unpublished

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**Session Classification:** Session1

**Track Classification:** Pixel sensors for tracking

Contribution ID: 253

Type: POSTER

## The TSV Processing of the Hybrid Pixel Detector for the High Energy Photon Source

*Saturday, December 14, 2019 2:05 PM (1 minute)*

HEPS-BPIX3 is the third prototype of single-photon counting pixel detector with 1.4 million pixels developed for applications of synchrotron light sources. It follows the first prototype, HEPS-BPIX, with a pixel size of 150  $\mu\text{m}$  x 150  $\mu\text{m}$  and frame rate up to 1.2 kHz at 20-bit dynamic range. To reduce the insensitive gap between modules, we start to upgrade it with the through silicon via (TSV) processing to replace the wire bonding. The TSV processing drills the via at the pad, and makes connection between the front and back sides of the read-out chip. The redistribution layer (RDL) and bump bonding are performed at the bottom of read-out chip to connect the control, readout signals and power supplies to the PCB. The insensitive area is reduced from 26.3% to 12.7%. We have tested the modules with X-ray and synchrotron radiation light, and read-out chip can be operated electrically through the TSV without any performance degradation.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Technologies

Contribution ID: 254

Type: ORAL

## Characteristics of silicon strip sensors irradiated up to proton fluence of $10^{17}$ n<sub>eq</sub>/cm<sup>2</sup>

*Tuesday, December 17, 2019 3:40 PM (20 minutes)*

Silicon semiconductor detector technology has been adopted by the experiments at the high-luminosity upgrade of the CERN Large Hadron Collider (HL-LHC) to perform precision tracking in the inner region surrounding the collision point where the traversing particle fluence will reach  $1 \times 10^{16}$  1-MeV n<sub>eq</sub>/cm<sup>2</sup>. Hadron colliders in future should provide even larger luminosity for rare physics searches and the detector needs to be more radiation hard. The n<sup>+</sup>-in-p microstrip detectors developed for the HL-LHC and fabricated by Hamamatsu Photonics were irradiated by 70-MeV protons up to fluence of  $10^{17}$  n<sub>eq</sub>/cm<sup>2</sup> and the changes in basic strip detector characteristics have been evaluated to investigate the impacts on the silicon detector designing for the future experiments. The characterization was conducted based on the methods developed for the ATLAS ITk strip sensor characterization. The charge collection measured with penetrating <sup>90</sup>Sr X-rays and fast ALIBAVA readout system is severely degraded above  $10^{16}$  n<sub>eq</sub>/cm<sup>2</sup>, as reported previously. The interstrip capacitance and aluminum strip resistance are barely influenced, while the poly-silicon bias resistance showed to increase gradually with the fluence and the implant strip resistance to increase at  $10^{17}$  n<sub>eq</sub>/cm<sup>2</sup>. The punch-through protection is found to be degraded but its functionality is sustained to occur below 100 V as required even at  $10^{17}$  n<sub>eq</sub>/cm<sup>2</sup>. The presentation will cover these measurement results.

### Submission declaration

Original and unpublished

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**Presenter:** SATO, Katsuya (University of Tsukuba (JP))

**Session Classification:** Session9

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 255

Type: POSTER

## A 12-Channel 120 Gbps Optical Transmitter in 55 nm CMOS for High-Energy Physics Experiments

*Saturday, December 14, 2019 2:46 PM (1 minute)*

VCSEL-based array optical data transmission system has been prevalingly researched and developed for the front-end data acquisition in high-energy physics experiments with advantages in density, data throughput, power consumption and radiation performance. This paper presents the design and test results of a 12-channel 12 x 10 Gbps VCSEL driving ASIC fabricated in 55nm CMOS technology. Each channel in the driver consists of an input equalizer stage, a pre-driver (limiting amplifier) stage and an output driver stage. The equalizer stage adopts a 4-step adjustable CTLE structure to compensate the high frequency losses from the system level including PCB traces and bonding wires. The pre-driver stage uses the passive shared inductor technique to obtain sufficient bandwidth (16.5 dB, 8.3 GHz) in a limited area (212  $\mu\text{m}$  x 235 $\mu\text{m}$ ). The output driver stage employs both the programmable R-C degradation pre-emphasis structure and the feed-forward capacitor to improve the bandwidth. All 12 channels can be controlled independently by the I2C module, which is strengthened with the Triple Modular Redundancy (TMR) structure.

The driving ASIC features a size of 1450  $\mu\text{m}$  x 4000  $\mu\text{m}$  with 74 pads. The chip has been wire bonded on the test board, and a full 12-channel electrical test has been conducted. Widely-open 10-Gbps eyes have been captured for all 12 channels at the typical settings of 2 mA bias current and 5 mA modulation current. The deterministic jitter (DJ) of the captured 10-Gbps eye is 12.9 ps, the random jitter (RJ) is 870 fs (rms), and the total jitter is 25.1 ps at a bit error rate of 1E-12. The tested power consumption of the chip is 32.5 mW/ch when working at 10 Gbps/ch. The full channel test results will be reported in the meeting.

### Submission declaration

Original and unpublished

**Primary authors:** Dr ZHAO, Cong (Central China Normal University); Dr GUO, Di (Southern Methodist University); Dr SUN, Hanhan (Central China Normal University); Prof. HUANG, Guangming (Central China Normal University); Prof. SUN, Xiangming (Central China Normal University); Dr XIAO, Le (Central China Normal University); Dr ZHANG, Wei (Central China Normal University); Dr ZHOU, Wei (Central China Normal University)

**Presenter:** Dr GUO, Di (Southern Methodist University)

**Session Classification:** POSTER

**Track Classification:** ASICs



Contribution ID: 256

Type: POSTER

## Use of a monolithic SOI pixel detector to study rolling contact fatigue of railway rails

*Saturday, December 14, 2019 2:07 PM (1 minute)*

In this study, a silicon-on-insulator (SOI) pixel detector was used to evaluate the fatigue damage of railway rails. For this purpose, the SOI pixel detector detected diffracted  $\text{CrK}\alpha$  X-rays from a sample of a rail. Part of the Debye ring generated by the diffracted X-ray beams was obtained and was then analysed by using the principle of the X-ray stress analysis method. The rail from which the sample was taken had been used in service on a commuter line in Japan for about seven years. Fatigue cracks formed on the rail head. Tri-axial residual stress state and the full width at half maximum (FWHM) of the rail head were determined by the  $\cos\alpha$  method. The results of the experiment clearly showed the mapping results of the actual state on the rail head in terms of the formation of residual tri-axial stresses and white etching layers.

This research was undertaken because the risk of rail failures generally depends on defects in the rail material. Such defects form and grow due to the repeated loading of wheels of passing trains. The formation and growth of the defects are mainly influenced by bending stress, contact stress, thermal stress, and residual stress. Although residual stress in rails has been studied by X-ray and neutron methods, the effect of residual stress at the surface of the rail head has not been revealed in detail. In this study, to analyse the residual stress at the rail head in a wider area in detail, X-ray stress analysis was conducted by using a SOI pixel detector, and then data was quickly acquired. The application of a SOI pixel detector to X-ray stress analysis will be contributed to studying on the rolling contact fatigue of rails.

Keywords: SOI pixel detector, Debye ring, strain, residual stress, railway rail, rolling contact fatigue.

### Submission declaration

Original and unpublished

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**Presenter:** Prof. SASAKI, Toshihiko (Kanazawa University)

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for imaging

Contribution ID: 257

Type: POSTER

## Monolithic CMOS sensors for sub-nanosecond timing

*Saturday, December 14, 2019 2:25 PM (1 minute)*

In the ATTRACT project FASTPIX we investigate monolithic pixel sensors with small collection electrodes in CMOS technologies for fast signal collection and precise timing in the sub-nanosecond range.

Deep submicron CMOS technologies allow tiny, sub-femtofarad collection electrodes, and large signal-to-noise ratios, essential for very precise timing. However, complex in-pixel circuits require some area, and one of the key limitations for precise timing is the longer drift time of signal charge generated near the pixel borders. Laying out the collection electrodes on a hexagonal grid and reducing the pixel pitch minimize the maximum distance from the pixel border to the collection electrode. The electric field optimized with TCAD simulations pulls the signal charge away from the pixel border towards the collection electrode as fast as possible. This also reduces charge sharing and maximizes the seed pixel signal hence reducing time-walk effects. Here the hexagonal geometry also contributes by limiting charge sharing at the pixel corners to only three pixels instead of four. We reach pixel pitches down to about 8.7 micron between collection electrodes in this 180 nm technology by placing only a minimum amount of circuitry with the pixel and the rest at the matrix periphery.

Consuming several tens of micro-ampere per pixel from a 1.8 V supply offers a time jitter of only a few tens of picoseconds. This allows detailed characterization of the sensor timing performance in a prototype chip with several mini-matrices of 64 pixels each with amplifier, comparator and digital readout and some additional pixels with analog buffers. The aim is to prove sensor concepts before moving to a much finer line width technology and fully integrate the readout within the pixel at lower power consumption.

The paper will present detailed TCAD simulation results and give an overview of the test chip with an outlook on finer line-width technologies. The development of a pyramidal structure micro-machined in silicon to further accelerate the charge collection and the time resolution of the sensor will also be presented.

### Submission declaration

Original and unpublished

**Primary author:** KUGATHASAN, Thanushan (CERN)

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**Presenters:** KUGATHASAN, Thanushan (CERN); Prof. ETOH, Takeharu (Ritsumeikan University)

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for tracking

Contribution ID: 258

Type: POSTER

## Highly compact digital pixel structures developed for the CEPC vertex detector

*Saturday, December 14, 2019 2:22 PM (1 minute)*

The proposed CEPC (Circular Electron Positron Collider) will offer the measurements of the Higgs properties with a new level of precision. The precise determination of the charged particle tracks and reconstruction of the primary and displaced decay vertices, impose stringent requirements on the CEPC vertex detector, which somehow incompatible with each other, such as high spatial resolution ( $<3\mu\text{m}$ ), low power consumption ( $<50\text{mW}/\text{cm}^2$ ) and fast processing speed ( $<10\mu\text{s}/\text{frame}$ ). CMOS pixel sensor with pixel-level discrimination represents one of the most promising candidates. However, the complexity of the in-pixel digital circuit always leads to increased pixel size, which is disfavored to obtain high spatial resolution.

In this context, we propose two pixel-structures with a balance between high precision and circuit simplicity to guarantee compact pixels, yet with satisfying high signal over noise ratio. Both of the two structures are based on the DMAPS (Depleted Monolithic Active Pixel Sensors) concept, employ a high-voltage (up to 10 V) biased charge collection diode, AC-coupled with a comparator with OOS (Output Offset Storage) technique to mitigate pixel-to-pixel performance dispersion. The main difference between the two structures concentrates on the signal amplification stage used in the comparator.

In order to verify the idea, a prototype named JadePix-2 which contains  $112\times 96$  pixels has been designed and fabricated with a  $0.18\mu\text{m}$  CMOS Image Sensor process. Both of the two structures have been realized within  $22\mu\text{m}$  pixel pitch size. JadePix-2 operates in the rolling-shutter mode, with processing speeds of  $100\text{ns}/\text{row}$  and  $80\text{ns}/\text{row}$ , respectively, for the two structures.

Experimental results show the total ENC of the two structures are about 29 e- and 31 e- respectively. More test results and design optimization details will be presented.

### Submission declaration

Original and unpublished

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**Presenter:** Dr ZHOU, Yang (Institute of High Energy Physics, CAS, Beijing, China)

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for tracking

Contribution ID: 259

Type: ORAL

## ATLAS ITk Pixel Detector Overview

*Sunday, December 15, 2019 11:20 AM (20 minutes)*

For the high luminosity era of the Large Hadron Collider (HL-LHC) it is foreseen to replace the current Inner Detector of the ATLAS experiment with a new, all-silicon detector to cope with the increase in occupancy, bandwidth and radiation damage that result from the increase of the instantaneous luminosity by a factor of 5 to 7.5. The new Inner Tracker (ITk) will consist of an inner pixel and outer strip detector aiming to provide tracking coverage up to  $|\eta|=4$ . The layout of the pixel detector is foreseen to have five layers of pixel silicon sensor modules in the central region and several ring-shaped layers in the forward region. This results in up to 14 m<sup>2</sup> of silicon depending on the selected layout.

While the outer 3 layers of the Pixel Detector are designed to operate for the full HL-LHC data taking period, the innermost 2 layers of the detector will be replaced around half of the lifetime. The innermost layer of the ITk Pixel Detector will feature 3D silicon sensors, due to their inherent radiation hardness and low power consumption, while the remaining layers will employ planar silicon sensors with thickness ranging from 100 $\mu$ m to 150 $\mu$ m. All hybrid detector modules will be read out by novel ASICs, implemented in 65nm CMOS technology, which will be connected to the silicon sensors using bump bonding. With about 4 $\cdot$ 10<sup>4</sup> pixels per cm<sup>2</sup> the bump bond density is a much higher than in previous hybrid detectors.

In order to reduce the amount of services needed, a serial powering scheme for the detector modules will be adopted. The pixel off-detector readout electronics will be implemented in the framework of the general ATLAS trigger and DAQ system with a readout speed of up to 5 Gb/s per data link for the innermost layers.

The talk will give an overview of the layout and current status of the development of the ITk Pixel Detector.

### Submission declaration

Redundant (overlaps with already published)

**Primary authors:** WEINGARTEN, Jens (Technische Universitaet Dortmund (DE)); BUTTAR, Craig (University of Glasgow (GB))

**Presenter:** BUTTAR, Craig (University of Glasgow (GB))

**Session Classification:** Session2

**Track Classification:** Pixel sensors for tracking

Contribution ID: 260

Type: POSTER

## Measurement results on Capacitively Coupled Particle Detector with 25 $\mu\text{m}$ x 50 $\mu\text{m}$ pixel size and 50 $\mu\text{m}$ Pad pitch

*Saturday, December 14, 2019 2:26 PM (1 minute)*

A sensor chip for a capacitively coupled particle detector (CCPD53) has been designed and produced in a 180 nm high voltage CMOS (HVCMOS) technology on a high resistivity wafer with deep p-well option. Capacitively coupled detectors are simple and low cost alternative to classical hybrid detectors and it can be used for several particle physics experiments.

The CCPD53 sensor chip contains a pixel matrix of 64 x 40 pixels, each has 25  $\mu\text{m}$  x 50  $\mu\text{m}$  in size. The digital output signals of the pixels are multiplexed to pads of 50  $\mu\text{m}$  x 50  $\mu\text{m}$  size. Using special address encoding a group of 16 pixels is connected to 8 transmitting electrodes. The pad geometry has been chosen so that it fits to the geometry of the pixel readout ASIC developed by RD53 collaboration at CERN. Via small number of large bumps the sensor chip CCPD53 and the readout chip can be mechanically connected together. The bumps can be also used for powering and configuring of the sensor chip. The digital pixel output signals have large amplitudes (1.8 V) and they are transmitted over the chip-chip gap via capacitive coupling.

The standalone CCPD53 chip tests with the injection circuit and Fe55 source, as well as the measurements on the CCPD53 chip that is attached to a readout chip have been performed. Several new measurements are planned, such as irradiations with beta sources and x-rays and investigations of capacitive coupling in the case of large chip to chip distance. In this contribution the sensor and the readout chip will be described and measurement results will be presented.

Key words: Capacitively Coupled Particle Detector, CCPD, HVCMOS Detector, Hybrid Pixel Detector

### Submission declaration

Original and unpublished

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**Presenter:** ZHANG, Hui (Karlsruhe Institute of Technology (KIT))

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for tracking

Contribution ID: 261

Type: POSTER

# Initial Tests of Large Format Sensors for the ATLAS ITk Strip Tracker

*Saturday, December 14, 2019 2:34 PM (1 minute)*

For the production of the Inner Tracker (ITk) as part of the phase-II upgrade programme to prepare the ATLAS experiment for the High-Luminosity (HL) LHC, batches of Long Strip (LS) and Short Strip (SS)  $n$ -in- $p$  type micro-strip sensors have been produced by Hamamatsu Photonics.

The full size sensors measure approximately  $98 \times 98 \text{ mm}^2$  and are designed and engineered for tolerance against the  $9.7 \cdot 10^{14}$ , including a safety factor of 1.5,  $1 \text{ MeV n}_{eq}/\text{cm}^2$  fluence expected at the HL-LHC. Each sensor has 2 or 4 columns of 1280 individual channels arranged at  $75.5 \mu\text{m}$  horizontal pitch.

To ensure the sensors comply with their specifications, a Quality Control (QC) procedure has been designed, comprising measurements on every individual sensor as well as on a sample basis. Every sensor is subjected to an initial visual inspection, after which the full surface of the sensor is captured with very high resolution by an automated camera setup. Non-contact metrology is performed to obtain the sensor surface profile.

Electrical measurements establishing the reverse bias leakage current and depletion voltage are conducted automatically, with the recorded results uploaded to a production database following data quality checks.

Sample sensors from every batch are subjected to 40 hour leakage stability checks in controlled atmosphere, and tests on every channel measuring leakage current, coupling capacitance and bias resistance are conducted.

In this paper, QC test validation data and the compiled results for the first batches of production grade sensors, consisting of approximately 30 LS and SS sensors each are presented. Data from multiple test sites are compared with the data provided by Hamamatsu Photonics where possible.

The QC protocol was validated, and the results of the first production sensors were confirmed to be within specification.

## Submission declaration

Original and unpublished

**Primary authors:** HOMMELS, Bart (University of Cambridge (GB)); KOFFAS, Thomas (Carleton University (CA))

**Presenter:** KLEIN, Christoph Thomas (University of Cambridge (GB))

**Session Classification:** POSTER

**Track Classification:** Strip sensors

Contribution ID: 262

Type: POSTER

## A 12-Channel 120-Gb/s Optical Receiver Array in a 55 nm CMOS technology for High-Energy Physics Experiments

*Saturday, December 14, 2019 2:47 PM (1 minute)*

Optical data transmission, characterized by high data rate capacity, low power consumption and space saving, has been extensively used in the detector readout electronics in high-energy physics (HEP) experiments. The photodiode (PD)-based optical receiver array is a key component to build paralleled optical links at the receiving end. The light traveling through a fiber experiences optical power loss before reaching a photodiode. Each channel of an optical receiver array consists of a transimpedance amplifier (TIA) and a few limiting amplifier (LA) stages and aims at converting the small optical current in the photodiode to a voltage and further amplifying it.

This paper presents the design and measurements of a 12-channel 120-Gb/s optical receiver array ASIC fabricated in a standard 55-nm CMOS technology. A pseudo-differential CMOS push-pull TIA with resistive feedback is utilized to provide common-mode noise rejection and improve jitter performance. A novel three-order active feedback strategy is employed in five LA stages to expand the bandwidth and optimize the gain performance. The shared-inductor peaking and RC degeneration techniques are used to further improve the bandwidth. The single channel of the optical receiver array exhibits a total gain of 89.4 dB $\Omega$  with a bandwidth of 7.5 GHz.

The whole chip occupies 1.4 mm  $\times$  4 mm and consumes 672 mW with all 12 channels enabled. Wide-open eyes diagrams are recorded and a bit error rate (BER) of less than 1E-12 is achieved at 10 Gbps/ch. Random jitter (RJ) is 1.16 ps (RMS), deterministic jitter (DJ) is 10.1 ps (peak-to-peak) and total jitter is 26.8 ps. All channels demonstrate similar performance. The measurements indicate that we achieve our design goal.

### Submission declaration

Original and unpublished

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**Presenter:** Dr CHEN, Chufeng (Central China Normal University)

**Session Classification:** POSTER

**Track Classification:** ASICs



Contribution ID: 263

Type: POSTER

## JICG CMOS Transistors for Reduction of Total Ionizing Dose and Single Event Effects in a 130nm bulk SiGe BiCMOS technology

*Saturday, December 14, 2019 2:48 PM (1 minute)*

We report on the mitigation of TID and SEE induced malfunctions for digital circuits fabricated in a 130 nm bulk SiGe BiCMOS technology using a novel RHBD approach. To avoid an increase of drain leakage for NMOS transistors and channel pinch-off for PMOS transistors due to trapped fixed positive charges at the lateral Shallow Trench Silicon interface we introduced a lateral junction isolation (JI) of the MOS transistors instead of shallow trench isolation (STI). To suppress SEE induced malfunctions in CMOS circuits as a result of generated electron hole pairs after an high energy particle impact we have introduced a redundancy on transistor level combined with suitable device construction measures which ensures that the CMOS output node remains its signal integrity. The constructive measures applied result in a JICG CMOS arrangement (Junction Isolated Common Gate) as a basic element for digital circuits suitable for applications in harsh radiation environments. The redundancy on transistor level in logical CMOS gates is achieved by splitting each NMOS and PMOS block into a series connection of two spatially distributed low side and high side blocks which share common gates (CG). The radiation tolerance of the JICG CMOS circuits designed were tested using a gamma source up to TIDs > 1.3 Mrad(Si) and SEE tests were performed at a heavy ion accelerator with LET values > 100 MeVcm<sup>2</sup> mg<sup>-1</sup> (LET:linear energy transfer). The penalties for the substantially increased radiation tolerance of the JICG CMOS gates as an increased chip area and a reduced digital switching speed will be discussed.

### Submission declaration

Original and unpublished

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**Presenter:** Dr SORGE, Roland (IHP)

**Session Classification:** POSTER

**Track Classification:** ASICs

Contribution ID: 264

Type: POSTER

## Quality Assurance Methodology for the ATLAS ITk Strip Sensor Production

*Saturday, December 14, 2019 2:37 PM (1 minute)*

The production of the strip sensors for the ATLAS Inner Tracker (ITk) will start in 2020. Nearly 22000 large area sensors will be produced over a period of roughly 4 years. The Institutes involved in the sensor development and production are committed to deliver and maintain the highest quality sensors for the experiment. A Quality Assurance (QA) strategy has been prepared to be carried out during the whole production period. Once the process has been characterized as providing the required pre-irradiation specifications and the proper radiation hardness, the onus is on the manufacturer to rigidly stick to that qualified process. Still, sample testing with specific device-element structures and irradiation of devices should be implemented by the ITk Groups.

The main devices that will be used by the collaboration for QA purposes are the miniature strip sensors, strip sensors with the same design as the MAIN sensor but with 1cm×1cm dimensions; the monitor diodes, 8mm×8mm pad diodes with contactable guard ring; and the ATLAS test chip. The ATLAS test chip contains several test structures to test specific device-element parameters. It includes a structure with bias resistors; a CBR (Cross-Bridge Resistor) structure, which allows a precise measurement of the sheet resistance; square coupling capacitances and field oxide capacitors for precise measurements of critical parameters for the device oxides such as capacitance, thickness, breakdown voltage, flat-band voltage, etc.; gated diodes, diodes with a gate implemented in order to evaluate the Si/SiO<sub>2</sub> interfaces; and specific structures to monitor the strip and inter-strip characteristics, such as strip-like structures or interdigitated structures.

The irradiations will be carried out on a sample basis. In order to have a practical methodology, samples from odd or even batches will be sent for different irradiations. A detailed description of the production flow, the periodic irradiations, and the different tests planned during production will be provided. Example measurements from the prototype batches will be shown and their results analyzed.

### Submission declaration

Original and unpublished

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**Presenter:** ULLAN COMES, Miguel (CNM-Barcelona (ES))

**Session Classification:** POSTER

**Track Classification:** Large scale applications

Contribution ID: 265

Type: POSTER

## Development of monolithic SOI pixel sensors capable of fine measurements of space and time

*Saturday, December 14, 2019 2:08 PM (1 minute)*

Keywords: SOI monolithic pixel, SOFIST, 3D

We are developing a monolithic pixel sensor SOFIST using a 0.2  $\mu\text{m}$  FD-SOI (Fully depleted silicon-on-insulator) technology for the ILC vertex detector. Adopted is a double SOI wafer manufacturing technology that two buried oxide layers are formed on a high resistive sensor wafer and MOSFETs are formed thereon. Advantages such as low noise due to small parasitic capacitance, small sensor material and radiation resistance against SEE are realized as an SOI monolithic sensor. Superior radiation resistance against TID of  $\sim 1\text{MGy}$  has also been demonstrated.

SOFIST (SOi Fine measurement of Space and Time) is designed to record information of the charge and time of the hit pixels, and we aim to achieve 3  $\mu\text{m}$  position resolution and identify ultimately the ILC beam bunches of 554 ns separation. In the previous study, we have demonstrated that SOFIST ver.1 achieved an intrinsic position resolution of 1.2-1.4  $\mu\text{m}$  for pixel size of  $20\times 20$   $\mu\text{m}$  depending on the depletion depths and 8-bit column ADC or 12-bit external ADCs. Also, SOFIST-v2 that has implemented a circuit to record the time achieved a time resolution of 1.55  $\mu\text{s}$  using a ramping voltage range of 0-1 V corresponding to a time interval of 0-0.5 ms.

In this presentation, we report the SOFIST-v3 performance evaluated using 120 GeV proton beam, reading multi-hit, and the status of SOFIST-v4 development. SOFIST-v3 includes the full circuits to read out the charge and time in each pixel of  $30\times 30$   $\mu\text{m}$  pixel size. Additionally, it was also implemented multi-memory that enable to read out multi-hit. The same functionality is to be realized in SOFIST-v4 with  $20\times 20$   $\mu\text{m}$  pixel size where the circuits implemented separately in two chips are stacked three-dimensionally using Au micro-bumps.

### Submission declaration

Original and unpublished

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**Presenter:** MURAYAMA, Hitoshi (University of Tsukuba )

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for imaging

Contribution ID: 266

Type: ORAL

## 1.28 and 5.12 Gbps multi-channel twinax cable receiver ASICs for the ATLAS Inner Tracker Pixel Detector Upgrade

*Tuesday, December 17, 2019 5:40 PM (20 minutes)*

We present two prototypes of a gigabit transceiver ASIC, GBCR, in a 65-nm CMOS technology for the ATLAS Inner Tracker Pixel readout upgrade.

The first prototype has four upstream receiver channels and a downstream transmitter channel. Each upstream channel receives the data at 5.12 Gbps through a 5-meter 34-AWG twin-axial cable from another ASIC called Aggregator and drives the optical transmitter in a VTRx+. The upstream channels consist of an equalizer, a DFE module (only in the 4th channel), a CDR, and an output driver. The downstream channel receives the data at 2.56 Gbps from an optical receiver of the VTRx+ and drives a receiver of the Aggregator through a cable of the same type. The test results indicate that the prototype chip works as expected except that the test of the DFE module is still ongoing. For an upstream channel, the total jitter (peak-peak) is 72.7 ps when the CDR is off and decreases to 35.4 ps when the CDR is on. The chip consumed 318 mW when the CDR is on. A TID test has been begun and will be completed in early September. A SEE test will be performed in the future.

The second prototype has seven upstream channels and each channel works at 1.28 Gbps to recover the data directly from the RD53 driver through a cable of 1-m flex and 6-m Twinax. Each channel consists of an equalizer, a retiming logic, a limiting amplifier, and an output driver. The retiming clock is provided by a phase shifter. From the post-layout simulation results, the additional jitter of the output signal is about 80 ps (peak-peak) when the retiming logic is off. When the retiming logic is on, the total jitter is estimated to be 50 ps. The entire chip consumes about 150 mW when the retiming logic is off. The design will be submitted by the end of October 2019.

### Submission declaration

Original and unpublished

**Primary authors:** Mr CHEN, Chufeng (SMU); Ms WALLANGEN, Veronica (Lawrence Berkeley National Lab. (US)); Mr GONG, Datao (Department of Physics, Southern Methodist University); GRACE, Carl (Lawrence Berkeley National Laboratory); Mr SUN, Quan (Southern Methodist University (US)); Dr GUO, Di (Southern Methodist University); HOU, Suen (Inst. of Physics, AS); Prof. HUANG, Guangming (Central China Normal University, China); KULIS, Szymon (CERN); Prof. LEROUX, Paul (KU Leuven (BE)); LIU, Chonghan (Southern Methodist University); LIU, Tiankuan (Southern Methodist University (US)); RODRIGUES SIMOES MOREIRA, Paulo (CERN); PRINZIE, Jeffrey (KU Leuven (BE)); WANG, Peilong (Southern Methodist University (US)); XIAO, Le (Central China Normal University, China); Mr YE, Jingbo (Department of Physics, Southern Methodist University)

**Presenter:** GONG, Datao (Southern Methodist University (US))

**Session Classification:** Session10

**Track Classification:** ASICs

Contribution ID: 267

Type: **ORAL**

## The Phase 2 upgrade of CMS Inner Tracker

*Sunday, December 15, 2019 10:20 AM (20 minutes)*

A new Silicon Tracker will be built for the Phase 2 Upgrade of the CMS experiment to fully exploit the increased luminosity delivered by HL-LHC. The innermost part, called the Inner Tracker, will be exposed to extreme conditions such as unprecedented radiation levels of 1.2 Grad and  $2E16$  neq/cm<sup>2</sup> and hit rates of 3.2 GHz/cm<sup>2</sup>. The new Inner Tracker relies on many novel solutions and technologies that allow for a design of a light and radiation-hard pixel detector of high performance. The hybrid pixel modules will be composed of pixel sensors with pixel size of 2500  $\mu\text{m}^2$  and new ASIC, designed in 65 nm CMOS technology, developed by the RD53 collaboration. A novel scheme of serial powering will be deployed to power the pixel modules and new technologies will be used for a high bandwidth readout system. The mechanics will be lightweight, based on carbon-fibre material and two-phase CO<sub>2</sub> cooling. In this contribution, the design of the CMS Inner Tracker system will be presented along with the prospective design choices.

### Submission declaration

Original and unpublished

**Primary author:** ORFANELLI, Stella (CERN)**Presenter:** ORFANELLI, Stella (CERN)**Session Classification:** Session1**Track Classification:** Large scale applications

Contribution ID: 269

Type: ORAL

## 64-channel photon-counting computed tomography using a new ceramic multi-pixel photon counter

*Sunday, December 15, 2019 4:40 PM (20 minutes)*

X-ray computed tomography (CT) is a widely used diagnostic tool. However, the exposure dose of conventional CT in a single scan is large, typically 10 mSv, and therefore, reducing the radiation dose is a problem to be solved. Furthermore, conventional CT does not have the energy information of individual X-ray photon because the read out is an integrated pulse signal. Hence, it causes the misidentification of the material being identified. For this reason, we propose a novel photon counting CT (PC-CT) system consisting of a multi-pixel photon counter (MPPC) coupled with high speed scintillators. This PC-CT can acquire CT images with low radiation dose (1/10-1/100 of that used in conventional CT). Moreover, the advantages of this system are its cost effective than other PC-CT system used cadmium zinc telluride (CZT). We succeeded in procuring color 3-dimensional images of a lighter and estimating absolute concentration of multiple contrast agents with this PC-CT system. In this study, we extended 16-channel PC-CT system to 64-channel. The improvement point from 16-channel PC-CT system is as follows. 1) 64-channel PC-CT system enable to image wider area. 2) The energy information of 64ch PC-CT system increase because the number of thresholds change four to six, and therefore, it enables to simultaneous image of different three contrast agents (e.g. iodine, gadolinium, gold nanoparticle). In addition, we developed a new ceramic MPPC which tolerate high X-ray rate and evaluated it. We conclude that this 64-channel PC-CT system make a giant step toward clinical application.

### Submission declaration

Original and unpublished

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**Presenter:** KIJU, Hiroaki

**Session Classification:** Session4

**Track Classification:** Applications in biology, medicine, medical equipments

Contribution ID: 270

Type: POSTER

## Design and Evaluation of Large Area Strip Sensor Prototypes for the ATLAS Inner Tracker Detector

*Saturday, December 14, 2019 2:36 PM (1 minute)*

The ATLAS community is facing the last stages prior to the production of the upgraded silicon strip Inner Tracker (ITk) for the High Luminosity Large Hadron Collider (HL-LHC). An extensive Market Survey was carried out in order to evaluate the capability of different foundries to fabricate large area silicon strip sensors, satisfying ATLAS ITk specifications.

The semiconductor manufacturing company Infineon Technologies AG was one of the two foundries, along with Hamamatsu Photonics K.K., evaluated for the production of the new barrel silicon strip sensors for the ITk. This work presents the complete tests carried out on the sensors designed and fabricated in 6-inch wafers in the framework of the Market Survey.

The full prototype wafer layout was designed using a Python-based automatic layout generation tool, able to rapidly design sensors with different characteristics and dimensions based on a few geometrical and technological input parameters.

A complete characterization of the full sensors and test structures fabricated is presented, including the results of proton and neutron irradiations, and their compliance with the specifications of the ITk strip tracker.

### Submission declaration

Original and unpublished

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**Presenter:** ULLAN COMES, Miguel (CNM-Barcelona (ES))

**Session Classification:** POSTER

**Track Classification:** Strip sensors

Contribution ID: 271

Type: POSTER

## First application of super-resolution imaging technique using a Compton camera

*Saturday, December 14, 2019 2:02 PM (1 minute)*

In medical imaging, precise and reliable images are very important. However, the quality of images is sometimes limited because of low-event statistics owing to the lack of sensitivity of detectors in radiology. However, long exposure to radiation and a long inspection duration become a burden for the patients. In this paper, we propose a method for generating/predicting high quality images of gamma-ray sources from low statistic data by using machine learning, particularly, sparse coding and dictionary learning. As a first application, we generated/predicted a high-quality image of  $^{137}\text{Cs}$ , which emits 662-keV gamma rays from low-event statistics measured using a Compton camera. We simulated various geometries of the gamma-ray source ( $^{137}\text{Cs}$ ; 662 keV) with the Compton camera by Geant4. Then, a complete set of low-resolution and high-resolution dictionaries were prepared. We acquired the images reconstructed from actually measured data as test samples. The convergence of gamma-ray image was found to be similar for the real and predicted images, which was also supported by an improvement of the structural similarity. We also discussed future plans to use this technique for visualizing radium chloride ( $^{223}\text{Ra}$ ) in the patient's body, which makes the in-vivo imaging of alpha-particle internal therapy possible for the first time.

### Submission declaration

Original and unpublished

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**Presenter:** SATO, Shogo (Waseda university)

**Session Classification:** POSTER

**Track Classification:** Applications in biology, medicine, medical equipments



Contribution ID: 272

Type: POSTER

## A fully functional peripheral readout logic design for a CMOS pixel sensor prototype developed for the CEPC vertex detector

*Saturday, December 14, 2019 2:23 PM (1 minute)*

The CEPC vertex detector system expects low resolution, low material, fast readout, and low power. Monolithic CMOS Pixel Sensors (CPS) are preferred. In the past, several chips have been developed for studying the sensing diode and the readout architectures. This work aims to realize a fully functional peripheral readout logic design for CPS.

In the CEPC experiments, the bunch spacings and the hit densities are 680ns and 2.5/bunch/cm<sup>2</sup> at 240GeV, 210ns and 2.5/bunch/cm<sup>2</sup> at 160GeV, and 25ns and 0.2/bunch/cm<sup>2</sup> at 91GeV. The maximal the data rate is near 120MHz, and the dead time for the pixel readout is about 500ns every double column. The existing CPS cannot satisfy all the requirements. Therefore, we propose a new readout architecture, where the hit pixel addresses in a double column of the pixel array are read out based on the data-driven scheme like FEI3 and ALPIDE, and all the double columns are read out parallel. The main functions of the peripheral readout circuits include: providing the read control signals for both ALPIDE and FEI3 timing, supporting trigger and triggerless modes, and providing real-time data compression. The possible error of timestamps is considered and a time window can be set in trigger mode. The design is also adapted with different address orders of pixels in a column. In addition, the chip tests are considered. Including the scan chains and the memory BIST, we also support to mask pixels with a well-designed setting flow and to generate the test patterns for the function test of peripheral readout circuits.

The design was finally realized in the 0.18 $\mu$ m Tower Jazz process. In the simulation, all the proposed functions were well supported. The hit rate of 120MHz for 1024 $\times$ 512 pixels can be well processed. The power consumptions of the peripheral readout logics are estimated as 25~30mW/cm<sup>2</sup> in trigger mode and 35~45mW/cm<sup>2</sup> in triggerless mode. The peripheral readout logic was reduced for 192 $\times$ 64 pixels in the CPS prototype named TaichuPix1. TaichuPix1 will be characterized this November.

### Submission declaration

Original and unpublished

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**Presenter:** WEI, Xiaomin

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for tracking

Contribution ID: 273

Type: POSTER

## Performance verification of detecting soft X-rays with a next generation Si CMOS detector for space applications

*Saturday, December 14, 2019 2:15 PM (1 minute)*

An all-sky survey of X-ray transient objects in the soft X-ray band is essential to discover mysterious electromagnetic counterparts of gravitational-wave sources, and observe high-redshift objects to probe unexplored physical conditions in the early universe. HiZ-GUNDAM is a future satellite mission to realize this in the soft X-ray band (0.4–4 keV). The X-ray detector of HiZ-GUNDAM has Si pixel sensors that require a fine positioning accuracy (e.g. tens of micrometer), a high-detection efficiency, large detection area (tens of cm<sup>2</sup>) and, relatively high frame rate of ~10 frames s<sup>-1</sup>. A back-illuminated Si CMOS image sensor can satisfy these requirements. For basic development, GSENSE400BSI-TVISB, fabricated by Gpixel Inc., with 2048×2048 pixels of size 11 μm, was selected. We conducted a detailed study on the spectroscopic performance of CMOS in the soft X-ray band and its radiation tolerance for space applications. When the CMOS was irradiated with low-energy X-rays in a vacuum environment fluorescent Al Kα X-ray at 1.49 keV and other similar low-energy lines were clearly detected. Furthermore, detection efficiency >50% was achieved in the soft X-ray band, corresponding to ~10 μm thickness of the depletion layer. We also evaluated radiation tolerance against high-energy gamma-rays (<sup>60</sup>Co for 30 krad) and 100-MeV protons (4.8×10<sup>10</sup> proton cm<sup>-2</sup>). The results showed that an increase in dark current was suppressed by cooling to less than -20 °C with an exposure time of ~0.1 s, and X-rays above 0.4 keV could be detected even after irradiation. In addition, we investigated radiation tolerance of low energy charged particles using alpha particles from <sup>241</sup>Am. Considering the physical structure of CMOS, we selectively irradiated the CMOS depletion and circuit layer with alpha rays by adjusting the Bragg peak positions. We found that even for high doses, a low detectable energy of 0.4 keV was achieved.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Pixel sensors for imaging

Contribution ID: 274

Type: POSTER

## X-ray irradiation studies on a large area HVCMOS pixel sensor chip for ATLAS ITk

*Saturday, December 14, 2019 2:29 PM (1 minute)*

This contribution presents the investigation of radiation damage on ATLASpix1\_M2, which is one of the design variants of ATLASpix1 chip. ATLASpix1 is a large area (1 cm x 1.3 cm) High Voltage CMOS (HVCMOS) sensor prototype in 180nm technology. ATLASpix1\_M2 is originally designed targeting the requirements of ATLAS ITk layer 4. It has a novel data transfer scheme from pixels to periphery where the readout circuitry is located. The ATLASpix1\_M2 prototype supports triggered readout. For this purpose, a Content Addressable Buffer (CAB) which stores the hit data until an on-chip programmable latency has been designed. The digital block contains a novel multiplexer based serializer and an 8b/10b pipelined encoder which will be presented in this work. The serial data link is tested to work at 1.28 Gbps which meets the requirement of ATLAS ITk. The chip was irradiated in steps reaching a total radiation dose of 100 MRad. The pixel and readout electronics is fully functional after irradiation. We were able to perform threshold tuning which resulted in 2 x reduction in threshold dispersion across the matrix (320x56). The effect of radiation on leakage current, signal to noise ratio and power consumption are studied. This work presents the functional testing of ATLASpix1\_M2 chip under X-ray irradiation.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Pixel sensors for tracking

Contribution ID: 275

Type: ORAL

## Design and performance of strip sensors with slim edges for HPS experiment

*Tuesday, December 17, 2019 3:00 PM (20 minutes)*

The HPS experiment is searching for heavy photon particle in mass range between 30 and 200 MeV/c<sup>2</sup>. This particle is postulated to mediate interactions with Dark Matter and is of cosmological importance. The experiment itself has a fixed target geometry. It is operated at Jefferson Lab's CEBAF electron accelerator. Electrons with energy of several GeV impinge on the thin target and can originate heavy photons in a process similar to bremsstrahlung. The photon decay into an electron-positron pair can then be detected.

HPS can use several search strategies. One of them relies on displaced vertex identification requiring a precision tracking and vertexing system. HPS was originally built with a 6-layer Silicon Vertex Tracker (SVT). For the on-going 2019 run SVT was upgraded with additional layer, called layer-zero (L0), which was placed at 5 cm distance from the target, half of the original 1st layer (L1) distance. In order to improve physics reach and avoid beam scattering, the new sensors' active region was designed to be 750  $\mu\text{m}$  away from the beam. This required slim edge sensor technology with target inactive width of sensor periphery of 250  $\mu\text{m}$ .

The sensors were laid out and fabricated by CNM Barcelona to HPS design. Each device has two rows of 1.5 cm long strips with 55  $\mu\text{m}$  strip pitch. The relatively short strip length allowed to use 200  $\mu\text{m}$  thick silicon wafers to reduce multiple scattering of individual tracks. The slim edge was implemented as a post-processing step using Scribe-Cleave-Passivate (SCP) technology. In order to improve SCP application, a wafer lattice alignment method was implemented as a pre-processing step using specifically-etched alignment marks on the bare silicon wafers. A sufficient number of sensors was produced to allow installation of the new L0. In addition, L1 modules were replaced to further enhance tracking performance.

The presentation will describe the sensor production and module building experience, as well as sensor operations during 2019 experimental run.

### Submission declaration

Original and unpublished

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**Session Classification:** Session9

**Track Classification:** Strip sensors

Contribution ID: 276

Type: POSTER

# High Counting Rate High Dynamic Range Front-End Readout ASIC for Electromagnetic Calorimeter in HIEPA

*Saturday, December 14, 2019 2:49 PM (1 minute)*

The 2-7GeV high intensity electron-positron accelerator (HIEPA), as one of the options for the new generation of particle physics test facility in China, is currently under pre-research stage. High energy resolution electromagnetic calorimeter (EMC) for measuring the energy and direction of photons and electrons is one of the important components in an accelerator. This abstract presents a front-end readout ASIC with high counting rate, and high dynamic range, which is designed for EMC. The ASIC is fabricated using TSMC 0.18- $\mu\text{m}$  CMOS technology, and used for APD detector whose parasitic capacitance is 270pF. The readout channel is comprised of a charge sensitive amplifier (CSA), two CR-RC2 shapers, two peak-detect-and-hold (PDH) circuits, a gain select circuit, a fast shaper, a discriminator and a readout buffer. The input range of the ASIC is from 0.4fC to 1000fC, reflecting to the energy level from 1 MeV to 2500 MeV. For this large input range, the readout channel has two branches after the charge-sensitive amplifier (CSA), high gain branch and low gain branch, and using the gain select circuit to choose which one is output. In the simulation, the readout channel counting rate is 200KHz with the peaking time can be adjusted from 0.5us to 1.5us. The readout channel is optimized for 270pF of input capacitance, and the verified result of signal to noise ratio (SNR) achieved 4 at 0.4fC input charge. The linear error is less than 3%, and the power dissipation is about 10mW/channel.

## Submission declaration

Original and unpublished

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**Presenter:** Mr LIU, Chao (Northwestern Polytechnical University)

**Session Classification:** POSTER

**Track Classification:** ASICs



Contribution ID: 279

Type: POSTER

## Study of the HV-CMOS active strip sensor (CHESS2) for future silicon trackers

*Saturday, December 14, 2019 2:30 PM (1 minute)*

CMOS active pixel sensor technology has become extremely attractive for charged particle tracking at High Energy Physics experiments. It integrates both the sensing element and the signal processing circuitry on one single chip. It promises high spatial resolution, low cost and low material budget that are desirable for high performance tracking. Sensors fabricated with high voltage (HV)-CMOS technology can achieve deeper depletion region and enable charge collection by drift that leads to faster charge collection and improved radiation hardness. These attractive features make HV-CMOS sensor a promising solution for the next generation large area silicon trackers at future collider experiments.

CHESS (CMOS HV/HR Evaluation for Strip Sensor) chip design aimed to evaluate CMOS sensors as an alternative solution to conventional micro-strip sensor for the ATLAS inner tracker upgrade. Intensive tests were carried out with the first prototype (CHESS1) to evaluate individual devices at analogue level, and results were used to optimize the second prototype (CHESS2).

CHESS-2 fabricated with the AMS-H35 high voltage process, was implemented with large matrix of pixel cells. Each pixel has its own amplifier and digitalization circuit embedded. The amplifier circuit has several bias currents for tuning its performance. Several prototype sensors have been wire-bonded to carrier boards and tested in laboratory. Tests results with different signal sources will be presented. Tuning of the in-pixel circuit using laser signal will be included as well. With the tests performed, some basic characteristics of the chip were identified. For the tests with the laser, different configurations of in-pixel circuit and laser were tried, and a better understanding of the chip was achieved by comparing the tests results with the simulation results. For example, the tests results showed that the amplifier response is larger with faster/narrower laser signal which is consistent with the circuit simulation results.

More tests with radioactive sources and laser with different injecting direction are foreseen to be done to achieve further understanding of the CHESS2 prototype sensors performance.

### Submission declaration

Original and unpublished

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**Presenter:** HAN, Yubo (Chinese Academy of Sciences (CN))

**Session Classification:** POSTER

**Track Classification:** Strip sensors

Contribution ID: 280

Type: POSTER

## A fully integrated 10-bit 100 MS/s SAR ADC with metastability elimination for the high energy physics experiments

*Saturday, December 14, 2019 2:51 PM (1 minute)*

The demand of high speed, low power analog-to-digital converter (ADC) is growing fast in future high energy physics experiments or in upgrade of current detectors. Also, the ADC becomes more and more critical in the front-end application specific integrated circuit (ASIC) design. Based on these considerations, a fully integrated, 10-bit 100MS/s successive approximation register (SAR) ADC with metastability elimination technique for the high energy physics experiments has been developed.

The ADC is composed of an internal bandgap biasing circuitry, a high bandwidth reference buffer, a digital clock management unit, and 10-bit digital output buffers with unsigned binary format. A non-binary weight capacitor digital-to-analog converter (C-DAC) network and a hybrid capacitor switching architecture are used to increase conversion accuracy and speed. A metastability elimination technique is employed to avoid comparator metastability, and then reduce the conversion error rate (CER) at a high-speed asynchronous operation. The full custom logic cells without floating nets are designed to improve the performance of the radiation hardness.

The ADC was designed and fabricated in a 40 nm CMOS process. It occupies 0.078 mm<sup>2</sup> active area including references and the core area is only 0.037 mm<sup>2</sup>. The measured power consumption of the ADC core is 1.32 mW and the total power consumption is 8.5 mW including references under a 1.1V supply. The resulting figure-of-merit (FOM), for sampling rate 100 MS/s, is 135 fJ/conversion-step. The largest power goes to a robust reference buffer that comprise a fully integrated ADC ASIC. It achieves a good dynamic performance with ENOB ~ 9.3bit at 100MS/s with 14.97MHz input signal. The measured spurious free dynamic range (SFDR), total harmonic distortion (THD) and signal-to-noise ratio (SNR) are 72dB, -69dB, 58dB, respectively. And the measured DNL and INL are +0.67/-0.54 LSB and +0.62/-0.4 LSB respectively.

### Submission declaration

Original and unpublished

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**Presenter:** Mr CAO, Shuxin (International Green Chip Co., Ltd.)

**Session Classification:** POSTER

**Track Classification:** ASICs

Contribution ID: 281

Type: POSTER

## Study of total ionization does effects on IHEP-NDL LGAD sensors

*Saturday, December 14, 2019 3:25 PM (1 minute)*

A High-Granularity Timing Detector (HGTD), based on low-gain avalanche detector (LGAD) technology, is proposed for the ATLAS Phase-II upgrade. In order to operate in harsh environment in high luminosity LHC, One of the most important parameters of the HGTD is radiation hardness of the sensors and electronics. This contribution focuses on total ionization does (TID) effects on LGAD sensors developed by NDL (Novel Device Laboratory) and IHEP. IHEP-NDL sensors are irradiated up to 3MGy using Multi-Rad 160 X-ray irradiator. In order to study the sensor surface damage due to TID effects, we measure the inter-pad isolation and surface leakage current of various 2x2 LGAD sensors with different doping profile, epitaxial resistance and guardring design. The surface damage due to TID effects are also measured performing laser test and beta source tests on IHEP-NDL sensors.

### Submission declaration

Original and unpublished

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**Presenter:** YU, Chengjun (Chinese Academy of Sciences (CN))

**Session Classification:** POSTER

**Track Classification:** New ideas and future applications

Contribution ID: 283

Type: ORAL

## Performance of the Belle II Silicon Vertex Detector

*Sunday, December 15, 2019 9:40 AM (20 minutes)*

The Belle II experiment at the SuperKEKB collider of KEK (Japan) started recording physics data in spring 2019 with all its subdetectors installed and with the goal of accumulating  $50 \text{ ab}^{-1}$  of  $e^+e^-$  collision events at the unprecedented instantaneous luminosity of  $8 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$ , about 40 times larger than its predecessor. The Belle II vertex detector plays a crucial role in the broad Belle II physics program, especially for time-dependent CP measurements. It consists of two layers of DEPFET-based pixels and four layers of double-sided silicon strip detectors (SVD).

The experience gained from first period of SVD operation can be summarized as smooth and reliable running of the detector, with high stability of noise levels and calibration parameters obtained from local calibration runs. No major problem has been experienced. The detector even survived without any notable damage to few serious radiation accidents in which the beam was lost due to failure in the machine focusing quadrupoles. This first period of physics data taking delivered enough data to determine the SVD performance. Despite a machine background, which is significantly higher than expected for the so far achieved luminosity, SVD shows excellent hit and tracking efficiency. Moreover, cluster energy and signal to noise ratio as well the hit time and spatial resolutions measured on data showed a fair agreement with the expected performance.

### Submission declaration

Original and unpublished

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**Session Classification:** Session1

**Track Classification:** Large scale applications

Contribution ID: 284

Type: ORAL

## IHEP-NDL Prototype LGAD sensors for the HGTD

*Wednesday, December 18, 2019 2:00 PM (20 minutes)*

A High-Granularity Timing Detector (HGTD), based on Low-Gain Avalanche Detector (LGAD) technology, is proposed for the ATLAS Phase-II upgrade.

In this contribution, we present new developments in the production of LGAD by NDL (Novel Device Laboratory, Beijing) and IHEP. NDL has delivered three batches of LGAD prototype sensors at the beginning of 2019. These sensors are fabricated with 30um high resistivity epitaxial silicon layer. Time resolution of  $\sim 30$  ps can be achieved with these sensors in both beta test and electron beam test before irradiation.

We will also show the collected charge and timing performances of IHEP-NDL LGAD sensors after proton irradiation up to  $4.5 \text{ E15 neq/cm}^2$  or after X-ray irradiation up to 3MGy. A variety of design strategies to improve radiation hardness, including changing the guard ring design, varying the resistance of the epitaxial silicon layer and varying gain layer doping profile of LGAD sensors, will be discussed.

### Submission declaration

Original and unpublished

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**Presenter:** Dr FAN, yunyun (IHEP)

**Session Classification:** Session13

**Track Classification:** New ideas and future applications

Contribution ID: 285

Type: POSTER

## Timepix3 telescope time performance.

*Saturday, December 14, 2019 3:21 PM (1 minute)*

A beam telescope based on the Timepix3 ASIC was built in order to perform detailed studies of VELO Upgrade prototypes using charged particle beams. The telescope consists of 8 planes of hybrid pixel detectors with 300  $\mu\text{m}$  p-on-n silicon sensors.

Tracks measured with the telescope have excellent spatial resolution, reaching under 2  $\mu\text{m}$  due to the small (55x55  $\mu\text{m}^2$ ) pitch, per-pixel measurements of the deposited charge, and the orientation of the detector planes in order to maximally profit from charge sharing.

In addition to precise spatial measurements, the Timepix3 ASIC operates with a 640 MHz oscillator that allows hit time-stamping in steps of 1.56 ns, giving a potential time-measurement resolution of 450 ps per plane. It is of great interest for future pixel trackers to investigate how precise time measurements can be combined to give optimal track time precision. Detailed studies have been performed to investigate the temporal resolution of individual telescope planes and the track timestamp obtained through the combination of the 8 planes.

In order to control systematic effects and provide an independent time measurement, two scintillators mounted on fast PMTs were placed at opposing ends of the telescope. Their signals are treated by constant fraction discriminators to minimise jitter. The combination of this setup and the track timestamps results in a temporal resolution of approximately 200 ps, which has allowed the assessment of new prototypes with more promising technologies for precise timing. The sub-nanosecond precision of the track time allows the study of timing structures within the pixel chip, along with measurements of other potential systematic effects. Complementary studies are being performed in the lab with a laser setup and preliminary results will be presented.

In this presentation the most recent results on the temporal resolution of the Timepix3 telescope will be presented, together with the timing performance of new sensor prototypes.

### Submission declaration

Original and unpublished

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**Presenter:** CARVALHO AKIBA, Kazuyoshi (Nikhef)

**Session Classification:** POSTER

**Track Classification:** New ideas and future applications

Contribution ID: 286

Type: ORAL

## In-depth experimental Study of Acceptor Removal in Low-Gain Avalanche Detectors

*Wednesday, December 18, 2019 2:40 PM (20 minutes)*

Low-Gain Avalanche Detectors (LGAD) have gained high consideration in the past years thanks to properties such as time resolution below 30 ps. The first large-scale use of LGADs will be in the High-Luminosity LHC upgrades of CMS and ATLAS. LGAD are thin silicon sensors with internal gain supplied by a thin layer of highly concentrated Boron close to the junction. During neutron and proton irradiation, the Boron concentration is reduced by the acceptor removal process, thought to involve the creation of a neutral complex of Boron with the interstitial states in the silicon. This process leads to a reduction of the gain with fluence.

We have investigated the acceptor removal through neutron irradiation up to a fluence of  $3E15$  neq/cm<sup>2</sup> by observing simultaneously a) the reduction in gain with charge collection studies with  $\beta$ -particles and b) the change in the bias voltage required to deplete the gain layer VGL using C-V measurements. We find perfect correlation between these parameters, although the correlations differ widely between LGAD produced by different manufacturers using different methods to extend the fluence reach of their LGAD. We will compare the acceptor removal of LGADs with Boron implanted at different depth and with additional Carbon implants.

### Submission declaration

Original and unpublished

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**Session Classification:** Session13

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 287

Type: POSTER

## Layout and Performance of HPK Prototype LGAD sensors for the High-Granularity Timing Detector HGTD

*Saturday, December 14, 2019 3:27 PM (1 minute)*

We report on the layout and performance of Low-Gain Avalanche Detectors (LGAD) produced by HPK as prototypes for the HGTD in ATLAS. The HGTD is a multi-layer upgrade of the ATLAS detector of total area of 6.4m<sup>2</sup> covering the pseudo-rapidity region between 2.4 and 4.0 with timing sensors with time resolution of 50 ps, representing the first large scale application of the LGAD. With a common mask, sensors with an active thickness of 50  $\mu\text{m}$  (2 splits) and 35  $\mu\text{m}$  (3 splits) were produced. The different splits refer to different combinations of doping profile of the gain layer and resistivity of the bulk, which were measured using C-V. The layout of the sensors is based on a pitch of 1.3 x 1.3 mm<sup>2</sup> pads. Single pads with varying distance to the edge and 2x2 arrays with different inter-pad gap were used to determine safe outside and inside dimensions. Large arrays with 5x5 and 15x15 pads were used to investigate the yield by measuring the breakdown voltage. The dynamic properties of the LGAD were determined with charge collection measurements with laser and charged particles yielding the bias dependence of the gain and of the time resolution.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** New ideas and future applications



Contribution ID: 288

Type: ORAL

## Radiation Campaign of HPK Prototype LGAD sensors for the High-Granularity Timing Detector (HGTD)

*Wednesday, December 18, 2019 2:20 PM (20 minutes)*

We report on the results of a radiation campaign with neutrons, protons and gammas of Low-Gain Avalanche Detectors (LGAD) produced by HPK as prototypes for the HGTD in ATLAS. With a common mask, sensors with an active thickness of 50  $\mu\text{m}$  (2 splits) and 35  $\mu\text{m}$  (3 splits) were produced. The different splits refer to different combinations of the doping profile of the gain layer and the resistivity of the bulk. Sensors were irradiated separately in steps of roughly 2x up to a fluence of  $3\text{E}15$  neq/cm<sup>2</sup>. As a function of the fluence, the following results will be reported for operation at -30C: the power and breakdown voltage using I-V measurement, doping profile for the gain layer and the bulk from C-V data, and the collected charge and time resolution from measurements with laser and charged particles. The results will be compared to the goal of operating the HGTD efficiently up to a fluence of  $3\text{E}15$  neq/cm<sup>2</sup>.

### Submission declaration

Original and unpublished

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**Presenter:** SHI, Xin (Chinese Academy of Sciences (CN))

**Session Classification:** Session13

**Track Classification:** New ideas and future applications

Contribution ID: 289

Type: POSTER

## Design of a low-noise, high-linearity, readout ASIC for CdZnTe detectors in gamma spectrometers

*Saturday, December 14, 2019 2:52 PM (1 minute)*

CdZnTe detectors are promising candidates for X-ray and gamma ray detecting, due to their good energy resolution, high detection efficiency and room temperature operation. They are suitable to be equipped in gamma spectrometers for energy measurement. Compared to board system, application specific integrated circuit (ASIC) features lower power consumption and smaller size. Especially for portable gamma spectrometer, readout ASIC is necessary. Low noise is required in order to improve energy resolution. Since the CdZnTe detectors may be far away from the ASIC, the influence of input capacitance is also hoped to be low. In order to measure energy in a large range, the output voltage must be always linear. Therefore, the gain of shaper is restricted. Tradeoff should be considered between noise and linearity.

The presented work aims to achieving low-noise and high-linearity in a wide range of input charge. In order to improve linearity, an active resistor and a high-linear analog buffer are employed. A  $CR - (RC)^2$  shaper is proposed. Different types of resistances are utilized in the first stage and second stage of the shaper, to achieve low noise and high linearity at the same time. A channel of the proposed circuit is composed of a preamplifier, a shaper, a peak and hold circuit, which can automatically detect the peak of shaper output voltage. The output voltage is not read out, except a channel is hit. Therefore, power consumption is decreased.

A prototype chip with 8 channels has been designed and fabricated in a standard commercial 1P6M 0.18  $\mu\text{m}$  CMOS process. Die area of one channel is about  $650 \mu\text{m} \times 110 \mu\text{m}$ . The input charge range is from 1.5 fC to 60 fC. Peaking time can be adapted from 3  $\mu\text{s}$  to 5  $\mu\text{s}$ . Measured ENC is about 206  $e^-$  at input capacitor of 0 F with the slope of 8.1  $e^-/\text{pF}$ . The gain is 18.7 mV/fC at peaking time of 4  $\mu\text{s}$ . Non-linearity is about 3%. More measured results will be presented in this symposium.

### Submission declaration

Original and unpublished

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**Presenter:** Dr WANG, Jia (Northwestern Polytechnical University)

**Session Classification:** POSTER

**Track Classification:** ASICs

Contribution ID: 290

Type: POSTER

## Testbeam measurements with passive CMOS pixel sensors in 150 nm LFoundry technology bump-bonded to the RD53A readout chip

*Saturday, December 14, 2019 2:27 PM (1 minute)*

The Large Hadron Collider at CERN will be upgraded to the High-Luminosity-LHC and will deliver an instantaneous luminosity increased by a factor of 5 - 8 from 2026 on compared to now. In order to cope with the increased radiation level and hit rate, detectors with better radiation tolerance and higher data rate capabilities are demanded. Therefore, the ATLAS experiment, one of the four large experiments at CERN, gets an all new pixel detector which is part of the ATLAS tracking detector. The new ATLAS pixel detector will consist of 5 layers and its surface will increase from 2 m<sup>2</sup> to around 15 m<sup>2</sup> in the future.

Therefore, commercial CMOS processes which offer high yield and high throughput at comparatively low costs are of interest in order to build up large scale detectors not only for the readout chip but also for the sensor.

In order to qualify the suitability of commercial CMOS pixel sensors for the ATLAS pixel detector upgrade, pixel sensors using a 150 nm CMOS technology offered by LFoundry have been designed and produced.

These passive CMOS sensors were bump-bonded to a RD53A readout chip which is the first prototype readout chip for the ATLAS pixel detector upgrade. The characterization of the pixel sensors in the lab as well as in a test beam using 2.5 GeV electrons will be presented.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Pixel sensors for tracking

Contribution ID: 291

Type: POSTER

## Solar Neutron and Gamma-ray Spectroscopy (SONGS) Mission

*Saturday, December 14, 2019 3:14 PM (1 minute)*

Solar neutron observations are important on understanding of nucleon acceleration mechanism in the Sun. However, previous ground-based observations with large area telescopes ( $\sim 10 \text{ m}^2$ ) at high latitude are not sensitive to solar neutrons due to attenuation in the earth atmosphere (roughly 10 detection since its discovery in 1980). From space, the SEDA-AP instrument with much smaller area ( $100 \text{ cm}^2$ ) onboard the International Space Station (ISS) monitored solar neutrons including charged particles, and successfully detected more than 30 detection since its launch in 2009. Unfortunately the SEDA-AP operation was stopped on March 2018. To overcome situation for no mission dedicated for solar neutrons, we have designed and developed a solar neutron and gamma-ray detector for a 3U cubesat with a size of  $30 \times 10 \times 10 \text{ cm}$ . Actually we launched the 50-kg class ChubuSat-2 satellite for solar neutron observations on February 2016, and have now been adjusting it to a 3U CubeSat application, which is named as Solar Neutron and Gamma-ray Spectroscopy (SONGS) Mission. The solar neutron and gamma-ray detector consists of multi-layered plastic scintillator bars, and GAGG(Ce) scintillator array, and both of them are read out with silicon photo-multipliers (Si PMs). More than 600 signals from Si PMs are processed by ASICs provided by IDEAS. In this paper, we will describe details of the detector and performance of its breadboard model (BBM).

### Submission declaration

Redundant (overlaps with already published)

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**Presenter:** Dr YAMAOKA, Kazutaka (ISEE, Nagoya Univ.)

**Session Classification:** POSTER

**Track Classification:** Applications in astrophysics

Contribution ID: 292

Type: ORAL

## The LHCb Vertex Locator Upgrades

*Sunday, December 15, 2019 11:40 AM (20 minutes)*

While the current LHCb Upgrade I is currently being installed and plans to run with increased luminosity and efficiency, the collaboration has already submitted a physics case for an Upgrade II detector to begin operation in 2031. Even at the Upgrade I accumulated statistics of  $50 \text{ fb}^{-1}$ , expected to be achieved by 2030, most physics channels will be statistically limited.

In the upcoming LHC run, the LHCb experiment will read out every bunch crossing and perform the trigger decision in a computing farm with the whole event information. The Vertex Locator (VELO) will be composed of a pixelated detector with  $55 \mu\text{m}$  pitch installed at 5 mm from the beam axis. The front-end has a data-driven readout optimised for high speed operation.

The future upgrade stage is designed to run at instantaneous luminosities of  $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  and accumulate over  $300 \text{ fb}^{-1}$ . At this intensity, the average pile-up would be 56 with around 2500 particles within the acceptance. Time measurements will be needed to assign correctly each b hadron to its origin primary vertex and to perform the real-time pattern recognition and track reconstruction. To achieve these goals a 4D hybrid-pixel detector with enhanced timing capabilities in the ASIC and sensor will be developed. Improvements in the mechanical design will also be needed to allow for periodic module replacement. The design will be further optimised to minimise the material before the first measured point on a track and to achieve a more fully integrated module design with thinned sensors and ASICs combined with a lightweight cooling solution. As well as improving the VELO performance, quantified by the impact parameter resolution, these changes will be beneficial in improving the momentum resolution of the spectrometer and reducing the impact of secondary interactions on downstream detectors.

In this presentation the VELO Upgrade electronics design and implementation will be shown as well as status of the construction and installation. The design considerations and R&D studies for the future upgrade will also be discussed.

### Submission declaration

Original and unpublished

**Primary authors:** CARVALHO AKIBA, Kazuyoshi (Nikhef); COLLINS, Paula (CERN)

**Presenter:** CARVALHO AKIBA, Kazuyoshi (Nikhef)

**Session Classification:** Session2

**Track Classification:** Large scale applications

Contribution ID: 293

Type: POSTER

## Fine residual stress distribution measurement of steel materials by the SOI pixel detector with synchrotron X-rays

Saturday, December 14, 2019 2:09 PM (1 minute)

Residual stress is an important factor to evaluate and control the quality of metal materials for industrial products. The residual stress measurement using X-rays is one of the most effective ways to evaluate residual stress without destruction. In this measurement, a Debye-ring that is formed by diffraction of X-ray beams on the surface of polycrystalline metal is used. The effects of residual stress on crystal structure can be observed by the Debye-ring's deformation. Thus, residual stress can be analyzed from the shape of Debye-ring.

In previous studies, we developed the residual stress measurement system based on the  $\cos\alpha$  method using the two-dimensional detector. The silicon on insulator (SOI) pixel detector, named INTPIX4, was implemented as this system's two-dimensional detector. In a typical setup in laboratory, this system requires only one second for measuring one specified point. It's drastically faster than a conventional system based on  $\sin^2\psi$  method that requires more than ten minutes. And it's also faster than the  $\cos\alpha$  based system using an imaging plate that requires one minute. This feature makes it easier to evaluate the two-dimensional distribution of residual stress in a short time and this will give us more detailed information to evaluate materials. We already tried to measure the two-dimensional distribution at laboratory setup with Cr X-ray tube (Cr  $K\alpha$  5.4 keV) and got some good results. We started to measure with synchrotron monochromatic X-rays to determine the fine accuracy and fine sampling pitch distribution as the next step.

In this presentation, we'll report the result in the first synchrotron's experiment, the residual stress distribution of the standard specimen.

### Submission declaration

Original and unpublished

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**Presenter:** Dr NISHIMURA, Ryutaro (High Energy Accelerator Research Organization)

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for imaging

Contribution ID: 295

Type: ORAL

## Performance study of a MAPS detector prototype for the BESIII inner tracker upgrade

*Sunday, December 15, 2019 12:20 PM (20 minutes)*

As one of the prototype schemes of the BESIII inner drift chamber upgrade, a MAPS (monolithic active pixel sensor) detector prototype is under developed. The mass production and quality verification of the pixel detector ladders with low material budget and high chip position precision have been performed based on the optimization of the single ladder. The ladder, consisting of ten MIMOSA28 chips thinned to 50  $\mu\text{m}$ , a flex cable and a carbon fiber support, is the basic structure and functional block of the prototype. In order to verify the design and quantify the performance of the ladders in terms of the detection efficiency, the spatial resolution, the gap between two chips and the material budget, a detector prototype system, including five layer ladders, readout electronics and the DAQ was set up and tested at T24 beam line in the DESY, Germany. The test and the data analysis will be presented, including the alignment method based on Karimäki's algorithm, track reconstruction and analysis software. The results show that the tracking efficiency of 96% is achieved, and the spatial resolution is about 5 $\mu\text{m}$ . The average gap between neighboring chips is measured to be about 340 $\mu\text{m}$ . The actual gap and the chip location accuracy is better than 10 $\mu\text{m}$  if the insensitive part of the sensor is taken into account. The material budget of one ladder is 0.35%  $X_0$ , which is well consistent with the predicted value of 0.37%  $X_0$ . These test results validate a good performance of the prototype.

### Submission declaration

Original and unpublished

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**Session Classification:** Session2

**Track Classification:** Large scale applications



Contribution ID: 296

Type: ORAL

## AC-coupled n-in-p pixel detectors on MCz silicon with atomic layer deposition (ALD) grown thin film process

Wednesday, December 18, 2019 9:40 AM (20 minutes)

We report the fabrication process and characterization of our novel n+/p-/p+ pixel detectors made on 150mm diameter p-type Magnetic Czochralski silicon (p-MCz Si) wafers. The pixels were segmented 52 × 80 dual column and designed to be AC capacitive coupled. The resistive coupling, allowing Quality Assurance (QA) probing prior the Flip-Chip bonding, between pixels was realized by thin film metal -nitride resistors. The bias resistors were fabricated by Atomic Layer Deposition (ALD) technique and in some cases, by sputtering deposition. This approach allows us to render silicon area consuming punch through resistor structures obsolete and simultaneously reduce overall process complexity. Moreover, our previous studies have emphasized that applying ALD Aluminum Oxide (Al<sub>2</sub>O<sub>3</sub>) field insulator and passivation layer results in negative net oxide charge and thus additional p-spray or p-stop surface current termination structures are not necessary.

Our focused application is radiation-hard ALD AC-coupled pixel detector to be used in future use of the High-Luminosity Large Hadron Collider (HL-LHC) experiment. In addition to particle physics experiments and photon science experiments with bright light sources.

The pixel detectors were tested at Helsinki Institute of Physics (HIP) Detector laboratory and Ruđer Bošković Institute (RBI). For further study, AC coupled sensor was hybridized to PSI46dig read out chip (ROC) having 4160 pixels by flip-chip (FC) interconnection technique.

We show measurement data of AC coupled pixel detectors and single pad detectors. Data of electrical properties, full depletion voltage and leakage current are shown as well. The experimental result of bias resistor value 15 kOhm was attained. MOS -capacitor test structures were irradiated by TRIGA reactor neutrons (JSI, Ljubljana) and by 60Co gamma source (RBI, Zagreb). We observed accumulation of negative oxide charge after neutron irradiation, and introduction of positive mobile charge induced by photon irradiation while fixed oxide charge remained stable. Our Transient Current Technique (TCT) measurements indicated clear pixel segmentation with excellent homogeneity.

### Submission declaration

Original and unpublished

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**Presenter:** GÄDDA, Akiko (Helsinki Institute of Physics)

**Session Classification:** Session11

**Track Classification:** Technologies

Contribution ID: 297

Type: POSTER

## A pixelated beam profile monitor for the 320kV ECR platform at Lanzhou

*Saturday, December 14, 2019 3:22 PM (1 minute)*

A 320kV ECR platform has been constructed at the Institute of Modern Physics in Lanzhou to deliver intense high charge state ion beams and medium charge state ion beams for atomic physics, material surface research and biology research. This ECR platform can accelerate the ions up to 300q kV. The dynamical range of the projectile velocity is from 0.3 a.u. to 2 a.u., covering electron capture dominant channel to ionization dominant channel.

To accurately monitor the beam in this ERC platform in real-time and non-interceptive manner, a pixelated Residual Gas Ionization Profile Monitor (RGIPM) has been designed. The RGIPM is expected to work in high vacuum condition of  $10E-9$ . It mainly consists of the TiN coated cathode, the micro-channel plate (MCP) and the pixelated anode, which is realized by the TopMetal 2- chips. The magnetic field, formed by NdFeB permanent magnets, is  $\sim 0.1$  T. The electric field created by the shaping electrodes reside in the magnetic field is  $\sim 50$  kV/m. The Topmetal chip has rather low noise as  $\sim 13e^-$ . The MCP has an electron gain of  $\sim 1500$ , which can provide enough electrons for the pixelated anode. Besides, a mesh is installed at the front of the coated cathode to prevent the secondary electrons, which are generated by ion bombardments, from reaching the anode.

Preliminary simulation and experiments show the RGIPM could provide a spatial resolution of  $\sim 5\mu\text{m}$ . Better spatial resolution can be achieved by adopting the Barycenter algorithm in the on-line data analysis system. This paper will discuss the design, installation and performance study of this RGIPM.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** New ideas and future applications

Contribution ID: 298

Type: POSTER

## First precision spectroscopy of cesium-137 from the ground to 150~m above in Fukushima

*Saturday, December 14, 2019 3:05 PM (1 minute)*

The nuclear disaster at the Fukushima Daiichi Nuclear Power Plant (NPP) in Okuma, Fukushima, was initiated primarily by the tsunami following the Tohoku earthquake on March 11, 2011. After a large amount of radioactive substances was released into the environment of the region, the distribution of the radiation sources on the ground was monitored. However, there have been only few estimations on the height dependence of the air dose rate in the contamination field at Fukushima, all of which discuss only the variation of gross count rates measured in a wide energy range, such as between 50 and 3,000 keV. This paper presents the first results of airborne gamma-ray spectroscopy of a contamination field in Namie, Fukushima, as measured from 0 m to 150 m above the ground by drone. We found that the gamma-ray dose rate measured at 100 m height is about seven times higher than that expected based on ground measuring, which is caused by two factors: (1) the integrated dose includes contamination of upward scattered 662-keV gamma rays and (2) radiation from  $^{137}\text{Cs}$  is vertically collimated because  $^{137}\text{Cs}$  is buried in the soil. We also argue novel method to obtain the distribution of radioactive substances in the soil only through aerial mapping.

### Submission declaration

Original and unpublished

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**Presenter:** Mr KURIHARA, Takuya (Waseda University)

**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 299

Type: POSTER

## CO2 cooling through microchannels

*Saturday, December 14, 2019 3:20 PM (1 minute)*

The LHCb Vertex Detector (VELO) is currently being upgraded to a lightweight, pixel detector capable of 40 MHz readout and operation in very close proximity to the LHC beams. The thermal management of the system will be provided by evaporative CO<sub>2</sub> circulating in micro channels embedded within 500 micron thin silicon plates. This solution has been selected due to the excellent thermal efficiency, the absence of thermal expansion mismatch with silicon ASIC's and sensors, the radiation hardness of CO<sub>2</sub>, and very low contribution to the material budget.

Although micro channel cooling is gaining considerable attention for applications related to microelectronics, it is still a novel technology for particle physics experiments, in particular when combined with evaporative CO<sub>2</sub> cooling. The LHCb design focusses on an efficient layout of the channels together with a delivery system composed of stainless steel pipes and an invar manifold. The assembled silicon plate and connector system must be capable of withstanding pressures in the order of 200 bars. Even distribution of the coolant is ensured by means of the use of 50 x 50 micron restrictions implemented before the entrance to a race-track layout of the main cooling channels.

The cooling plates are produced by etching microchannels in a multi-step process, to account for the different channel depths, in a base silicon wafer, followed by bonding a cover wafer, and finally thinning the assembly. The microchannel production is a complex process involving quality control of production and dicing steps at the manufacturer, followed by a careful assembly technique of the cooling plates to the connectors and pipes, via a flux free soldering process which is performed partially in vacuum and uses formic acid. The quality control includes assessment of surface quality, a cyclic stress test in pressure and temperature, high pressure tests, and helium leak tests. The microchannel production is now underway and the status will be described along with future R&D improvements that could be envisaged.

### Submission declaration

Original and unpublished

**Primary authors:** CARVALHO AKIBA, Kazuyoshi (Nikhef); COLLINS, Paula (CERN)

**Presenter:** CARVALHO AKIBA, Kazuyoshi (Nikhef)

**Session Classification:** POSTER

**Track Classification:** Technologies

Contribution ID: 300

Type: ORAL

## Radiation Resistant Innovative 3D Pixel Sensors for the CMS Upgrade at the High Luminosity LHC

*Monday, December 16, 2019 9:20 AM (20 minutes)*

The High Luminosity upgrade of the CERN Large Hadron Collider (HL-LHC) calls for new high-radiation tolerant silicon pixel sensors, capable of withstanding, in the innermost tracker layer, fluences up to  $2.3 \times 10^{16}$  neq/cm<sup>2</sup> (1MeV equivalent neutrons). An extensive R&D program aiming at 3D pixel sensors, built with a top-side only process, has been put in place in CMS in collaboration with FBK (Trento, Italy) and CNM (Barcelona, Spain) foundries. A few sensors were interconnected with the RD53A readout chip, the first prototype, in 65nm technology, of the pixel readout chip which will be used in the HL-LHC inner trackers. In this presentation results obtained in laboratory measurements and beam tests experiments before and after irradiations will be reported. Irradiation of single chip interconnected modules were performed at CERN IRRAD facility or in KIT Irradiation Center, up to a maximum equivalent fluence of  $1 \times 10^{16}$  neq/cm<sup>2</sup>. Preliminary analysis of collected data shows excellent performance and hit detection efficiencies close 99% measured after the above mentioned irradiation fluences. New ideas and designs for 3D sensors will also be illustrated.

### Submission declaration

Redundant (overlaps with already published)

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**Presenter:** MESCHINI, Marco (Universita e INFN, Firenze (IT))

**Session Classification:** Session5

**Track Classification:** Pixel sensors for tracking

Contribution ID: 303

Type: ORAL

## A Prototype for the SHiP Timing Detector

*Wednesday, December 18, 2019 11:00 AM (20 minutes)*

SHiP (Search for Hidden Particles) is a proposed general purpose fixed target experiment to be located at the CERN SPS. It will search for weakly interacting particles with masses below 10 GeV. The experiment will comprise a heavy target followed by a magnetic muon shield and a dedicated neutrino detector. Downstream of the neutrino detector is a Hidden Sector detector, consisting of an evacuated vacuum vessel, spectrometer, veto timing detector, calorimeters and a muon detector.

A veto timing detector is necessary in order to reject combinatorial di-muon backgrounds. It was found that requiring coincidence events to be within 100 ps was sufficient to reduce this background to an acceptable level. A proposed option for the timing detector consist of scintillating bars read out by arrays of silicon photomultipliers. The detector comprises 546 bars of EJ-200 scintillating material with dimensions 168 cm x 6 cm x 1cm broken into three columns and covering an active area of 5 m x 10 m. The end of each bar is read out by an array of eight silicon photomultipliers attached to custom PCBs and subsequently read out by a DAQ system based on SAMPIC.

We present test beam results on a single column 22 bar prototype for the SHiP timing detector. Measurements were taken at the T10 beam line of the CERN PS. A timing resolution across the entire detector is found to be about 90 ps. The particle identification capability using a ToF method is also demonstrated.

### Submission declaration

Original and unpublished

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**Session Classification:** Session12

**Track Classification:** Large scale applications

Contribution ID: 304

Type: POSTER

# A Wide-Range, 42ps Resolution Time-to-Digital Converter for the Electromagnetic Calorimeter of HIEPA

*Saturday, December 14, 2019 2:50 PM (1 minute)*

The 2-7 GeV High Intensity Electron-Positron Accelerator (HIEPA) is one of the three options for the new generation of particle physics test facility in China, which can help test Quantum Chromodynamics (QCD) in low energy regions and find new physics theory. As one of the important components in the accelerator, the electromagnetic calorimeter (EMC) needs to measure the time information of photons and electrons with sufficient resolution and dynamic range. Therefore, a two-step Time-to-Digital Converter (TDC) with high precision and wide dynamic range is presented in this abstract. The time interval measurement is implemented using a coarse counter, two Delay Locked Loops (DLLs) and a couple of coarse-fine interpolators. The DLL has been used to mitigate the effect of PVT on the proposed TDC. The interpolator consists of a coarse-fine synchronizer and a Vernier Delay Loop, which can minimize the integral non-linearity (INL) through cyclic sliding scale. The proposed TDC is going to be implemented with 0.18  $\mu\text{m}$  CMOS technology, and is verified to be able to measure time intervals from 0 to 2.56  $\mu\text{s}$  with bin size of 42 ps as well as rms precision of 7.1 ps. The TDC consumes 20mW with a 1.8-V supply, and the DNL and INL are both better than 1 LSB.

## Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** ASICs



Contribution ID: 305

Type: POSTER

## Development of CdTe Hybrid Pixel ASIC for Hard X-ray Imaging

*Saturday, December 14, 2019 2:53 PM (1 minute)*

Due to its high atomic number, high detection efficiency and good energy resolution, the cadmium telluride (CdTe) semiconductor has been regarded as a promising material for hard X-ray observation. We have developed a front-end ASIC for a CdTe pixel detector for future hard X-ray astronomy missions. The ASIC is designed for a hybrid configuration so that each CdTe pixel can be vertically bump-bonded to a corresponding pixel circuit. It was fabricated with a TSMC 0.35  $\mu\text{m}$  process CMOS technology. The total chip size is 8 mm by 8 mm and the pixel area is 7 mm by 7 mm and has a total of 784 channels. The pixel area consists of 28 by 28 identical cells with an area of 250  $\mu\text{m}$  by 250  $\mu\text{m}$ . The 10-bit Wilkinson ADC is implemented in each column of the pixel matrix and performs parallel AD conversion. The signals are processed and acquired either in the peak-hold or sample-hold mode before being fed into the ADCs which performs the parallel AD conversion. We tested the ASIC circuit performance and measured its Equivalent Noise Charge (ENC) of about 40 electrons, its integral non-linearity of about 1% and its power consumption was about 0.2 mW per pixel. The pixelated CdTe detector was successfully bump-bonded onto the ASIC and the characteristics and measurement results of the CdTe bump-bonded pixel ASIC will be discussed in this presentation.

### Submission declaration

Original and unpublished

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**Presenter:** ORITA, Tadashi (The University of Tokyo)

**Session Classification:** POSTER

**Track Classification:** ASICs

Contribution ID: 306

Type: POSTER

## IHEP LGAD Sensor Design for ATLAS HGTD

*Saturday, December 14, 2019 3:24 PM (1 minute)*

The IHEP HGTD group has recently developed their first version LGAD sensor. Electrical Characterization TCAD Simulation was tuned to get simultaneously high breakdown voltage and proper gain. N-JTE and P-stop are the critical structures to guarantee high breakdown voltage. The gain layer was optimized for proper gain factor and hence good time resolution. Fabrication process simulation was also performed. Thermal growing oxide process is included for improved irradiation performance. Carbon implantation, high energy injection and low resistance simulation are added in the second version design.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** New ideas and future applications

Contribution ID: 307

Type: POSTER

## Study of characterization, time resolution and proton hardness of IHEP-NDL LGAD sensors

*Saturday, December 14, 2019 3:26 PM (1 minute)*

In view of the high-luminosity Large Hadron Collider (HL-LHC) upgrade, the ATLAS, CMS, RD50 collaborations are developing new irradiation-hard silicon sensors for precision timing measurements using Low gain avalanche diode (LGAD). In China, Novel Device Laboratory in Beijing (NDL) and IHEP have fabricated several batches of LGAD sensors. The basic characterization of IHEP-NDL LGAD sensors will be presented with leakage current measurement and sensor capacitance measurement. The time resolution is also studied using a pico-second laser test system setup in IHEP and electron beam test performed in DESY with 5 GeV electron beam. In order to study the proton radiation hardness, the bulk damage in IHEP-NDL LGAD sensors after proton irradiation is also presented. The proton irradiation is performing in China Institute of Atomic Energy (CIAE) using 100 MeV proton beam up to  $4.5 \times 10^{15}$  neq/cm<sup>2</sup> or in CYRIC using 80 MeV proton beam up to  $1 \times 10^{15}$  neq/cm<sup>2</sup>.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** New ideas and future applications

Contribution ID: 310

Type: ORAL

## Development of a Low-Noise Front-end ASIC for CdTe Detectors

*Wednesday, December 18, 2019 9:20 AM (20 minutes)*

We have developed a series of front-end ASICs with spectroscopic capability for hard X-ray and gamma-ray imaging applications. Our latest ASIC, the “KW04H64” is designed for in-vivo molecular imaging, in which molecules are labeled with radioisotopes and injected into a small animal and their distribution in a body is detected externally. It requires a radiation detector that has good spatial and energy resolution and also covers a large detection area. The ASIC measures 7.12 mm x 8.03 mm and was implemented with X-fab 0.35  $\mu\text{m}$  CMOS technology. It consists of 64 readout channels and each channel contains a charge sensitive amplifier (CSA) including leakage current compensation function, a pole-zero cancellation circuit, two kinds of low pass filter (fast/slow shaper) capable of baseline adjustment for energy and timing measurement, a comparator, a sample and hold circuit, and a 10-bit Wilkinson ADC with common mode subtraction function. According to the photon energy range, the dynamic range can be changed by setting the register controlling the gain of the CSA. A novel function of the ASIC is that the voltage output of the fast shaper can be also digitized, which provides a user friendly method for adjusting the baseline of it. In the highest gain mode, the dynamic range is  $\sim 40,000$  e- and the noise performance is  $31 \text{ e-} + 5.1 \text{ e-}/\text{pF}$  from simulation. Besides the performance verification test of the ASIC itself, we also connected the ASIC to a CdTe detector and measured the spectrum of the radioactive sources of Am-241 and Ba-133. In this presentation, we will report on the results of the performance of the ASIC itself and the detector system, including the comparison with predictions made by simulations.

### Submission declaration

Original and unpublished

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**Session Classification:** Session11

**Track Classification:** ASICs

Contribution ID: 311

Type: ORAL

## Development of the detector simulation framework for the Wideband Hybrid X-ray Imager onboard FORCE

*Sunday, December 15, 2019 2:40 PM (20 minutes)*

FORCE is a space-based astronomy mission for an X-ray imaging spectroscopy in an energy range of 1–80 keV. The Wideband Hybrid X-ray Imager (WHXI), which is the main focal plane detector, will use a hybrid semiconductor imager stack composed of silicon and cadmium telluride (CdTe). The silicon imager, for which we will adopt a certain type of the XRPIX series, will be based on the silicon-on-insulator (SOI) technology to meet requirements of a thick depletion layer and short timing resolution that realizes anti-coincidence particle background rejection. Since the sensor has a small pixel size of 36  $\mu\text{m}$  and the thick sensitive region, understanding the detector response is not trivial and is important to optimize the camera design and to make science planning.

We have developed a simulation framework for the WHXI to predict observed spectra based on Compton Soft, a software suite for Monte Carlo simulation and data analysis. To determine the physical parameters of the XRPIX required for the simulation, we made a comparison of simulations with laboratory measurements. The measurements were conducted using the XRPIX 6H and 6C sensors and radioactive isotopes to evaluate spectra at various energies. The spatial distribution of the charge collection efficiencies, the noise level and diffusion length were considered as parameters to be determined. We compared the measured branching ratio and spectra of single- and double-pixel events to those of simulations at 5.90 keV and 32.2 keV. The simulations well agreed with the measurements mainly by optimizing charge collection efficiencies around the edges of each pixel. This framework is also applicable to future XRPIX updates including the one will be part of the WHXI. In this talk, we present the framework design, evaluations of the measurements and simulations, as well as the expected WHXI spectrum of the Crab Nebula, a standard celestial reference source in the X-ray sky.

### Submission declaration

Original and unpublished

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**Presenter:** SUZUKI, Hiromasa (University of Tokyo)

**Session Classification:** Session3

**Track Classification:** Applications in astrophysics

Contribution ID: 312

Type: POSTER

## Fabrication and X-ray characterization of an organic photodetector for indirect X-ray imaging sensor

*Saturday, December 14, 2019 2:17 PM (1 minute)*

Digital X-ray imaging systems have been substituting analog X-ray imaging systems with conventional X-ray film-screen for radiography applications. Currently, the large-area flat panel imagers with TFT (thin film transistor) and CMOS (complementary metal-oxide semiconductor) process have been widely used in various X-ray imaging applications. Indirect detection type for digital X-ray imaging is essentially consisting a scintillator film and 2D imaging sensor such as amorphous and crystalline silicon based arrays. Both terbium-doped gadolinium oxysulfide (Gd<sub>2</sub>O<sub>2</sub>S:Tb) and thallium-doped cesium iodide(CsI:Tl) are commonly used for conversion of X-ray to visible lights. Currently, the organic polymer-based semiconductor has been widely studied in various field such as OLED display and solar cell due to simple fabrication, cost effectiveness. The organic sensor materials show effective light absorption in emission region of the x-ray conversion scintillator with good photo-generation yield, sensitivity, and response time.

In this work, the conjugated polymer poly(3-hexylthiophene) (P3HT) as a p-type semiconductor and the fullerene derivative phenyl-C<sub>61</sub>-butyric acid methyl ester (PCBM) as an n-type semiconductor have been used to form the bulk heterojunction(BHJ) structure of the organic photodetector. The solution-processed organic structure was prepared with various manufacturing parameters such as different active layer thickness (100-300nm), blending ratio (P3HT:PCBM=3:1, 1:1, 1:3) and buffer layers(hole and electron transport layer). The various scintillators such as Gd<sub>2</sub>O<sub>2</sub>S:Tb and CsI:Tl with columnar structure were used as the X-ray to visible light converter. The fabricated organic active layers in photodetector and scintillators with good green wavelength were optically combined to investigate the X-ray properties.

The properties of the fabricated organic X-ray detector such as the dark current density, X-ray sensitivity, signal to noise ratio, dynamic range were measured under practical X-ray exposure. Typically, our OPDs show satisfactory results with a leakage current density of 10 pA/mm<sup>2</sup> at -2 V bias. The sensitivity of our organic detectors linearly increased as the incident X-ray dose increases. This paper will demonstrate the significant potential of our organic photodetectors for medical imaging and NDT applications with low-dose and high-resolution

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Pixel sensors for imaging

Contribution ID: 313

Type: POSTER

## Development of Front-end ASIC for Silicon-strip Detectors of J-PARC Muon g-2/EDM Experiment

*Saturday, December 14, 2019 2:54 PM (1 minute)*

We develop a front-end ASIC for the silicon strip detector of the J-PARC muon g-2/EDM experiment, which aims to measure the muon anomalous magnetic moment and electric dipole moment to search for new physics beyond the Standard Model. In this experiment, we use a silicon strip detector with high granularity and fast response to detect positrons from muon decay. Since the timing of the muon decay is key information in the experiment, the ASIC is required to tolerate a high hit rate of 1.4 MHz per strip and to be stable to the change of hit rate by a factor of 1/150. To accommodate the pulsed muon beam at J-PARC, the ASIC has a buffer memory to save the binary hit information.

The prototype ASIC has been designed and fabricated using the Silterra 180 ns CMOS process. The prototype contains 128 readout channels, consisting each of a charge-sensitive-amplifier, a CR-RC shaper, a differentiator, two comparators and the buffer memory. Threshold voltage at comparators are adjustable channel by channel using 6-bit Digital-to-Analog Converter (DAC) to compensate channel-to-channel threshold variations. The output of the comparators is then sampled by a 200 MHz clock for the period of 40.96 us and are saved in the buffer memory. The data is serially readout before the next bunch arrives. The main difference of the previous prototype is to add the differentiator at the output of the CR-RC shaper to reduce the time-walk effect. Several bias parameters in the analog circuit are optimized to improve the performance of the noise and peaking time.

The fabricated prototype was directly mounted on a printed circuit board for the evaluation test and was electrically connected by wire-bonding. We checked the response of the prototype with the test pulse charge and estimated the gain, equivalent noise charge, pulse width, time-walk and timing-jitter. In this talk, we present the design of the front-end ASIC and its performance.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** ASICs



Contribution ID: 314

Type: POSTER

## Performance evaluation of recoil electron track detection with an electron tracking Compton camera using an SOI pixel sensor

*Saturday, December 14, 2019 2:10 PM (1 minute)*

Sub-MeV gamma rays are produced by nucleosynthesis processes caused by high energy phenomena in the universe such as supernova explosions. As the details of such nucleosynthesis processes can be inferred from their spectral line features, improved spectral performance in the sub-MeV range is vitally important. However, observations in this energy band have lagged by some decades because of difficulties in removing considerable detector background with a conventional Compton camera. One of the solutions is an advanced Compton camera because it enables high background rejection by detecting recoil electron tracks produced by Compton scattering processes. Therefore, we developed an electron tracking Compton camera using semiconductor sensors with high energy resolution. The selected sensors were XRPIX2b pixel sensors with a fine pitch (30  $\mu\text{m}$ ), high energy resolution, and a trigger capability enabled by silicon-on-insulator (SOI) technology. The in-pixel trigger circuit enables an event-driven readout allowing us to use the coincidence technique to select candidate Compton events and reject background events. We developed a prototype camera using XRPIX2b sensor to verify the recoil electron detection performance of the sensor for sub-MeV gamma rays. This prototype comprises a scatterer using XRPIX2b and an absorber using a 1  $\text{cm}^2$  CsI(Tl) scintillator with a photomultiplier tube. Using this prototype, we measured the  $^{22}\text{Na}$  of a 511keV line gamma ray source and confirmed imaging of the recoil electron tracks. We will report the imaging capability for various gamma ray scattering angles and the dependence on rotational angles of the detector, and show the comparison with Monte Carlo simulations.

### Submission declaration

Original and unpublished

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Contribution ID: 315

Type: POSTER

## Study of time resolution of low-gain avalanche detectors

*Saturday, December 14, 2019 3:29 PM (1 minute)*

We are conducting research on Low-Gain Avalanche Detector (LGAD), a semiconductor detector with excellent time resolution, which has a signal amplification function inside the sensor and can obtain a sufficiently large signal even with a thin detector. LGAD is currently researching applications for future accelerator experiments and PET-CT sensors for medical use, etc. We measured the electronic characteristics and evaluated the time resolution, and confirmed that the radiation resistance and that there was a time resolution of about 30 ps. However, it is known that there is position dependency depending on the incident position of the signal particle, and there is a possibility that there is a difference in the time resolution of the incident signal due to the difference in the amplification factor.

In this study, we conducted a beam test using Fermilab's 120 GeV proton beam, and evaluated the time resolution and the relationship between the signal amplification factor and the incident position of the signal particle. Until now, the time resolution was evaluated using the beam from the accelerator, but an amplifier for evaluating the time resolution of LGAD using a beta source was created, and the time resolution was evaluated using the beta source. ACLGAD has been devised as a sensor with a structure that improves the non-uniformity of the amplification factor for the practical application of LGAD. For ACLGAD, we verified whether a uniform amplification factor could actually be obtained using TCAD simulation.

### Submission declaration

Original and unpublished

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**Presenter:** ONARU, Kyoji (University of Tsukuba (JP))

**Session Classification:** POSTER

**Track Classification:** New ideas and future applications

Contribution ID: 316

Type: ORAL

## Test results from the RD53A pixel readout chip and design status of its successor

*Tuesday, December 17, 2019 10:20 AM (20 minutes)*

The RD53 Collaboration has been tasked with the development of Pixel detector readout chips for the upgrades of the silicon detectors of the ATLAS and CMS experiment for the HL-LHC era. This talk will summarise the results achieved with the first large size demonstrator chip developed by the RD53 collaboration, named RD53A. RD53A contains 76,800 pixels with 50 by 50  $\mu\text{m}^2$  pitch. RD53A features three analog front-ends which have been characterised extensively and all fulfil the RD53A specification of being very low-noise and enabling thresholds of 1000  $e$  and less. Based on these results each experiment has chosen the analog front-end to be featured in their Pixel detector readout chip. Furthermore RD53A has been used by each experiment for sensor characterisation as well as a foundation to design and test the system architecture and components of their future Pixel detectors. The successor to RD53A will be RD53B, which will serve as a common virtual baseline from which each experiment will derive their readout chip to match the requested size and front-end choice. The first chip to be derived from RD53B will be ITkPixV1 the pre-production readout chip for the ATLAS Pixel detector upgrade, which will be submitted for production in Fall 2019. The lessons learned from RD53A and how they influenced the RD53B will be discussed, as well as a general overview of new features of the RD53B design.

### Submission declaration

Original and unpublished

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**Presenter:** HEIM, Timon (Lawrence Berkeley National Lab. (US))

**Session Classification:** Session7

**Track Classification:** Large scale applications

Contribution ID: 317

Type: POSTER

## Fast in-pixel readout for a CMOS pixel sensor prototype developed for the CEPC vertex detector

*Saturday, December 14, 2019 2:24 PM (1 minute)*

The proposed Circular Electron Positron Collider (CEPC) imposes new challenges for the vertex detector in terms of material budget, spatial resolution, readout speed, and power consumption. CMOS Pixel Sensor (CPS), as one of the promising candidate technologies, has been studying within the CEPC vertex detector R&D activities since 2015. According to the latest collider design and study on the beam-induced background, the highest hit rate for the vertex detector is expected to be  $\sim 107/\text{cm}^2/\text{s}$ . In addition, the readout system should meet the 25 ns bunching spacing for the Z pole. A CPS prototype with a high data rate (120 MHz) has been developed in a 180 nm CMOS process. This talk presents the dedicated improvements on the design of in-pixel readout to achieve a pixel pitch of 25  $\mu\text{m}$  and a fast readout capability of 40 MHz. The analog front-end is derived from the ALPIDE (ALice Pixel DEtector) chip. Improvement on the analog front-end is made to obtain a faster-rising edge with a time walk less than 25 ns. Moreover, two new fast in-pixel digital readout designs have been implemented: an FE-I3-like scheme and an ALPIDE-like scheme. The two variations employ the same double-column drain architecture. In the FE-I3-like pixel, some modifications on the pixel address generator are made to save area. In the ALPIDE-like logic, the hit storage registers have been replaced by an edge-triggered flip-flop, leading to a smaller pixel size and preventing repeated hit readout before the analog front-end resets. The priority address encoder block has been modified to boost its speed to 40 MHz. When a hit is detected in one of the pixels, the end of column circuitry stores the current time stamp with a resolution of 25 ns. The data whose timestamp matches with the trigger (with a time window of 175 ns) are buffered for output in case of trigger mode. The designed prototype is in fabrication and expected to be characterized this November.

### Submission declaration

Original and unpublished

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**Track Classification:** Pixel sensors for tracking

Contribution ID: 318

Type: ORAL

## Imaging and spectral performance of a 60 $\mu\text{m}$ pitch CdTe double-sided strip detector

*Sunday, December 15, 2019 3:00 PM (20 minutes)*

Semiconductor detectors with high energy efficiency in the range at several 10 keV are now playing an important role in various research fields; from X-ray astronomy to non-destructive material analysis and in vivo medical imaging. We have been working on a double-sided strip detector based on high energy resolution Cadmium Telluride (CdTe) diode.

In this presentation, we will present the performance of a 60  $\mu\text{m}$  pitch CdTe Double-sided Strip Detector (CdTe-DSD), which was originally developed for the focal plane detector of hard X-ray telescope to observe the Sun. The detector has a thickness of 750  $\mu\text{m}$  and has 128 strip electrodes orthogonally placed on both sides of the detector and covers energy range from 4 keV to 80 keV. The width of the strip electrode is 50  $\mu\text{m}$  and the gap between the strips is 10  $\mu\text{m}$ . Studies of uniformity and effects of charge sharing are of importance in order to provide accurate imaging. For this, we constructed a simple imaging system using a 5 mm thick Tungsten plate that has a pinhole collimator with a diameter of 100  $\mu\text{m}$  and an opening angle of 40 degrees. In order to make evaluation of the detector in a laboratory easy, we have developed a new type of sealed radioisotope (RI) in collaboration with the Japan Radioisotope Association. The RI is mixed with resin and injected into micro tubes with different diameters ranging from 0.167 mm to 1 mm with a pattern that is suitable for testing how accurately we can reconstruct the fine structure of target sources. By using these setups, we obtained 1.3 keV energy resolution at 59.5 keV peak (FWHM). In terms of position resolution, after applying depth corrections of interaction and charge sharing between strips, we obtained a position resolution smaller than the strip pitch of 60  $\mu\text{m}$ .

### Submission declaration

Original and unpublished

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**Presenter:** Mr NAGASAWA, Shunsaku (Kavli IPMU)

**Session Classification:** Session3

**Track Classification:** Applications in biology, medicine, medical equipments

Contribution ID: 319

Type: ORAL

## Depleted monolithic active pixel sensors in 180 nm TowerJazz and 150 nm LFoundry Technology

Monday, December 16, 2019 11:20 AM (20 minutes)

The planned upgrade of LHC leading to the High-Luminosity Large Hadron Collider (HL-LHC) imposes new requirements on the detectors in terms of particle rates and radiation. We have addressed these demands by developing depleted monolithic active pixel sensors (DMAPS) employing high resistivity substrates and high bias voltage at the same time. Full size pixel matrix prototypes with complete readout architecture have been designed and characterized, one employing a large electrode and one a small electrode approach in LFoundry 150 nm and TowerJazz 180 nm technology, respectively.

These prototypes, LF-Monopix and TJ-Monopix, use a column drain readout architecture. LF-Monopix is designed with a large charge collection electrode where readout electronics are placed inside which generally offers homogeneous electrical field in the sensor and short drift distances. TJ-Monopix employs a small charge collection electrode with separated readout electronics and an additional n-type implant to achieve full depletion of the sensitive volume.

This approach offers a low detector capacitance and smaller achievable pixel size at a low power consumption. Different flavors in both designs allow for a study of minor modifications in the pixel design.

The chips have been characterized with regard to their usage in high radiation environments like the future ATLAS ITk at HL-LHC.

In this talk, recent results from lab tests with radioactive sources and X-ray irradiations will be presented. Furthermore, an overview of ongoing work towards future chips in both CMOS technologies will be shown.

### Submission declaration

Original and unpublished

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**Presenter:** BESPIN, Christian (University of Bonn (DE))

**Session Classification:** Session6

**Track Classification:** Pixel sensors for tracking



Contribution ID: 320

Type: POSTER

## Development of a Neutron Imaging Sensor using INTPIX4, SOI Pixelated Silicon Devices

*Saturday, December 14, 2019 2:11 PM (1 minute)*

We have developed a neutron imaging device based on the INTPIX4 SOI pixelated silicon sensors. INTPIX4 is an integration-type sensor with  $17\ \mu\text{m} \times 17\ \mu\text{m}$  pixel circuit array on a SOI wafer, in which correlated double sampling (CDS) circuits and storage capacitors are implemented for synchronized operation with outer trigger timings. The number of pixels is  $832 \times 512$  and effective area is  $14.1\ \text{mm} \times 8.7\ \text{mm}$ . Readout time is  $0.3\text{-}0.4\ \mu\text{s}/\text{pixel}$ . Maximum frame rate is  $70\text{-}90\ \text{Hz}$ . Float Zone (FZ) silicon wafer of  $500\ \mu\text{m}$  thickness is used for the sensor's substrate, where its resistivity is a few k Ohm. Aluminum layer with  $200\ \text{nm}$  is coated on back side of the sensor in the fabrication process. We coat a enriched  $^{10}\text{Boron}$  of  $200\ \text{nm}$  thickness on top of this aluminum layer, which converts neutrons to energetic charged particles, daughter nuclei from the neutron capture reaction. The nuclei make charges in the active area of the sensor and its charge cluster indicate a position of neutron. In this presentation, we will show a production process of the conversion layer and a status of property tests of this device in neutron imaging.

### Submission declaration

Original and unpublished

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**Presenter:** KAMIYA, Yoshio (University of Tokyo (JP))

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for imaging

Contribution ID: 321

Type: POSTER

## Optical Blocking Performance of CCDs Developed for the X-ray Astronomy Satellite XRISM

*Saturday, December 14, 2019 3:15 PM (1 minute)*

We have been developing P-channel Charge-Coupled Devices (CCDs) for the upcoming X-ray Astronomy Satellite XRISM, planned to be launched in 2022. While the basic design of the CCD camera (Soft X-ray Imager; SXI) is almost the same as that of the lost Hitomi (ASTRO-H) observatory, we are planning to improve several critical points on the basis of Hitomi's in-orbit data. One of the largest problems recognized in the Hitomi data is so-called light-leak events, which were only found in the data taken during time when the backside of the spacecraft is toward the day earth. The main light paths are originating from holes opened for other instruments on the back plane of Hitomi. Although XRISM is designed to close these holes to block the outside light, we further improved the optical blocking performance of the CCDs as a kind of fail-safe design. There are two origins that cause light-leak events: One is "pinholes" found on the aluminum optical blocking layer (OBL) deposited on the surface of the CCDs. The other is an end-surface leakage that happens near the physical boundaries of the imaging areas. To suppress the generation of pinholes, which is considered to be a deterioration of the aluminum layer, we adopted a double-layer OBL with an 100+100-nm thickness. We also added an extra aluminum layer on the backside of the CCDs to block light from a transparent die bonding sheet, which is the main path of the end-surface leakage. We developed test sample CCDs and irradiated optical/infrared LED light on them to evaluate their optical blocking performance. As a result, the light leak was effectively reduced compared with that of Hitomi's CCDs. We thus conclude that the light leak found in Hitomi will be addressed by these two new designs. We here report on the details of the optical blocking performance of flight-model CCDs for XRISM.

### Submission declaration

Original and unpublished

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**Presenter:** UCHIDA, Hiroyuki (Kyoto University)

**Session Classification:** POSTER

**Track Classification:** Applications in astrophysics

Contribution ID: 324

Type: ORAL

## Evaluation the first SOI pixel detector with 3D integration technology.

*Sunday, December 15, 2019 5:40 PM (20 minutes)*

In HSTD11, we reported a SOI pixel sensor, SOFIST Ver.4, for the International Linear collider using 3D integration technology. In SOFIST4, we had integrated preamplifier, comparator and 3-stage charge and timestamp memories all within  $20 \mu\text{m} \times 20 \mu\text{m}$  pixel area. This chip would satisfy the requirements for the linear collider vertex detector: the low hit occupancy, low material budget and high spatial resolution.

To integrate the complex functions within the small pixel area, a 3D integration technology was adopted. The functions, and the sensor were separated to two silicon chips. The lower chip consists of the pixel sensor, preamplifier and the comparator while the upper chip houses the logic circuits and analog memories. *Micro gold bumps* were produced on both the chips using photolithography method to combine both the chips. The analog and comparator outputs from the lower chip are connected to the upper chip in each pixel. The chip size can be thinned out to  $50 \mu\text{m}$  after the 3D integration.

In 2019, the first prototype was delivered and its intense evaluation is in progress.

In this presentation, we will review the 3D integration technology, SOFIST4 chip concept and results from the ongoing evaluation.

### Submission declaration

Original and unpublished

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**Presenter:** TSUBOYAMA, Toru (KEK)

**Session Classification:** Session4

**Track Classification:** Pixel sensors for imaging

Contribution ID: 325

Type: ORAL

## Demonstrator for a proton beam computed tomography system at MedAustron

*Sunday, December 15, 2019 3:40 PM (20 minutes)*

MedAustron is a center for ion therapy and research in Wiener Neustadt, located about 50km south of Vienna, the capital of Austria. The facility provides three beam lines for cancer treatment with proton beams at energies up to 252.7 MeV as well as carbon ion beams up to 400 MeV/u.

In addition to this medical application, the facility features a further beamline, which is exclusively reserved for non-clinical research. The research beam line is currently being commissioned for even higher proton energies of up to 800MeV.

Currently, treatment planning for proton therapy is based on x-ray computed tomography, which implies certain sources of inaccuracy in calculation of stopping power (SP). A more precise method to acquire the SP is to directly use high energy protons and perform proton computed tomography (pCT). With this method, the ions are tracked before entering and after leaving the patient and finally their residual energy is measured at the very end.

Therefore, a pCT demonstrator, comprising a tracking telescope made from double-sided silicon strip detectors and a residual energy calorimeter was set up and recently, first measurements with this pCT prototype were performed in a beam test at MedAustron.

This contribution introduces the principle of ion imaging with proton beams in general as well as the design of the pCT prototype. Moreover, first results from recent test beams and ideas for future developments will be presented.

### Submission declaration

Original and unpublished

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**Presenter:** PAULITSCH, Peter (Austrian Academy of Sciences (AT))

**Session Classification:** Session3

**Track Classification:** Applications in biology, medicine, medical equipments

Contribution ID: 326

Type: POSTER

## Beam background study for the Belle II Silicon Vertex Detector

*Saturday, December 14, 2019 3:08 PM (1 minute)*

The Belle II experiment aims to accumulate  $50 \text{ ab}^{-1}$  of  $e^+e^-$  collision data at the SuperKEKB asymmetric energy collider (Tsukuba, Japan). The first physics data using all Belle II detectors were taken in spring 2019.

In the vast physics program of the Belle II experiment, the vertex detector plays a crucial role for the determination of the B-mesons decay vertices. It consists of two inner layers of pixelated silicon detectors and four outer layers of double-sided silicon strip detectors (SVD).

To achieve a design luminosity of  $8 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ , 40 times higher than the recorded luminosity of its predecessor, the SuperKEKB collider squeezes the beams to a vertical size of 50 nm ("nano-beam scheme") and doubles the beam currents.

Therefore, the detectors are required to tolerate intense beam backgrounds due to the upgrade. During the 2019 spring run we measured beam background levels in the SVD, as the strip occupancy of each sensor. With the low initial luminosity, the observed beam backgrounds mostly originated from Touschek and beam-gas scattering in individual beams. Since the scattering rates show different dependencies on beam conditions, such as the beam current, beam size and pressure, these contributions can be decomposed. We estimated the background rate and spatial distribution of each contribution and compared them with simulated ones. The results enable us to predict the background levels at increased beam currents and luminosity in the coming years. They also hint remedies to mitigate the beam backgrounds. In the poster, we will report the results of the beam background studies and the prospect for the SVD beam backgrounds in the future operation.

### Submission declaration

Original and unpublished

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**Co-author:** ON BEHALF OF THE BELLE II SVD AND BACKGROUND GROUPS

**Presenter:** TANIGAWA, Hikaru (The University of Tokyo)

**Session Classification:** POSTER

**Track Classification:** Large scale applications

Contribution ID: 327

Type: POSTER

## Metal materials evaluation by X-ray using SOI pixel detector

*Saturday, December 14, 2019 2:12 PM (1 minute)*

In recent years, the aging of metal structures has become a problem in various social infrastructures that form the basis of livelihood and production. Therefore, various inspections are performed on metal structures to evaluate their degree of fatigue and the remaining life. Residual stress is one of the indicators for evaluating the soundness of metal structures, and many evaluation technologies have been developed since long ago. However, there are few conventional residual-stress-measurement methods used for on-site measurement, but they have destructive nature of inspection and take long measurement time. Therefore, we have developed a high-speed and compact X-ray residual-stress-measurement device equipped with a high-sensitivity, high-definition, charge-integration type silicon-on-insulator (SOI) pixel detector, INTPIX4, and we studied quality-evaluation techniques for metal materials.

Previous studies have shown that residual stress can be measured in less than 1 second by using a measurement device with an SOI pixel detector. In this study, we will introduce the characteristics of the installed INTPIX4, specification of the measurement device, and the technology for analyzing the detected X-ray images. Furthermore, we will report technologies on the data-processing methods for analyzing and measuring residual stress, aiming to evaluate the soundness of metal structures and inspect machines and metal products.

### Submission declaration

Original and unpublished

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**Presenter:** Dr MITSUI, Shingo (Kanazawa university)

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for imaging

Contribution ID: 328

Type: POSTER

## The Silicon Sensors for the High Granularity Calorimeter of CMS

*Saturday, December 14, 2019 3:09 PM (1 minute)*

During the Long Shutdown 3 (LS3) of the Large Hadron Collider (LHC), around 2024-2026, significant parts of the CMS detector will be upgraded to allow an efficient data taking during the subsequent High Luminosity LHC phase (HL-LHC). The HL-LHC will have a factor 5 higher instantaneous luminosity - resulting in a factor 5 higher event "pileup", and a factor 10 increase in integrated luminosity by ~2037 compared with the end of LHC operation. Especially the forward calorimeters will be exposed to unprecedented levels of radiation and pileup. The CMS collaboration will, during LS3, replace the existing endcap calorimeters with a new High Granularity Endcap Calorimeter (CE). It features unprecedented transverse and longitudinal segmentation for both electromagnetic (CE-E) and hadronic (CE-H) compartments. This will facilitate particle-flow calorimetry, where the fine structure of showers can be measured and used to enhance pileup rejection and particle identification, whilst still achieving very good energy resolution. The CE-E and a large fraction of CE-H will consist of a sandwich structure with silicon sensors as active detector material. The sensors will be of hexagonal shape, maximizing the available area of 8-inch wafers and covering  $600\text{m}^2$  in total. Each sensor consists of either 192 or 432 individual hexagonal diodes, each of  $0.5 - 1.1\text{ cm}^2$  in size, without any common biasing structure. Biasing and readout of each diode is performed on the module level through a printed circuit board (PCB), which is glued onto the sensor and equipped with readout ASICs, connected by wire-bonding through holes in the PCB to the sensor. In this talk, we present the current status of the HGCal project, with special focus on the silicon sensors. It will show the R&D path being followed for the sensors, the design of the modules and larger structures (cassettes, disks) to build up the whole detector. Optimization studies of the sensors, measurement results of the first prototypes, irradiation studies and beam tests will be shown.

### Submission declaration

Original and unpublished

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Contribution ID: 330

Type: ORAL

## The Phase 2 upgrade of CMS Outer Tracker

*Tuesday, December 17, 2019 11:20 AM (20 minutes)*

The Large Hadron Collider(LHC) at CERN will undergo major upgrades to be able to deliver peak instantaneous luminosities of about  $5 - 7.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$  by 2026. This High Luminosity upgrade of the LHC (HL-LHC) is expected to deliver a total of about  $3000-4500 \text{fb}^{-1}$  during ten years of operation. At the nominal instantaneous luminosity of the HL-LHC, a single bunch crossing will produce 140-200 proton-proton collisions. The current CMS outer tracker and the CMS Phase-1 pixel detector will not be able to survive the harsh operating conditions of the HL-LHC period.

The CMS experiment will install a new silicon tracker for HL-LHC. The Phase-2 Outer Tracker (OT) will have increased radiation hardness, higher granularity and track separation, compatibility with higher data rates, and a longer trigger latency. In addition, the OT will provide tracking information to the Level-1 trigger, allowing trigger rates to be kept at a sustainable level without sacrificing physics potential. To achieve this, the OT will be made up of modules with two closely spaced sensor readout by a single ASIC which can correlate data from both sensors to form short track segments called stubs which will be used in tracking at Level-1. In this contribution, the design of the CMS Phase-2 OT, the technological choices and highlights about research and development activities will be reported.

### Submission declaration

Redundant (overlaps with already published)

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**Session Classification:** Session8

**Track Classification:** Strip sensors

Contribution ID: 331

Type: POSTER

## Particle tracking and radiation field characterization with Timepix3 in ATLAS

*Saturday, December 14, 2019 2:31 PM (1 minute)*

Four hybrid active pixel detectors of Timepix3 technology, installed in the ATLAS experiment, were taking data from April 2018 until the end of Run-2 data taking period (December 2019). They are arranged in two stacks with face to face geometry allowing coincidence measurement of penetrating particles from the interaction point (IP) or beam pipe and are synchronized with the LHC orbit clock. The Timepix3 detectors used have silicon sensor layers of thickness 500  $\mu\text{m}$ , segmented into a square matrix of 256 x 256 pixel with a pixel pitch of 55  $\mu\text{m}$  (active area: 1.98  $\text{cm}^2$ ). The data-driven readout scheme allows a continuous and simultaneous measurement of ToT and ToA in each pixel. It was shown elsewhere, that the time granularity of 1.6 ns is sufficient to resolve the LHC bunch structure and allows 3D track reconstruction with resolution around 55  $\mu\text{m}$ . In the present contribution, we describe the method of identification of particles interacting in the sensors synchronized with LHC orbit clock utilizing their precise 3D tracking and ToF as well as the coincidence information. We present the stopping power spectra and particle impact angle maps measured during collisions. Hereby, we show that in individual bunch crossings, aligned MIP particle tracks originating from IP, which overlay the otherwise more random and frequent background tracks, can be well recognized.

### Submission declaration

Original and unpublished

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**Presenter:** BILLOUD, Thomas Remy Victor (Universite de Montreal (CA))

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for tracking

Contribution ID: 332

Type: POSTER

## The miniaturized read-out interface “SPECTRIG MAPD” dedicated for silicon photomultipliers

*Saturday, December 14, 2019 2:04 PM (1 minute)*

The new pocket size read-out interface device dedicated for silicon photomultipliers (SiPM) has been designed and developed. While it was designed as a miniaturized and low power device it still provides a wide spectrum of functionality necessary for measurements and testing of SiPMs and SiPM based detectors. Full signal processing has been integrated within the device involving variable gain amplification, filtration and digitization. Signal acquisition can be performed with sampling frequency 400 MSa/s at 12 bit resolution or 600 MSa/s at 8 bit resolution while achieving full waveform capture & download rate about 20 000 events per second. The read-out interface is fully powered from the USB bus allowing operation without need of additional power line connection. An integrated bias source can be set in range from 0V to +200V with 12 bit precision. The read-out interface is primarily dedicated for spectroscopy purposes. There are two input signal channels with different optimization regarding the signal gain to cover a low stimulus in range of single photo-electron detector response as well as to cover a high stimulus corresponding to detector response operated with scintillator registering gamma radiation in order of MeVs. Both input channels are equipped with fine gain adjustment in range from -9 dB to 26 dB with 1 dB step in addition to the fixed gain of each signal channel. The FPGA based design of the read-out interface allowed implementation of advanced triggering functionality like a data driven trigger, external trigger, gating of trigger to extend read-out interface capability even further in a way of complex experiments. A set of functional tests and experiments with SiPM called micropixel avalanche photodiode (MAPD) and MAPD based detectors have been performed to characterize real properties of the read-out interface.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** New ideas and future applications

Contribution ID: 333

Type: POSTER

## Data-acquisition system developments for ATLAS pixel QA/QC test toward High Luminosity LHC

*Saturday, December 14, 2019 3:11 PM (1 minute)*

In preparation for the High luminosity LHC (HL-LHC) upgrade, the whole ATLAS inner tracker will be replaced by a new silicon detector tracker. The innermost region will be covered by silicon pixel detectors as a high density of produced particles is expected. In order to operate in such an environment, high-resolution sensor and high-speed readout system is required. At the moment the RD53A, the prototype of front-end readout chip, and a data-acquisition system (the YARR system) based on commercial FPGA and dedicated software for quality assurance (QA) and quality control (QC) test have been developed.

Due to its high density of sensor channels, output speed from RD53A is at maximum 1.28 Gbps per line, which is sixteen times faster than the readout front end chip currently used in ATLAS pixel system. The data-acquisition system needs to establish communication in such high speed at QC test, to validate data-acquisition path, and to optimize the procedure for data taking at high speed. From the QC perspective this optimization allows us to test large numbers of modules in parallel exploiting the DAQ lines speed reducing the time needed for tests.

Another challenging point is the novel concept of readout structure planned for the operation after installation. In HL-LHC, large parts of the ATLAS DAQ system infrastructure is going to be shared among all sub detectors, using FELIX systems, while current ATLAS DAQ system are dedicated for each sub detector. This means that all processes done in the present DAQ system hardware need to be overhauled into software running on the new DAQ system. In order to minimize the differences between the DAQ system for operation and QC test, we introduced prototype FELIX system into the DAQ path of YARR system.

In this report, an established DAQ structure for QA and QC test for the new pixel detector will be introduced. And results from basic QC tests of the pixel detector with new readout chip will be shown.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Large scale applications

Contribution ID: 334

Type: POSTER

## The MuPix sensor for the Mu3e experiment

*Saturday, December 14, 2019 2:32 PM (1 minute)*

The Mu3e experiment will search for the charged lepton flavour violating decay  $\mu^+ \rightarrow e^+ e^- e^+$  with a sensitivity of one in  $10^{16}$  decays (in phase II). To reach this sensitivity a momentum resolution of 0.5 MeV/c and a vertex resolution of about 200  $\mu\text{m}$  is required.

The particle rate is given by the more than  $10^9$  muon stops per second. All the hits will be readout using a continuous readout system. To achieve the specifications High Voltage Monolithic Active Pixel Sensors (HV-MAPS) are used for all layers of the tracking system. The chip developed for Mu3e is called MuPix. In the last years several prototypes were designed and tested. The first large prototype is the MuPix8 ( $1 \times 2 \text{ cm}^2$ ) which has been successfully tested in the lab and using test beams. The next large MuPix, MuPix10, will be submitted by the end of 2019 and represents a final version prototype. The matrix contains  $250 \times 256$  pixels, each pixel with size  $80 \mu\text{m} \times 80 \mu\text{m}$ . The total chip size is  $20.66 \times 23.18 \text{ mm}^2$ . The signal is amplified in the pixel and then transmitted as an analog signal to the readout cell located in the chip periphery where the signal is discriminated with two comparators. The time information consists of 11 bits for the hit arrival time and 5 bits for the time-over-threshold. MuPix10 is based on a 180 nm HV-CMOS process.

In this talk the measurement results of the MuPix8 and the final design of the MuPix10 will be presented.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Pixel sensors for tracking

Contribution ID: 336

Type: ORAL

## Annealing of proton radiation damages in Si-PM at room temperature

*Tuesday, December 17, 2019 5:00 PM (20 minutes)*

CAMELOT (CubeSats Applied for MEasuring and LOcalizing Transients) project plans to launch a group of nano-satellites for detection and position determination of short gamma-ray bursts and other transients. Detector is designed to consist of CsI (TI) scintillator and Silicon Photomultipliers (Si-PMs). Si-PMs can be driven with low voltage (~50 V), high gain (10e6) and small size (~mm), which are suitable for the nano-satellite platform. However, they have been little used in space, and their damages of orbital radiations have not been investigated in detail. As a purpose of this study, we investigated how Si-PM performance recovers after proton-beam irradiation.

In this experiment, we irradiated Si-PMs (Hamamatsu Photonics K.K: S13360-6050CS) with dose of 300, 1000 and 5000 rad of 200 MeV protons in The Wakasa-wan Energy Research Center in November 2018. The dose of 100 rad is yielded by  $6.2 \times 10^8$  200 MeV protons and equivalent to the same number of irradiation with 1 MeV neutron. Then, we measured the performance at two epochs, just after irradiation and after 7 month. Si-PMs were stored at room temperature during these 7 months.

We measured the energy spectrum of X-ray of  $^{241}\text{Am}$  by using  $1 \text{ cm}^3$  CsI (TI) and Si-PM irradiated with 300 rad of proton. It shows recovery of the energy threshold by a factor of ~2. Si-PM irradiated by 5000 rad protons had a higher noise and  $^{241}\text{Am}$  signals were not able to be detected just after irradiation. As a result of room-temperature annealing during 7 month, a lower energy threshold is achieved and 59.5 keV peak of  $^{241}\text{Am}$  is visible. In this paper, we report the recovery of various properties of Si-PM.

### Submission declaration

Original and unpublished

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**Presenter:** Mr NAOYOSHI, Hirade (Dept. of Physical Science, Hiroshima Univ.)

**Session Classification:** Session10

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 337

Type: ORAL

## 3D Trenched-Electrode Pixel Sensors: design, technology and initial results

*Monday, December 16, 2019 10:00 AM (20 minutes)*

As the luminosities produced by particle collider experiments increase in the next few years, increasing the pile up, the tracking detectors in these experiments will require improved spatial and timing resolution to distinguish between different tracks as well as having the required radiation hardness to survive for the duration of the experiment. 3D sensors have already been proven as a viable and inherently radiation hard technology. While encouraging timing results have been obtained from small-pitch 3D test structure, new approaches are also being investigated to meet the challenges of the coming years.

One such approach, pursued in the framework of the INFN TIMESPOT project, is the development of 3D sensors with trench electrodes. The trench geometry will provide more uniform electric and weighting fields than in current devices, allowing for good timing resolution, while also maintaining or improving upon the usual advantages of a 3D geometry.

The fabrication of the first batch of devices, designed with input from TCAD simulations, consisting of TIMEPIX compatible pixel sensors, as well as a number of test devices to study the performance of different pixel geometries, was carried out at FBK (Trento, Italy) on 6-inch diameter, p-type, Si-Si Direct Wafer Bonded substrates having a 150- $\mu\text{m}$  thick FZ active layer. Initial I-V measurements of the TIMEPIX-compatible sensors and other small pixel arrays was performed making use of a temporary metal layer. Results highlighted good intrinsic properties, with leakage current density of the order of a few pA per pixel and breakdown voltage in excess of the measurement limit of 50V. However, a non-negligible density of process defects was also observed, that makes the yield of the large area sensors quite low.

This presentation will report on the design and technological aspects, and report results from the electrical characterization of pixels and test structures.

### Submission declaration

Original and unpublished

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**Session Classification:** Session5

**Track Classification:** Pixel sensors for tracking



Contribution ID: 338

Type: POSTER

## Performance evaluation of GAGG/LFS scintillator+MPPC array readout with ASIC

*Saturday, December 14, 2019 3:16 PM (1 minute)*

In the soft gamma ray region (100 keV-10 MeV), Compton scattering is the dominant physical process, and it is an unexplored region where observation has not progressed because the background is rather high compared to the signal from celestial sources. In this region, the direction and energy of incident gamma rays can be determined by using Compton camera technique where photons are Compton scattered by a scatterer and then fully absorbed by an absorber. Recently, semiconductor detectors with excellent energy and position resolution are used in the Compton camera, but when observing higher energy than 1 MeV, it is required to develop an array-type detector in which scintillators with excellent gamma ray stopping power are assembled in the form of pixels as an absorber. So we constructed a gamma ray detector by combining two types of scintillator array detectors with an MPPC array, and evaluated the performance by reading out the signals from the MPPC with a low-power integrated circuit (ASIC) manufactured by IDEAS in Norway. One of the two types of scintillators is a GAGG ( $\text{Ga}_3\text{Al}_2\text{Gd}_3\text{O}_{12}$ ) scintillator, and the other is an LFS scintillator. The scintillator array is 2.5 cm x 2.5 cm in size and is coated with  $\text{BaSO}_4$ -based white paint as a reflector except for the side optically coupled to the MPPC. The energy resolution of the GAGG array was about 7% at 662 keV at room temperature. This is almost equivalent to the typical energy resolution. In this presentation, we report on the performance evaluation of GAGG and LFS scintillator array.

### Submission declaration

Original and unpublished

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**Presenter:** Mr NOBASHI, Daiki (Nagoya University)

**Session Classification:** POSTER

**Track Classification:** Applications in astrophysics

Contribution ID: 339

Type: ORAL

## New Pixel Detector Concept 'DuTiP' for Belle II Upgrade and the ILC with an SOI Technology

*Sunday, December 15, 2019 5:00 PM (20 minutes)*

Belle II experiment was successfully started. The first data for physics with full Belle II detector were taken in 2019 and  $50\text{ab}^{-1}$  data will be accumulated by 2027. A discussion of an upgrade plan for Belle II and SuperKEKB is started. The instantaneous luminosity by the upgraded SuperKEKB is 5 times larger than current design luminosity for SuperKEKB ( $8 \times 10^{35} \text{cm}^{-2} \text{s}^{-1}$ ) and the upgraded Belle II will collect data sample of  $250\text{ab}^{-1}$ . In such high luminosity environment, current DEPFET pixel detector is hard to operate due to too high occupancy since the readout scheme of DEPFET is rolling shutter mode with a  $20\mu\text{s}$  frame.

We have invented a new pixel detector concept 'DuTiP' (Dual Timer Pixel) which is a binary pixel detector with a trigger signal based global shutter readout scheme. A binary hit information is stored in a down counting timer inside a pixel whose initial value is set as trigger latency plus 1 clock (around  $5\mu\text{s}$ ). If the trigger signal is received when the timer is 1 (0 or 2), the hit information is readout as current (previous or next) timing. To take into account for multiple hits during trigger latency, two timers are equipped in a pixel. The clock speed is important parameter for the occupancy and data size. We tentatively decided the clock speed as 15.9MHz (62.9ns). The requirement of spatial resolution at Belle II is around  $10\mu\text{m}$  for both  $z$  and  $r$ - $\phi$  directions, thus  $35\mu\text{m}$  pixel size is selected. This pixel detector can be also used for layer 7 and 8 of ILC vertex detector which requires single bunch (554ns) time stamping capability and moderate spatial resolution of  $10\mu\text{m}$  in  $r$ - $\phi$  direction.

We report the concept of 'DuTiP' and the status of development of the pixel detector with an SOI technology for Belle II upgrade.

### Submission declaration

Original and unpublished

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**Presenter:** Dr ISHIKAWA, Akimasa (KEK)

**Session Classification:** Session4

**Track Classification:** Pixel sensors for tracking

Contribution ID: 340

Type: ORAL

## A Reconfigurable CMOS Sensor for Tracking, Pre-Shower and Digital Electromagnetic Calorimetry

Monday, December 16, 2019 12:00 PM (20 minutes)

Recent advances in CMOS imaging sensor technology have led to designs able to withstand much higher radiation levels, up to those required at hadron colliders for all but the innermost layers. Also, with stitching, wafer scale devices have been fabricated on the same process as used for the prototypes described in this submission, for applications such as, for example, direct electron detection in transmission electron microscopy.

A small sensor prototype has been designed and fabricated in the TowerJazz 180nm CMOS imaging process. The prototype has a pixel matrix of 64x64 pixels with a pitch of 55x55  $\mu\text{m}$  and reads out using fast logic at 40 MHz. Each pixel contains four collection electrodes, trimming logic, pre-amplifier, shaper, comparator and discriminator with digital output. It can be reconfigured to function as either a binary short strip sensor, for particle tracking including as a pre-shower, or as a pad sensor, counting the number of pixels above threshold for digital calorimetry.

As well as providing a seamless transition from outer tracking to EM calorimetry, for optimal use of particle flow algorithms, digital calorimetry also can give excellent energy resolution. This concept is proposed as a possible option for future digital calorimeters able to read-out at LHC collision rates with good radiation hardness and realisable in low cost commercial technologies for equipping large areas.

The presentation contains both the results on physics performance simulation in a FCC-hh context and the characterisation of the prototype sensor. The summing logic is demonstrated and the analogue pixel performance is validated by illuminating a test pixel within the matrix with a laser of wavelength of 1064 nm. The absolute laser intensity is calibrated such that the injected charge is similar to that expected for a MIP. The measurements of the pre-amplifier and shaper signals are compared to Cadence simulations. Laser illuminations in the digital pixel area and the response measured using a threshold scan confirm successful digital functionality in strip and pad operation modes.

### Submission declaration

Original and unpublished

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**Presenter:** Prof. ALLPORT, Philip Patrick (University of Birmingham (UK))

**Session Classification:** Session6

**Track Classification:** Technologies

Contribution ID: 341

Type: POSTER

## Novel architecture for the analog front-end of Medipix4

*Saturday, December 14, 2019 2:56 PM (1 minute)*

Medipix4 is the latest member of the Medipix family of pixel detector readout chips aimed at high rate spectroscopic X-ray imaging. Unlike its predecessors it will be possible to tile the chip on all 4 sides permitting seamless large area coverage. This presentation focuses on the development of a new architecture for the front-end of Medipix4 capable of event-by-event data processing allowing photon energy reconstruction with charge sharing correction at an increased rate compared with Medipix3. The architecture is particularly well adapted to high-Z detector materials allowing accurate energy binning of incoming hits at a fine pixel pitch.

In order to fulfil the demanding requirements from future users of Medipix4, a novel front-end architecture has been implemented to improve the energy dynamic range, the count-rate capability, and the energy resolution. As the chip can be tiled on 4 sides it is necessary to have a readout pixel pitch which is slightly smaller in one dimension than the sensor pixel pitch. The fan-in required from sensor to readout imposes further constraints on the front-end. Moreover, the architecture is tuned to contact a sensor with either 70  $\mu\text{m}$  or 140  $\mu\text{m}$  pitch

The analog front-end is implemented using a commercial 130 nm deep sub-micron technology process, and the functionality is verified by simulation. Each 70  $\mu\text{m}$  pixel contains a charge sensitive amplifier with a baseline holder to compensate DC leakage currents coming from the sensor, two shapers for implementing the charge sharing correction mode (CSM), followed by discriminators with locally programmable threshold. The linear range of the front-end is extended to 150 keV using a sensor CdTe, implying a 40% enhancement with respect to Medipix3. A feedback circuit in the shaper with a reference current allows a faster return to the baseline, resulting in an expected count rate of 17 Mphotons/mm<sup>2</sup>.s at 10% hit loss for a pixel pitch of 140  $\mu\text{m}$ , and not affected by charge sharing effect, showing a gain of factor 5 with respect to its predecessor.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Pixel sensors for imaging

Contribution ID: 342

Type: POSTER

## Study of Interpad-gap of FBK (UFSD3) and HPK 3.1 Type sensors with Transient Current Technique

*Saturday, December 14, 2019 3:23 PM (1 minute)*

The Phase-II upgrade of LHC to HL-LHC by 2026 allows an increase in the operational luminosity value by a factor of 5-7 that will result in delivering  $3000\text{-fb}^{-1}$  or more integrated luminosity. This amount of data will not just allow an increase in the precision of the Standard Model (SM) measurements but also widen the horizon for Beyond Standard Model (BSM) searches. To achieve high luminosity, a number of interactions per bunch crossings (pileup) will increase up to a value of 140-200. To cope with high pileup rates, precision timing detector (MTD) that will measure minimum ionizing particles (MIPs) with a time resolution of  $\sim 30\text{-}40$  ps and hermetic coverage up to a pseudo-rapidity of  $|\eta| = 3$  is proposed by the CMS experiment. An endcap part ( $1.6 < |\eta| < 3$ ) of MIP timing detector (ETL) will be based on low-gain avalanche detector (LGAD) technology. The third production of Ultra Fast Silicon Detectors (UFSD3) from Fondazione Bruno Kessler (FBK) and Low Gain Avalanche Detectors (LGADs) from Hamamatsu Photonics K.K. (HPK) include  $2 \times 2$  sensors with different structural strategies, in particular, different values of narrower inactive region widths between the pads. These sensors have been designed to study specific features required for the ETL. A comparative study on the dependence of breakdown voltage with the inter-pad gap width for both sensor types has been carried out. Results of measured inter-pad gap widths and spatial mappings within their non-active regions using MIPs (IR light) from the Scanning-Transient Current Technique (Scanning-TCT) set-up will be shown. A fill-factor, which is the ratio of the area within the active region (Gain region) to the area of the total scanning region has been studied. Results on how fill-factor varies depending on temperature (from  $25^\circ\text{C}$  to  $-25^\circ\text{C}$ ) and proton fluence on irradiation will also be shown.

### Submission declaration

Original and unpublished

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Contribution ID: 343

Type: POSTER

## DESIGN OF LARGE SCALE SENSORS IN A 180nm CMOS PROCESS MODIFIED FOR RADIATION TOLERANCE

*Saturday, December 14, 2019 2:16 PM (1 minute)*

The last couple of years have seen a large learning curve in Depleted Monolithic Active Pixel Sensors (DMAPS) fabricated with a process modification for increasing radiation tolerance. Two large scale prototypes: Monopix with a column drain synchronous readout, and Malta with a novel asynchronous architecture have been fully tested and characterised. This experience has shown that certain aspects have to be improved such as charge collection after irradiation and high data rate capabilities. Some improvements resulting from extensive TCAD simulations were verified on a small test chip, miniMalta. A detailed cluster analysis, with different sources, at different biases, for high and low thresholds and before and after irradiation will be covered in detail.

This presentation will further focus on the continuation of the development in this TowerJazz-180 nm technology, with a new submission foreseen for the end of this year, where the new process modifications will be applied on the large scale prototypes. A trigger memory will be as well added in the MonopixV2 chip.

The digital architecture for both chips will be reviewed capable of dealing with data rates of around 80 MHz/cm<sup>2</sup> similar to what it is expected in the outer layer of the ATLAS inner tracker Upgrade. Simulations to study the data rate capability and output bandwidth using realistic hits generated by the ATLAS simulation engine Athena including special techniques like on-chip clustering and data compression will also be presented.

Finally, a longer-term outlook will be covered in the presentation.

### Submission declaration

Original and unpublished

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**Presenter:** FLORES SANZ DE ACEDO, Leyre (University of Glasgow (GB))

**Session Classification:** POSTER

**Track Classification:** Simulations



Contribution ID: 344

Type: POSTER

## Hodoscope with Timepix Detectors for PilsenCube2 Cubesat

*Saturday, December 14, 2019 3:17 PM (1 minute)*

This contribution describes design of Timepix-based hodoscope for cubesat applications, such as PilsenCube2, developed by the University of West Bohemia. This hardware platform consists of two Timepix detectors with silicon 500 $\mu$ m sensors, placed in face-to-face arrangement and rotated relative to each other by 90°, forming a telescope set-up. A copper separator is placed between two sensor layers to distinguish electrons and protons. Besides that, it helps to dissipate heat produced by both detectors. The payload hardware and firmware is designed to support single detector operation as well as dual detector operation mode, in which particle coincidence detection is possible. The hodoscope electronic has been designed with respect to harsh radiation environment present in space. Therefore radiation hardened components such as the flash-based FPGA (Microsemi Smartfusion2 SoC device) and radiation hardened voltage regulators are used.

The device implements independent power supplies, including bias high voltage supply (operating up to 250 V) and auxiliary threshold reference DAC for each Timepix ASIC (sensor layer). All Timepix power supplies can be controlled independently, with the power-control module connected with the APB (Advanced Peripheral Bus) to the microcontroller subsystem (MSS). Considering highly limited achievable data throughput between the cubesat and the ground control station, enhanced on-board data processing has been developed in order to reduce the size of transmitted data. Therefore the original FITPix protocol has been modified in order to allow full integration within the SmartFusion2 SoC to maximally exploit performance of the Cortex-M3 microprocessor.

### Submission declaration

Original and unpublished

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**Presenter:** URBAN, Ondřej

**Session Classification:** POSTER

**Track Classification:** Applications in astrophysics

Contribution ID: 345

Type: POSTER

## ATLASPIX3 – a reticle size HVCMOS pixel sensor designed for construction of multi chip modules

*Saturday, December 14, 2019 2:28 PM (1 minute)*

High voltage CMOS pixel sensors will be used in several particle physics experiments for particle tracking. ATLASPIX3 is the first full reticle size monolithic HVCMOS sensor which has all necessary features for construction of multi chip modules. ATLASPIX3 has been designed for ATLAS pixel upgrade, layer 4, within ATLAS CMOS collaboration. The size of the chip is 2cm x 2.1cm with periphery at one side which makes the chip 3-sides buttable. ATLASPIX3 has been implemented in a standard 180nm HVCMOS process. Each pixel has an area of 50 $\mu$ m x 150 $\mu$ m and contains a large charge collecting electrode implemented as a deep n-well. Pixel electronics is embedded inside the n-well. The p-substrate around the n-well is depleted by applying high voltage bias. To increase the depth of the depleted region, the chips have been implemented on high resistivity substrates. ATLASPIX3 implements the zero-suppressed readout. Upon particle hits, hit words containing time-, amplitude- and spatial information are generated. The readout electronics supports both triggered- and triggerless readout. Trigger latency is programmable up to 25 $\mu$ s and trigger window can be as small as 25ns. The readout electronics can cope with hit and trigger rates expected in the layer 4 of ATLAS high luminosity upgrade. The digital chip interface is based on two lines, one command-input and one data-output. ATLASPIX3 is compatible with RD53 ASIC in terms of physical interface and command and data format. ATLASPIX3 could be used for the construction of CMOS modules for ATLAS or similar experiment where high time resolution, high radiation tolerance, low power and thin sensors are required. The chip is already available and first measurement results are promising. The structure of the sensor and measurement results will be presented.

### Submission declaration

Original and unpublished

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Contribution ID: 346

Type: POSTER

## A Concept for Spatially and Timely Correlated Single Event Effects Detection in Semiconductors Using Timepix3 Pixel Detectors

*Saturday, December 14, 2019 3:06 PM (1 minute)*

Knowing the reliability of electronic systems operating under extreme conditions is crucial, especially in nuclear and space applications. In such environment, the proper functionality of electronic systems is endangered because of Single Event Effect (SEE) occurrence. In our work, we present an experimental setup for measuring fault detection correlated with events occurring in silicon detectors. A replaceable Device Under Test (DUT) is connected to the holder board via soldering pads. I/O signals are processed in a tester, FPGA based board, synchronized with two Timepix 3 readouts.

In this work, we present an electronic system for measuring SEEs timely and spatially correlated with Timepix detectors. The Timepix detector is a semiconductor pixel detector, which contains 256 x 256 pixels. It provides energy or time information for each hit pixel. Our experimental setup consists of FPGA based board synchronized Timepix3 readout and a Device Under Test (DUT).

### Submission declaration

Original and unpublished

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**Presenter:** Dr BROULIM, Jan (University of West Bohemia)

**Session Classification:** POSTER

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 347

Type: ORAL

## High resolution tracking using 3D sensors with partial electrode depth using Timepix3 electronics

3D silicon pixel sensors [1] have low drift times due to their electrode geometry. It is assumed that within the given time resolution, the time-of-arrival (ToA) for every pixel of a track created by a particle would be identical, then, the track z-coordinate can be obtained only from the particle impact and end points.

Partial 3D silicon sensors (electrode depth: 230  $\mu\text{m}$ , thickness: 300  $\mu\text{m}$ ) [2] bump-bonded to the Timepix3 ASIC (65,536 pixels of 55 x 55  $\mu\text{m}^2$ , ToA binning: 1.5625 ns) [3] were used for this investigation.

The detectors were placed in a 40 GeV/c pion beam and a relativistic mixed ion beam at different incident angles. ToA differences within particle tracks (delta-ToA) were studied.

In the region of the sensor where the n and p electrodes are overlapping and parallel to each other, the measured delta-ToA are indistinguishably short at the detector time resolution. Since the electrodes in the sensors do not fully penetrate the bulk, between electrodes tips and the opposite sensor surfaces, we found that delta-ToA is proportional to the particle interaction depth and the applied bias. Delta-ToA increases up to 300 ns as the particle interaction depth moves from the electrode tip towards the sensor surface, from this we can gain multiple additional z-coordinates information of the particle track. In addition, we found that delta-ToA correlates to the interaction position in the xy plane. A subpixel resolution of lower than 11.33  $\mu\text{m}$  can be achieved when particles impact at an angle, this resolution is being improved upon.

We show with simulated and measured data how the ToA information can be used to improve the tracking resolution. The experimental results were reproduced in a simulation and compared with measurements obtained with planar silicon sensors of the same dimensions.

### Bibliography:

- [1] Da Via, C. et al., NIM A 694, pp.321-330 (2012).
- [2] Pellegrini, G. et al., NIM A 699, pp.27-30 (2013).
- [3] Poikela, T. et al., JINST 9(05), p.C05013 (2014).

### Submission declaration

Original and unpublished

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**Presenter:** Mr GAO, Tianqi (University of Manchester)

**Session Classification:** Unknown (Virtual block)

**Track Classification:** Pixel sensors for tracking

Contribution ID: 348

Type: POSTER

## Fabrication and its Performance of a Pixelated Silicon Sensor Integrated with JFET

*Saturday, December 14, 2019 2:18 PM (1 minute)*

In the previous Hiroshima symposium (HSTD11), we presented a detection concept of a pixelated silicon sensor integrated with junction field effect transistor (JFET), fabrication process flow charts of it, and simulation studies based on this detector concept. The JFET is designed to have the cylindrical structure and is used as a switch to readout charges accumulated in the pixelated sensor. We determine detector design parameters such as a distance between the source and the drain, a coverage region of the deep p-well implemented underneath the drain of the JFET, and doping concentration for the deep p-well. All pixels with one row are read in parallel and the next row is then selected by the gate voltage after finishing the reading one row. The photon detection efficiency of the silicon at low energy X-ray is very high so that this detection can be used for direct irradiation method, and the thickness of the active silicon should be twice of the absorption length of the silicon at that energy. We fabricate a pixelated silicon sensor integrated with JFET using a 625  $\mu\text{m}$ -thick, high resistivity ( $> 5 \text{ kohm}\cdot\text{cm}$ ) n-type and double-sided polished 6-in silicon wafer. In this poster we present electrical characteristics of the fabricated sensors and the drain currents as a function of the drain voltage for different the gate voltages. We also present the optimized design parameters of the prototype sensor to demonstrate the proper functioning of the switch.

### Submission declaration

Original and unpublished

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**Presenter:** PARK, Hwanbae (Kyungpook National University)

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for imaging

Contribution ID: 349

Type: POSTER

## Large Input-Capacitance Compensation Method Employed in a CSA Designed for EMCs in HIEPA

*Saturday, December 14, 2019 2:55 PM (1 minute)*

In this paper, a large input-capacitance compensation method is proposed in order to improve the performance of a CSA designed for electromagnetic calorimeter (EMC) in high intensity electron-positron accelerator (HIEPA), which is one of the options for the new generation of particle physics test facility in China. Charge Sensing Amplifier (CSA) is an important unit which can convert input charges into corresponding voltages. In advanced radiation sensing applications, high-resolution imaging as well as rare particles detection demands for detectors with large volumes or intercept area, which definitely bring large input capacitance to following CSA. When particles incident into the detector, the produced charges are shared between the detector capacitance and the miller equivalent of CSA's feedback capacitance. Generally, in order to achieve better noise performance, the feedback capacitance of the CSA is set to fermi farad, whose miller equivalent may hardly be comparable with the detector capacitance. Therefore, a large amount of signal charges shunt to ground through the detector capacitance and fail reaching the input node of CSA, which result in SNR degradation. Furthermore, the rising time of the CSA's output signal is also retarded as a result of signal loss. A capacitance compensation method is proposed in order to make the voltage of one capacitance plate varies with the that of the other plate, thus the detector (ideally) shows no capacitance to the input of the CSA. A unity-gain amplifier is carefully designed to execute the proposed method, in which, an output small signal current cancel-out technique is applied. Simulation results shows that the gain and bandwidth of the unity-gain amplifier are 0.019dB and 31MHz, respectively. The SNR of the CSA output is substantially enhanced by 4 times at the 270pF input-capacitance.

### Submission declaration

Original and unpublished

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**Presenter:** Prof. WANG, Jia (Northwestern Polytechnical University)

**Session Classification:** POSTER

**Track Classification:** ASICs

Contribution ID: 350

Type: POSTER

## Screening and calibration of XRISM/Xtend flight model CCD

*Saturday, December 14, 2019 3:18 PM (1 minute)*

X-ray Imaging and Spectroscopy Mission (XRISM) will be launched in early 2022. XRISM has a soft X-ray imaging telescope using X-ray mirror and CCD cameras, named “Xtend”. In 2019, we have performed screenings to choose four flight-model (FM) CCD chips from twelve FM candidates provided by Hamamatsu Photonics company. After that, we performed on-ground calibration for the selected FM CCD chips. In this presentation, we report results of the screenings and calibrations.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Applications in astrophysics

Contribution ID: 353

Type: ORAL

## An experimental study on the charge transfer inefficiency of X-ray CCDs developed for the XRISM satellite

*Sunday, December 15, 2019 2:20 PM (20 minutes)*

XRISM is the seventh Japanese X-ray astronomical satellite planned to be launched in early 2020's, and carries an X-ray charge-coupled device (CCD) camera as one of the two focal plane detectors. The camera has four P-channel back-illuminated CCDs with an imaging area size of 31 mm × 31 mm arranged in a 2×2 array. The charge transfer inefficiency (CTI) is defined as a fraction of charge loss per one pixel transfer, which is caused by the trap of signal charge with defects in the channel, and the modeling of the CTI is the key of the CCD calibration especially for such a large-format CCD. The CTI depends on several operational/observational parameters: transfer rate, pixel size, X-ray photon energy, X-ray event grade, X-ray photon flux, CCD temperature, and so on. We here present an experimental study on the CTI dependencies on these parameters. X-ray CCD data frames are obtained with different clocking modes, different incident X-ray energy, different X-ray photon flux, and different CCD temperatures. Analyzing this data set allows us to disentangle the degeneracy of the CTI dependencies and build a more reliable CTI correction model. X-ray spectra before and after applying the CTI correction utilizing these results are also shown.

### Submission declaration

Original and unpublished

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**Presenter:** KANEMARU, Yoshiaki (University of Miyazaki)



**Session Classification:** Session3

**Track Classification:** Applications in astrophysics

Contribution ID: 354

Type: POSTER

## Soft X-ray Trigger Performance of X-ray Astronomy SOI Pixel Sensors, "XRPIX"

*Saturday, December 14, 2019 2:13 PM (1 minute)*

We have been developing X-ray Silicon-On-Insulator (SOI) pixel sensors, called "XRPIX" for the next generation X-ray astronomy satellite "FORCE" (Tsuru et al. 2018, Proc. of SPIE 10709, 107090H). XRPIX has the event trigger output function which achieves a time resolution of 10  $\mu$ s. This time resolution is higher by an order of five than that of X-ray CCDs, used as the main detectors in the current X-ray astronomy satellites. In this presentation, we report results on the evaluation of the trigger function. (1) We show the linearity between the X-ray energy and the threshold voltage of the trigger circuit using monochromatic X-rays such as Fe-K $\alpha$  (6.4 keV), Al-K $\alpha$  (1.5 keV), and F-K $\alpha$  (0.68 keV). Although overall linearity is good enough, there is an offset equivalent to 1.4 keV. (2) We report the lower X-ray energy threshold. It is determined by the circuit noises of the charge sensitive amplifier and the comparator for the trigger output function. The noise of the comparator circuit is equivalent to 70  $\sim$  80 e (rms), which is significantly higher than that of the charge sensitive amplifier of  $\sim$  10 e (rms). The lower threshold X-ray energy that can be detected with the trigger output function is 1.5 keV, which is determined by the lowest threshold voltage at which the comparator circuit noise is not triggered. The target lower threshold is 1.0 keV, so further noise reduction is necessary. (3) In addition, we report the spectral performance for low energy X-rays such as energy resolution and the tail structure in the spectrum.

### Submission declaration

Original and unpublished

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**Presenter:** Mr KODAMA, Ryota (Kyoto University)

**Session Classification:** POSTER

**Track Classification:** Pixel sensors for imaging

Contribution ID: 355

Type: POSTER

## Improvement and Evaluation of the Event-driven SOI Pixel Detector with Pattern Processing Circuit for X-ray Astronomy

*Saturday, December 14, 2019 2:14 PM (1 minute)*

Future X-ray astronomical satellite missions will require a new type of detector that offers a lower non-X-ray background (NXB) rate. To realize this, we have been developing a series of monolithic active pixel detectors, named “XRPIX,” based on silicon-on-insulator (SOI) complementary metal-oxide-semiconductor technology. The XRPIX series offers higher coincidence time resolution ( $< 10 \mu\text{s}$ ) and wider energy range (1–40 keV) compared to the currently used charge-coupled devices. The XRPIX includes a comparator circuit within each pixel, and can output information of the hit trigger (timing) and the two-dimensional hit pattern (position). Therefore, it is possible to read only the fired pixels, driven by the event. The X-ray readout method using this function is called event-driven mode. This is a key technique in realizing an effective anti-coincidence system. In a previously reported study, we improved the spectroscopic performance by introducing a pinned depleted diode (PDD) structure (Harada et al. 2018, NIMA). The readout noise was measured to be  $\sim 10 e^-$  (rms). The energy resolution was  $\sim 240 \text{ eV}$  (FWHM) in the frame-readout mode at 6.4 keV. However, in this device, an unexpected current path from under the peripheral circuit to the pixel sensing node was observed. We designed a new prototype that improved the structure under the peripheral circuit. In this presentation, we report the recent status and evaluation results of the developed detector with PDD structure.

### Submission declaration

Original and unpublished

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Contribution ID: 357

Type: POSTER

## Low Gain Avalanche Detectors for Precision Timing in the CMS Endcap

*Saturday, December 14, 2019 3:28 PM (1 minute)*

The MIP Timing Detector (MTD) of the Compact Muon Solenoid (CMS) is designed to provide precision timing information (with resolution of ~40 ps per layer) for charged particles, with hermetic coverage up to a pseudo-rapidity of  $|\eta|=3$ . This upgrade will reduce the effects of pile-up expected under the High Luminosity LHC running conditions and brings new and unique capabilities to the CMS detector. The time information assigned to each track will enable the use of 4D reconstruction algorithms and will further discriminate in the time domain interaction vertices within the same bunch crossing to recover the track purity of vertices in current LHC conditions. The endcap region of the MTD, called the Endcap Timing Layer (ETL) will be instrumented with silicon-based low gain avalanche detectors (LGADs), covering the high radiation pseudo-rapidity region between  $|\eta|=1.6$  and 3.0. Each endcap will be instrumented with a two-disk system of LGADs, read out by Endcap Timing Readout Chips (ETROCs), being designed for precision timing measurements. We present the status of the R&D and progress towards the MTD ETL and report on recent test beam results.

### Submission declaration

Redundant (overlaps with already published)

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**Presenter:** HELLER, Ryan (Fermi National Accelerator Lab. (US))

**Session Classification:** POSTER

**Track Classification:** New ideas and future applications

Contribution ID: 358

Type: POSTER

## Improvement in Breakdown Voltage and radiation hardness of doping less charge plasma Silicon Microstrip Detectors studied using TCAD simulator

*Saturday, December 14, 2019 2:39 PM (1 minute)*

We have introduced for the very first time doping less charge plasma technique on Silicon based microstrip detectors. We have performed Synopsys TCAD 2D simulation study of these detectors to determine the breakdown voltage and post radiation effects for next generation microstrip detector for futuristic particle physics experiments. The simulation study of doping less charge plasma on Silicon based microstrip detectors shows the improvement in breakdown voltage by around 66% (2500V for doping less charge plasma silicon detector while 1500V of doped silicon detector) over conventional doped silicon microstrip detector with same configuration/geometry. We also observed decrease in backplane capacitance of plasma based detector by around 83% (0.3Ff/um for doping less charge plasma while 1.87Ff/um for conventional doped detector) over conventional Silicon detector which is good for detection of higher signal and lesser noise. Doping less charge plasma microstrip detector is able to withstand radiation fluence of  $1e15$  neq/cm<sup>2</sup> in terms of breakdown voltage unlike the conventional silicon based microstrip detector having same configuration/geometry. This doping less charge plasma technique is also helpful in thermal budget consideration of these detectors at fabrication level. . This doping less charge plasma technique in detectors may play a crucial role in determination of future particles in high energy physics experiment. We will put up the detail results of our simulation study in full paper.

### Submission declaration

Original and unpublished

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**Session Classification:** POSTER

**Track Classification:** Simulations

Contribution ID: 359

Type: ORAL

## Radiation-Hard Miniature Optical Engine with High Bandwidth

*Wednesday, December 18, 2019 9:00 AM (20 minutes)*

Future silicon trackers will be operated in an intense radiation environment and require large volume of data to be transmitted off detector. In addition, the optical modules must be of low mass in order to limit multiple scattering and nuclear interactions that would degrade the overall performance of the detector. We will present a miniature optical engine that satisfies these constraints. The optical engine consists of two miniature connectors, an electrical connector and a MT ferrule. The “brain” of the optical engine consists of an ASIC driving a VCSEL (Vertical Cavity Surface Emitting Laser) array in an optical package. This intelligent part of the optical engine is relatively small in comparison. The ASIC is designed to operate a 12-channel VCSEL array at 5 Gb/s per channel, which yields a total bandwidth of 60 Gb/s. The ASIC is designed using only core transistors in a 65 nm CMOS process to enhance the radiation-hardness. The ASIC contains a DAC to control the bias and modulation currents of the individual channels in the VCSEL array. Each channel also contains pre-emphasis and equalization circuits so that the ASIC can restore the highly distorted electrical signal after propagating through several meters of small gauge wires (“skinny wires”). The pre-emphasis and equalization are programmable via a DAC. The DAC settings are stored in SEU (single event upset) tolerant registers. The results of the optical engine will be presented at the conference.

### Submission declaration

Original and unpublished

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**Session Classification:** Session11

**Track Classification:** ASICs

Contribution ID: 360

Type: ORAL

## Serial powering for the Phase 2 upgrade of the CMS pixel detector

*Tuesday, December 17, 2019 9:40 AM (20 minutes)*

The Compact Muon Solenoid (CMS) silicon tracker will be replaced at the High Luminosity Large Hadron Collider (HL-LHC) upgrade by a new radiation-hard detector capable of handling higher pileup, higher data rates, and longer trigger latency. RD53A prototype chip in a 65 nm feature size CMOS technology has been developed by RD53 Collaboration to meet these requirements. Meeting the performance specifications requires higher granularity which leads to a higher power consumption. In addition, the smaller feature size leads to lower operating voltage, thus further increasing the current. This cannot be satisfied with the current parallel powering scheme, without significantly increasing the cable mass. Therefore a serial powering scheme will be used. A chain of modules will be powered by a constant current while the necessary internal rails will be provided by the special on-chip voltage regulators called Shunt Low Drop-Out (SLDO) regulators. The SLDO regulator also ensures that the chip sinks a constant input current independent of the internal circuit consumption. In addition, this scheme is less susceptible to voltage transients and noise, while improving the powering efficiency. Four chips on each module are powered in parallel to prevent a single failure from compromising the chain. Optimisation of this mixed scheme will be discussed light of the different failure modes. The first four-chip RD53A modules have been built to test the powering scheme in a realistic system. I will present the challenges of the module design and assembly. Furthermore, the performance of the individually powered modules will be compared to the serially powered chain.

### Submission declaration

Redundant (overlaps with already published)

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**Session Classification:** Session7

**Track Classification:** Pixel sensors for tracking



Contribution ID: 361

Type: ORAL

## Radiation Damage Effects on Double-SOI Pixel Sensors for X-ray Astronomy

*Sunday, December 15, 2019 5:20 PM (20 minutes)*

We have been developing the X-ray SOI (Silicon-On-Insulator) pixel sensor named XRPIX for the future astronomical satellite FORCE. XRPIX is a monolithic active pixel sensor composed of high-resistivity Si sensor, thin SiO<sub>2</sub> insulator and CMOS pixel circuits by utilizing the SOI technology. Since XRPIX is capable of event-driven readout, it can achieve a high timing resolution better than ~10 μs, which enables a low background observation by adopting the anti-coincidence technique. XRPIX onboard the FORCE satellite will be put into the low earth orbit, and will suffer from the radiation effects mainly due to the geomagnetically trapped cosmic-ray protons. From the previous studies of the radiation effects in the SOI pixel detectors, positive charges trapped in the thin oxide layer have a large impact on the detector performance. To improve the radiation hardness of the SOI pixel detectors, we introduced a double-SOI structure, where an additional middle Si layer was added in the oxide layer. The negative potential applied on the middle Si layer compensates the radiation effect due to the trapped positive charges. Although the radiation hardness of the double-SOI detectors for application at high energy accelerators was evaluated, radiation effects on the X-ray imaging spectroscopic performances in the double-SOI detectors was not yet evaluated. In order to evaluate the radiation effects of the X-ray double-SOI detectors, we carry out an irradiation experiment with 6 MeV proton beam with a total dose of ~5 krad, corresponding to a few tens of in-orbit operation. This experiment reveals that the radiation hardness is improved in the X-ray double-SOI detectors. The energy resolution in full-width half maximum for 5.9 keV X-ray is increased by 7±2% with 5 krad irradiation. In this presentation, we present results of the proton irradiation experiment of the X-ray double-SOI detectors, and discuss the possible mechanisms of the degradation of the energy resolution.

### Submission declaration

Original and unpublished

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**Presenter:** HAGINO, Kouichi

**Session Classification:** Session4

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 362

Type: ORAL

## Novel Strategies for Fine-Segmented LGADs

*Wednesday, December 18, 2019 3:00 PM (20 minutes)*

Beside LGADs are now considered a promising solution for 4D-tracking thanks to the excellent timing resolution, in some HEP applications the latter should come with a state-of-the-art spatial resolution of the segmented sensors. The currently available LGAD technology typically features large pixels, in the range  $500\ \mu\text{m} - 1\ \text{mm}$ , due to the presence of a gain-loss region between adjacent pixels, typically  $50-100$  micrometers wide, in which the gain is partially or completely suppressed. In this contribution, we will discuss the segmentation issues in standard LGAD technology and we will present new segmentation strategies, developed by FBK and INFN, aimed at producing sensors with small pixels ( $50-200\ \mu\text{m}$ ) and high fill factor.

Resistive AC-coupled detectors (RSD) are an evolution of LGADs where a not-segmented resistive n-well and multiplication layers have been implemented. In this scheme, the segmentation is provided by the metal read-out pads, AC-coupled to the resistive n-well via a thin dielectric layer. In the first batch, sensors with very fine pitch ( $50, 100, \text{ and } 200\ \mu\text{m}$ ) and 100% fill factor have been produced and characterized in terms of gain, timing, and spatial resolution.

The second proposed technology is the so-called Trench-Isolated LGAD (TI-LGAD). In this new design, the standard inter-pixel isolating structures (Junction Termination Edge) has been replaced with a trench, physically etched in the silicon and filled with silicon oxide, which provides electrical isolation between adjacent pixels. Numerical simulations show that this isolation technology is effective in reducing the gain-loss inter-pixel region to less than  $5\ \mu\text{m}$ , an order of magnitude less than in standard LGADs, without affecting the other detector performance. The first produced TI-LGAD samples with  $250\ \mu\text{m}$  pitch have been characterized and the main results demonstrate that the new trench isolation structure: i) provides electrical isolation among pixels; ii) supports high-bias voltage ( $> 300\text{V}$ ) without edge-breakdown; iii) strongly increases the pixel fill-factor paving the way at the developing of LGADs sensors with pitch  $< 100\ \mu\text{m}$ .

### Submission declaration

Original and unpublished

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**Presenter:** PATERNOSTER, Giovanni (Fondazione Bruno Kessler)

**Session Classification:** Session13

**Track Classification:** Technologies

Contribution ID: 363

Type: ORAL

## New beam test results of 3D pixel detectors constructed with poly-crystalline CVD diamond

*Monday, December 16, 2019 9:40 AM (20 minutes)*

Detectors based on Chemical Vapor Deposition (CVD) diamond have been used extensively and successfully in beam conditions/beam loss monitors as the innermost detectors in the highest radiation areas of Large Hadron Collider (LHC) experiments. For future experiments at CERN it is expected that the innermost detectors will accumulate an order of magnitude larger fluence than present experiments. This trend of increasing required radiation tolerance is now common in areas where sources and beams are developed with higher energy or higher intensity to reach new regimes of physics. As a result an enormous effort is ongoing to find detector materials that operate after fluences of  $>10^{16}$  particles/cm<sup>2</sup>.

Diamond is one candidate for such a material primarily due to its large displacement energy which enhances its inherent radiation tolerance. Over the last two years the RD42 collaboration has constructed a series of 3D pixel detectors using CVD diamond as the active material and laser fabricated columns in the bulk and characterized them in test beams. This article presents beam test results of 3D pixel detectors fabricated with poly-crystalline CVD diamonds. The cells of the devices had a size of 50  $\mu\text{m}$  x 50  $\mu\text{m}$  with columns 2.6  $\mu\text{m}$  in diameter. The cells were ganged in a 1 x 5 and 3 x 2 pattern to match the layouts of the pixel read-out electronics currently used in the ATLAS and CMS experiments at the Large Hadron Collider, respectively. In beam tests, using tracks reconstructed with a high precision tracking telescope, a tracking efficiency of 99.3% was achieved. The efficiency of both devices plateaus at a bias voltage of 30V. In addition to the test beam results, the effects on charge collection in poly-crystalline CVD 3D diamond pixel devices due to radiation will be discussed leading to methods for achieving a device capable of operating at  $10^{17}$  particles/cm<sup>2</sup>.

### Submission declaration

Original and unpublished

**Primary authors:** KAGAN, Harris (O); TRISCHUK, William (University of Toronto (CA))

**Presenter:** KAGAN, Harris (O)

**Session Classification:** Session5

**Track Classification:** Pixel sensors for tracking

Contribution ID: 364

Type: ORAL

## Latest Results on the Radiation Tolerance of Diamond Pixel and Pad Detectors

*Tuesday, December 17, 2019 4:40 PM (20 minutes)*

As nuclear and high energy facilities around the world are upgraded and move to higher and higher intensities, the detectors in use at these facilities must become more radiation tolerant. Diamond is a material in use at many facilities due to its inherent radiation tolerance and ease of use. In this talk, we will present the results of recent radiation tolerance measurements of the highest quality poly-crystalline Chemical Vapor Deposition (pCVD) diamond material for a range of proton energies, pions and neutrons up to a fluence of  $2 \times 10^{16}$  particles/cm<sup>2</sup>. From this data we are able to derive the damage constants as a function of energy and particle species and compare with theoretical models. We will also present the recent measurements of the rate dependence of pulse height for non-irradiated and irradiated pCVD diamond pad and pixel detectors. The results we will present include detectors tested over a range of particle fluxes up to 20 MHz/cm<sup>2</sup> with both pad and pixel readout electronics. Our results indicate the pulse height of unirradiated poly-crystalline CVD diamond detectors and the neutron irradiated poly-crystalline CVD diamond detectors measured with the pad readout show no dependence on the particle flux.

### Submission declaration

Redundant (overlaps with already published)

**Primary authors:** TRISCHUK, William (University of Toronto (CA)); KAGAN, Harris (O); KRAMBERGER, Gregor (Jozef Stefan Institute (SI))

**Presenter:** KRAMBERGER, Gregor (Jozef Stefan Institute (SI))

**Session Classification:** Session10

**Track Classification:** Radiation damage and radiation tolerant materials

Contribution ID: 366

Type: POSTER

## Development of gamma-ray detector consisting of 1 mm pixelated halide scintillator arrays and MPPC arrays

*Saturday, December 14, 2019 2:03 PM (1 minute)*

Scintillator and scintillator array detectors have been applied as gamma-ray imaging sensors in many fields, including high-energy physics, medical imaging, astrophysics, and homeland security. One of the most recent trends in gamma-ray imaging is the Compton camera. The Compton camera is based on active-matrix pixels composed of either (1) semiconductor detectors or (2) scintillators. Although the scintillator is advantageous for use in practical commercial systems because of its cost effectiveness, there is still room for improvement in the scintillation performance in terms of the energy resolution, light yield, and decay time.

Because of their excellent energy resolution and high light yield, increasing focus has been placed on halide scintillator crystals over the last decade. The SrI<sub>2</sub>:Eu scintillator is one of the most promising candidates for use in gamma-ray imaging detectors such as Compton cameras because of its high energy resolution and fast decay time [1]. In a previous study, we reported the development of 3×3×3 mm<sup>3</sup>/pixel 8×8 matrix SrI<sub>2</sub>:Eu halide scintillator arrays and obtained average energy resolution of 6.7% (FWHM) for 662 keV gamma-rays [2]. However, the assembly of 1.0 mm or smaller pixels in the halide scintillator matrix is both technically challenging and time consuming because these pixels are highly hygroscopic and are difficult to process.

In this study, we develop a radiation detector with 1.0 mm pixel-sized SrI<sub>2</sub>:Eu arrays using a dicing technique that is cost-effective, widely applicable, and provides good energy resolution. In this conference, we will present the energy and position performance of developed SrI<sub>2</sub>:Eu arrays coupled with MPPC arrays. The study of depth-of-interaction (DOI) capability of these arrays will also be shown.

### REFERENCES

- [1] A. Yoshikawa et al., "Growth of 2Inch Eu-doped SrI<sub>2</sub> single crystals for scintillator applications," *Journal of Crystal Growth*, vol. 452, pp. 73?80, 2016.
- [2] M. Yoshino et al., "Development of Eu:SrI<sub>2</sub> Scintillator Array for Gamma-Ray Imaging Applications," *IEEE Trans Nucl Sci*, vol. 64, no. 7, pp. 1647?1651, 2017.

### Submission declaration

Original and unpublished

**Primary authors:** YOSHINO, Masao (IMR, Tohoku University); KIM, Kyoung Jin (IMR, Tohoku University); KAMADA, Kei (NICHe, Tohoku University; C&A Corporation); KUROSAWA, Shunsuke (NICHe, Tohoku University); YOKOTA, Yuui (NICHe, Tohoku University); YAMAJI, Akihiro (IMR, Tohoku University); SHOJI, Yasuhiro (IMR, Tohoku University; C&A Corporation); OHASHI, Yuji (NICHe, Tohoku University); SATO, Hiroki (NICHe, Tohoku University); FUJIEDA, Kazuya (Waseda University); TANAKA, Ryo (Waseda University); KATAOKA, Jun (Waseda University); YOSHIKAWA, Akira (IMR, Tohoku University; NICHe, Tohoku University; C&A Corporation, Sendai Japan)

**Presenter:** YOSHINO, Masao (IMR, Tohoku University)

**Session Classification:** POSTER

**Track Classification:** Technologies



Contribution ID: **367**

Type: **not specified**

## **Opening of dinner**

*Tuesday, December 17, 2019 7:00 PM (10 minutes)*

**Session Classification:** Symposium dinner

Contribution ID: **368**

Type: **not specified**

## **Special entertainment: "Kagura" dancing**

*Tuesday, December 17, 2019 7:50 PM (20 minutes)*

**Session Classification:** Symposium dinner

Contribution ID: **369**

Type: **not specified**

## **Closing of dinner**

*Tuesday, December 17, 2019 8:50 PM (1 minute)*

**Session Classification:** Symposium dinner

Contribution ID: 370

Type: **not specified**

## **Opening of door of the room**

*Sunday, December 15, 2019 8:30 AM (30 minutes)*

**Session Classification:** Session1

Contribution ID: 371

Type: **ORAL**

## Opening address, Logistics

*Sunday, December 15, 2019 9:00 AM (20 minutes)*

### Submission declaration

Original and unpublished

**Presenters:** UNNO, Yoshinobu (High Energy Accelerator Research Organization (JP)); FUKAZAWA, Yasushi (Hiroshima University)

**Session Classification:** Session1

Contribution ID: 372

Type: **not specified**

## **Opening of door of the room**

*Monday, December 16, 2019 8:30 AM (30 minutes)*

**Session Classification:** Session5

Contribution ID: 373

Type: **not specified**

## **Opening of door of the room**

*Tuesday, December 17, 2019 8:30 AM (30 minutes)*

**Session Classification:** Session7

Contribution ID: 374

Type: **not specified**

## **Symposium photo**

*Monday, December 16, 2019 12:20 PM (20 minutes)*

**Session Classification:** Excursion



Contribution ID: 375

Type: **not specified**

## Excursion to Miyajima island

*Monday, December 16, 2019 12:40 PM (5h 50m)*

Conference center - (busses) - Miyajima-guchi - (ferry) - Miyajima port - (walk) - Itsukushima shrine - (Free time) - Miyajima port - (ferry) Miyajima-guchi - (busses) - Conference Center

**Session Classification:** Excursion

Contribution ID: 376

Type: **not specified**

## **Meeting to the venue**

*Tuesday, December 17, 2019 6:30 PM (30 minutes)*

**Session Classification:** Symposium dinner

Contribution ID: 377

Type: **not specified**

## **Opening of door of the room**

*Wednesday, December 18, 2019 8:30 AM (30 minutes)*

**Session Classification:** Session11

Contribution ID: 378

Type: **not specified**

## **Closing remarks**

**Session Classification:** Session13

Contribution ID: 379

Type: **not specified**

## **Announcement of the next venue (HSTD13 in 2021)**

**Session Classification:** Session13

Contribution ID: **380**

Type: **not specified**

## **Adjourn, wish you safe trip back**

**Session Classification:** Session13

Contribution ID: **381**

Type: **not specified**

## **Closing remarks**

*Wednesday, December 18, 2019 3:20 PM (20 minutes)*

### **Submission declaration**

**Presenter:** UNNO, Yoshinobu (High Energy Accelerator Research Organization (JP))

**Session Classification:** Closing the symposium

Contribution ID: **382**

Type: **not specified**

## **Presentation of the next venue (HSTD13 in 2021)**

*Wednesday, December 18, 2019 3:40 PM (10 minutes)*

**Presenter:** POLEY, Luise (Deutsches Elektronen-Synchrotron (DE))

**Session Classification:** Closing the symposium



Contribution ID: **383**

Type: **not specified**

## **Adjourn, wishing you safe trip back**

*Wednesday, December 18, 2019 3:50 PM (5 minutes)*

**Session Classification:** Closing the symposium