

Machine Protection Workshop May 2019

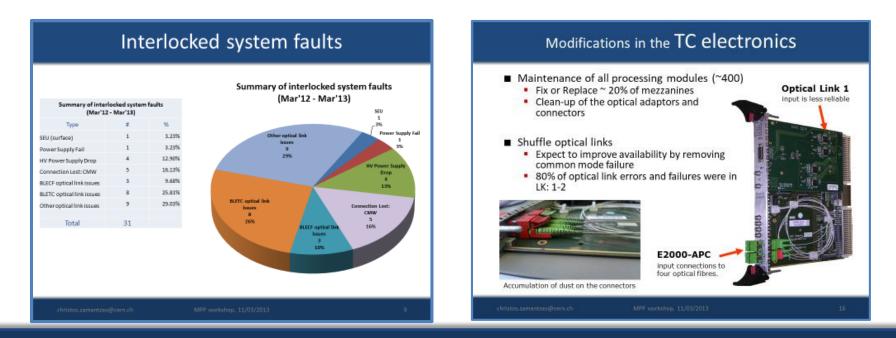
LHC BLM SYSTEM: STATUS AND UPDATES DURING LS2+

Christos Zamantzas on behalf of the BLM team.

Run 1 Availability

During Run 1 a large portion of downtime was attributed to the communication between the acquisition and processing electronics

Several mitigation actions during LS1



Run 2 Availability

During Run 2 the communication issues became manageable

- Less than 5 issues per year
- Additional monitoring and preventive actions during Technical Stops implemented
 - Assignment of a piquet team with daily tasks
 - Better organisation during stops and interventions

Issue	e 2015 2016 2017					2018				
SEU (surface)	2x	1x	4x							
Power Supply Fail			1x	1x	6%	3h37m	19%			
Connection Lost: FESA/VME/CPU	7x	1x	1x					Issues with highest impact duri	st impact during 20	
HV Power Supply Drop								Power Supply failure	(3ł	
HV Power Supply Noise	Зx	2x							•	
Sanity Error: Communication/VME	6х	2x	4x	5x	28%	2h11m	12%	 Tunnel/Surface cards (5x) 	(4ł	
Sanity Error: IC	1x		1x					 Sanity Check (7x) 	(7ł	
Sanity Error: LIC									י רשה	
Sanity Error: SEM	5x	4x	3x	2x	11%	5h28m	29%	Other (5x)	(3h	
BLECF + optical link issues			4x	4x	22%	2h23m	13%			
BLETC + optical link issues	1x	4x		1x	6%	2h10min	11%			
Other optical link issues										
Other	2x	2x		5x	28%	3h6m	16%			
	27x	16x	18x	18x						
	2d15h16m	1d12h36m	1d06h32m			18h54m				

(3h30min)

(4h30min)

(7h45min)

Activities requested to support outside to the LHCBLM modifications

LS2 SUPPORT ACTIVITIES

DISMAC – BLM

In order to allow the intervention on the diodes:

- Disconnect & Remove detectors (with support)
- Protect cables (signal & power)
- Remove or lift cable tray (depends on action)

Temporary storage of all material in plastic boxes below adjacent magnets

This affects 40% of the detectors and all cable-trays from half-cell 8



DISMAC-BLM Schedule Overview

Schedule consists of four main blocks:

- Removal : From Apr. 2019 to Sep. 2019, starting from sector 81
- Re-installation : From Nov. 2019 to Jun. 2020
- System Checkout
 - Follows the completion of a sector.
 - System is re-started and basic validation is done to allow next step
- Irradiation campaign : Should start as early as possible in the plan

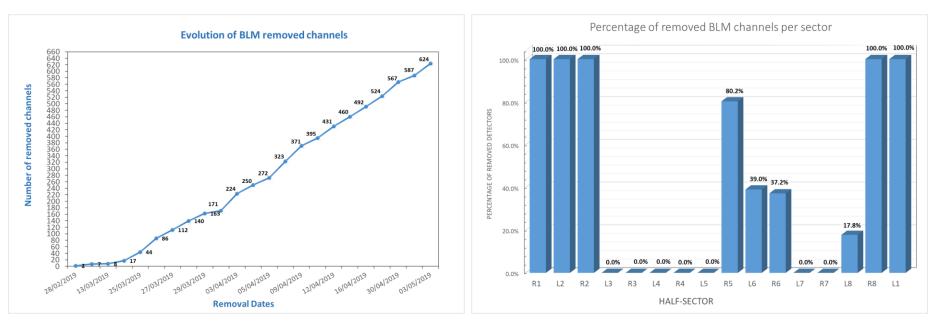
Notes:

- Some locations to be advanced outside the main schedule, e.g. openings for leak localisation and other special interventions.
- Non-Conformity discoveries and IC re-opening will require some locations to be treated twice.

	Year	2019															2020						
	Month	Jan Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	August			
	Week	1 2 3 4 5 6 7 8	9 10 11 12	13 14 15 16 1	7 18 19 20 21	22 23 24 25	26 27 28 29	30 31 32 33 34	35 36 37 38	39 40 41 42	43 44 45 46 47	48 49 50 51	52 1 2 3	4 5 6 7 8	3 9 10 11 12	2 13 14 15 16	6 17 18 19 20 2	21 22 23 24 25	26 27 28 29	30 31 32 33 34 35			
LHC	DISMAC Activities	DISMAC BLM Equipment removal DIS												ISMAC BLM Equipment reinstallation									
LHC	System Checkout														LHC System Checkout and Commissioning								
LHC	Irradiation campaign																Irradiation of	campaign					
LHC	DISMAC 8-1				Open IC					Closing	g IC												
LHC	DISMAC 1-2			Open IC					Closing IC														
LHC	DISMAC 2-3	Follow request	Follow requests for Magnet exchanges, Collimation and	het		Ope	n IC				Clos	sing IC											
	DISMAC 3-4				Open IC					Closing													
LHC	DISMAC 4-5	VSC ta			Open IC					Closing IC													
	DISMAC 5-6	v00 ta	4313		Open IC						Closing IC												
LHC	DISMAC 6-7				Open IC					Closing					losing IC								
LHC	DISMAC 7-8				Open IC						Closir					sing IC							
LHC	CryoBLM 09R7																						
LHC	CryoBLM 09L5																						

DISMAC-BLM Current Status

- In general, activity is on-track and in some cases ahead of schedule
 - Currently at ~45% of removals completed
 - Aim is to complete this first part by July 2019



Listing main actions to be performed or developed in the system

FIRMWARE/SOFTWARE CHANGES

Modification of the BLETC firmware

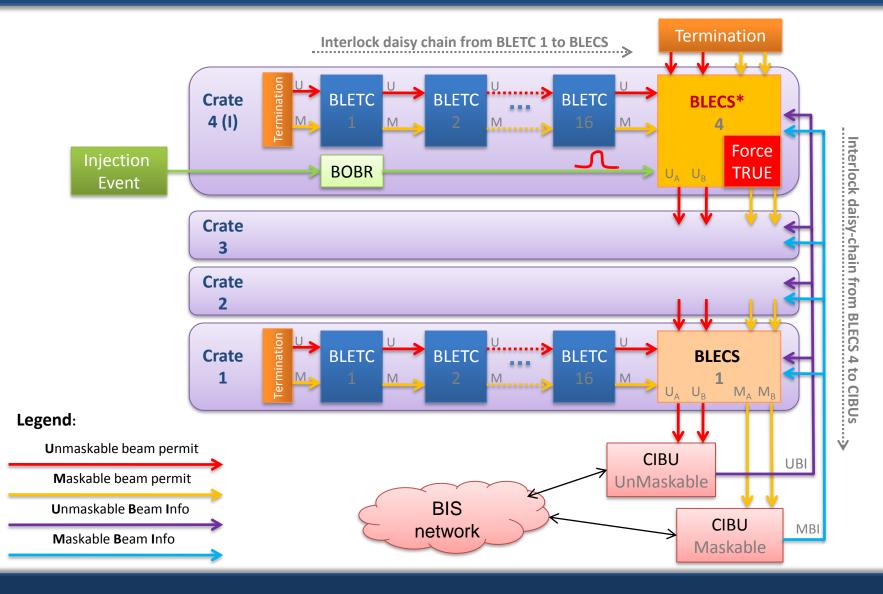
Processing Module firmware modifications:

- Add better compatibility with new CPUs
 - New VMEbus core with MBLT mode
 - New memory map optimized for block transfers
- Restructure of the code to better/newer industry standards
 - Allow the use of common libraries with the other developments
 - Simplify transfer of code to newer electronics

Modification of the BLECS firmware

- Combiner and Survey firmware modifications:
 - Improve regular automatic system checks
 - block increase of input offset
 - add timeout for check completion
 - Improve connectivity check
 - Increase range of values allowed
 - Add compatibility with new CPUs
 - new VMEbus core with MBLT mode
 - new memory map optimized for block transfers
- Full deployment of the "Injection Inhibit" feature
 - Force the Beam Permit line for a fixed period of time when it receives the injection signal and certain other conditions are satisfied.
 - Persistent FESA settings per crate will (in the future can become part of the MCS parameters):
 - Activate/Disactivate the inhibit functionality.
 - Define the time the beam permit is forced to TRUE

Interlock Inhibit Functionality



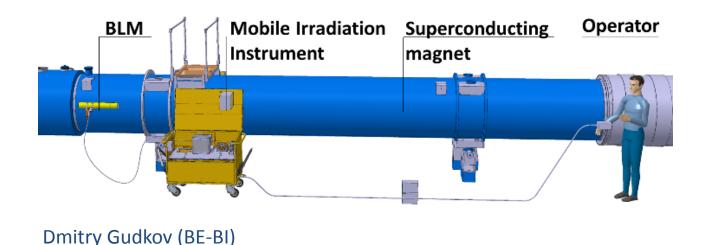
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Modifications of the BLM Software

- Servers to be upgraded to FESA3 and 64bit OS
 - Major re-write of various parts
 - Prototypes have been evaluated during 2018
- Sanity checks code have been taken over by BI-SW team
 - Modifications are done to improve speed and connections to LSA DB
- Automatic daily checks update for NXCALS
 - All logging data in parallel to CALS & NXCALS during 2018
 - History has been transferred
 - Checks to be updated for using only NXCALS
- All diagnostic applications are being reviewed and being consolidated

HARDWARE DEVELOPMENTS

Rad. Source with Trolley



- A complete redesign has been made to the LS1 BL trolley aiming to reduce failures and dose to operators.
- Previous run needed ~ two weeks per sector (+ delays when need to cross doors)
- Complex issues: slow, needs two people for operation, rad. source transportation and daytime storage. Great as a backup plan..
- Will have two completely new trolleys available next year.

Rad. Source with TIM





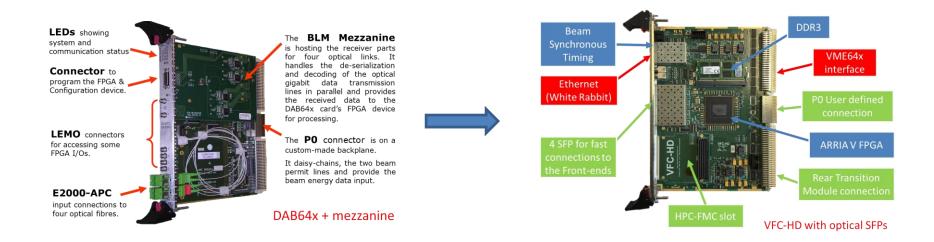
- Work on-going to replace the trolley based solution with the Train Inspection Monorail (TIM)
 - Objective is to build an autonomous system for the complete BLM system validation
 - Train to move from previous BLM + vision recognition + arm placement + arm alignment
 - Supervision system to analyse measurements online and report pass/fail
 - TIM can operate for ~9h, then needs recharge
 - Estimated test time per detector ~ 3 minutes, i.e. < 4 days per sector

Mario Di Castro (EN-SMM)

Processing Module Development

Aim to develop a generic processing board for all BLM installations (and majority of BI systems)

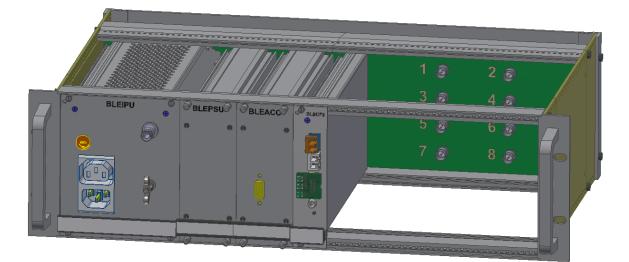
- Currently at 90% of the production (1150 units)
- Extensive testing that includes functional, burn-in and run-in cycles on-going
- Plan to replace the current board in stages:
 - All functionality is being replicated and to be verified on a vertical slice (LS2)
 - Replace (post LS2) the operational units
 - Add new functionalities (LS3)



Acquisition Crate Upgrade

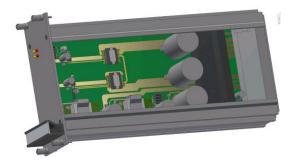
For the future upgrade of BLM acquisition systems in SPS and LHC a new crate is under design

- Height = 3U , Depth = 280mm
- Fully shielded
- No HV or 230V_{AC} inside the chassis
- Maintenance and repair actions from the front side

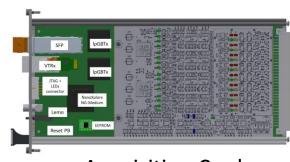




Input Power Unit



Power Supply Unit



Acquisition Card

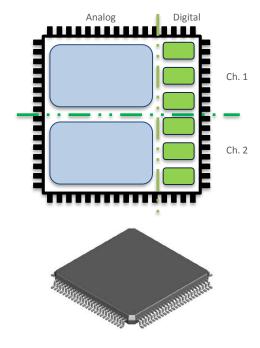
BLM ASIC Development

Two fully functional custom chips are being developed in order to evaluate the performance of two different architectures within a realistic environment:

- CFC asynchronous better suited to handle large currents and quickly varying signals
- Delta-Sigma ideal for high accuracy due to oversampling and filtering
- Technology standard CMOS 130 nm qualified at CERN for 200 Mrad
- Supply voltage 1.2 V (possibly higher for analog)
- Two analog readout channels per chip
- Triplicated digital circuitry with majority voting
- Directly compatible with LpGBT (e-Link)
- Double communication channels for redundancy
- Chip dimensions 4x4 mm
- To be housed in a standard 64 pin Quad Flat Package (10x10 mm)

Project schedule:

- Q1 2018: Technology selection and feasibility
- Q2 Q3 2018: Transistor level design and simulation
- Q4 2018 Q1 2019: Layout design and simulation
- Q2 2019: Submission of two, full size prototypes
- Q4 2019: Testing (evaluation of functionality and radiation tests)
- Q1 2020: Final prototype architecture selection



DETECTOR DEVELOPMENTS

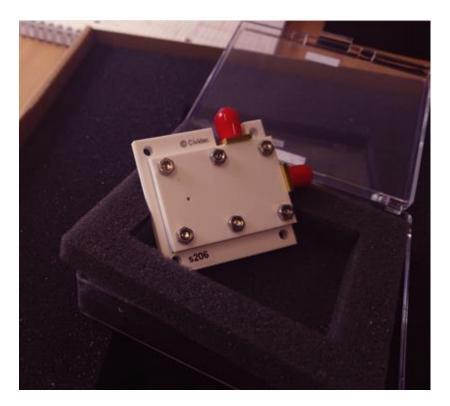
CryoBLM upgrade

New design and production of the detector:

- Cryo dBLM with HV supply, HV filter, charging capacitance
- Readout transmission line 50Ω
- No ground outside
- sCVD diamond sensors
- Ceramics material (Al2O3)



Installation foreseen at QQBI.9L5 and QQBI.9R7



Little Ionisation Chamber

This IC detector with three parallel aluminium electrode plates has reduced geometrical acceptance to extend the dynamic range of the BLM system and is installed at locations where higher losses are expected.

- A new prototype version is being tested at HRM with better ceramics
- Delivery of full production, if agreed, would be before LS3

Proposal to deploy & replace SEMs in more locations using ver.1 LICs during LS2

- Allow time to eliminate those with bad performance
- Provide data to evaluate if different design would be needed long-term



Proportional Chamber

- This detector should provide 100-1000 times (depending on the applied bias voltage) higher sensitivity to the LHC type IC.
 - the parallel plates are replaced with a single wire and
 - the gas from Nitrogen with a mix of Argon & CO2.
- Not ideal for machine protection (gas leakage or voltage change would modify largely the measurements), it is a drop-in replacement to the standard detectors and should avoid the need of the complex bundle installations such those done in 16L2 and 31L2.



