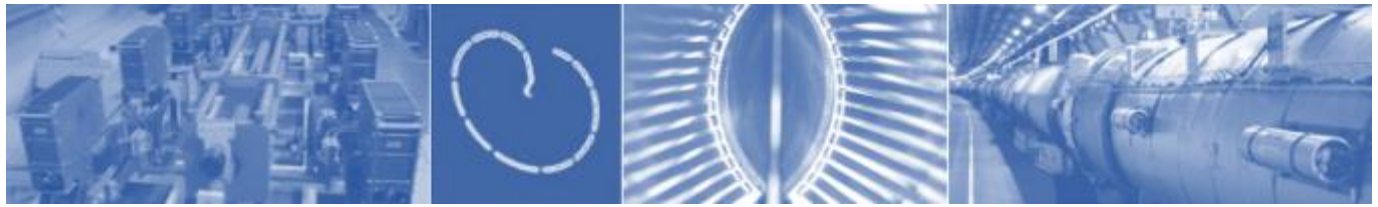
Changes to other BI Systems

T. Levens

on behalf of the Beam Instrumentation group



MPP Workshop 2019

Contents

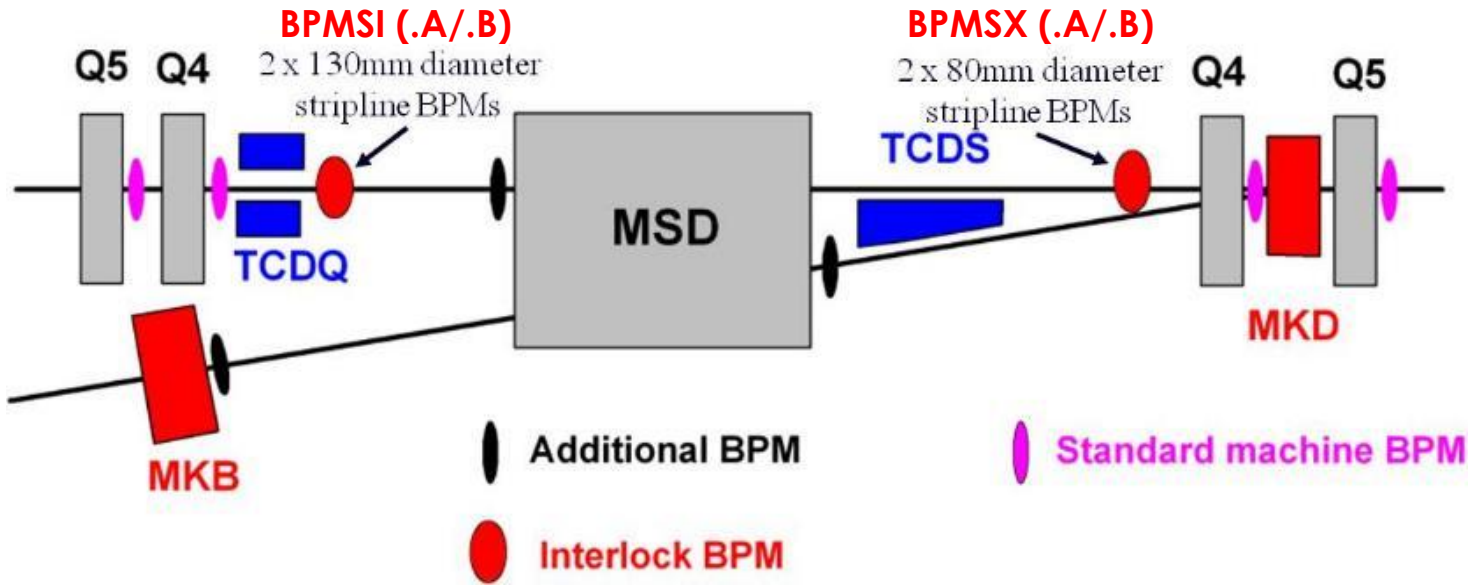
LHC

- Interlock BPMs
- New dI/dt (BCCM)
- DOROS
- BSRA (Abort Gap Monitor)

SPS

- ALPS BPMs
- dI/dt on DC BCT

LHC Interlock BPMs



Two redundant BPMs are used to measure the local orbit around the dump extraction channel

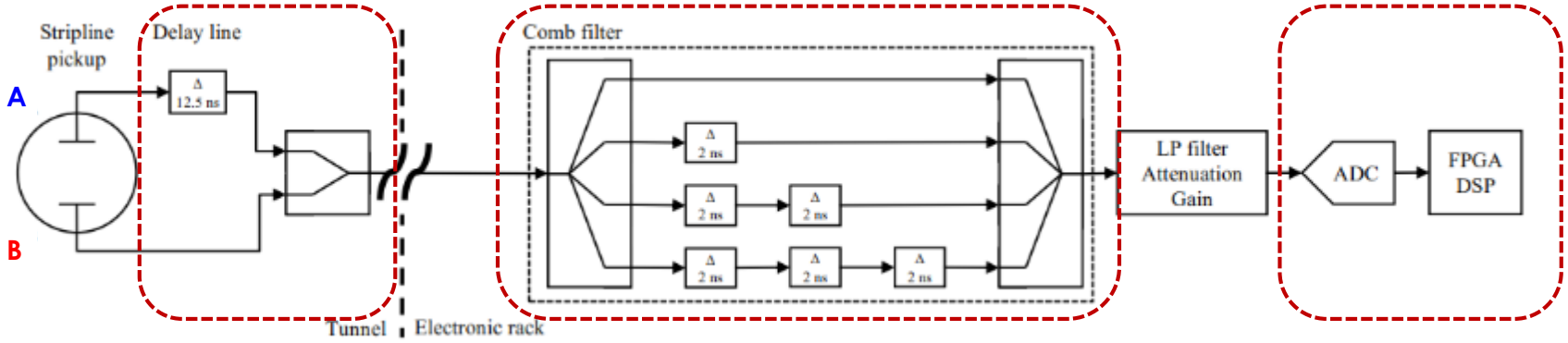
- Abort beam in case of large bunch / beam orbit excursions
- Avoid high losses and/or damage of the septum and the dump line

The system, as it exists today, is based on the standard WBTN BPM read-out electronics

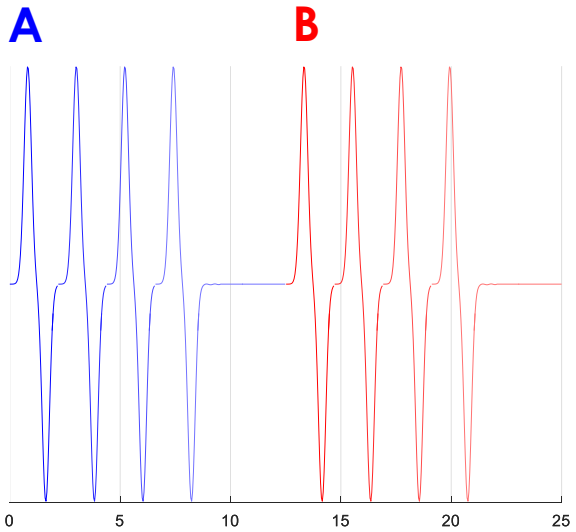
- Terminated strip-lines and absorptive LPF installed during LS1 to reduced signal reflections
- Separate sensitivity setting for interlock and ring BPM
- Bunch-by-bunch, turn-by-turn acquisition
- **Not compatible with doublet bunches → upgrade project launched after LS1**
  - In Run 2, used "fudge" factors on the dump thresholds to artificially cope with doublet bunches

LHC Interlock BPMs – upgrade concept

→ Can take advantage of high speed digitizers that are now available

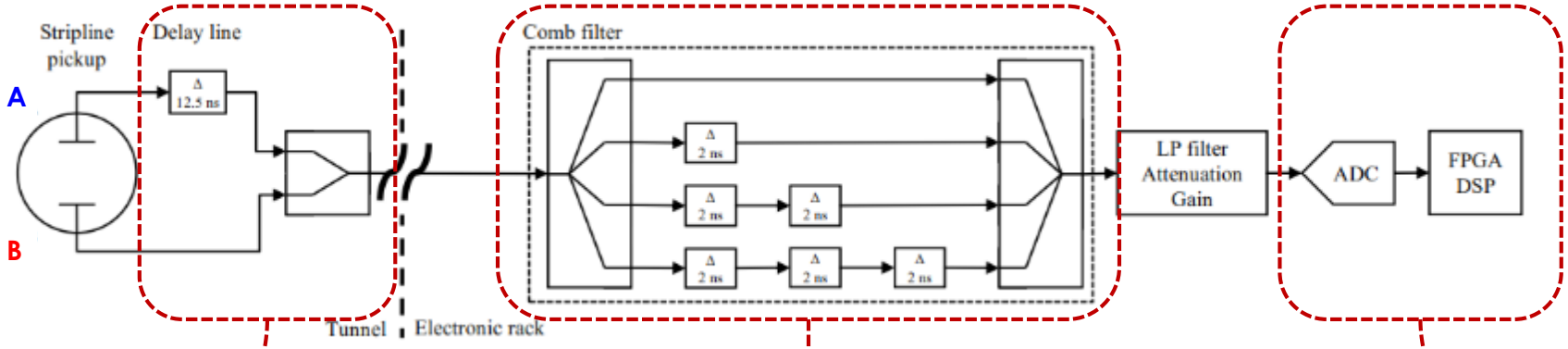


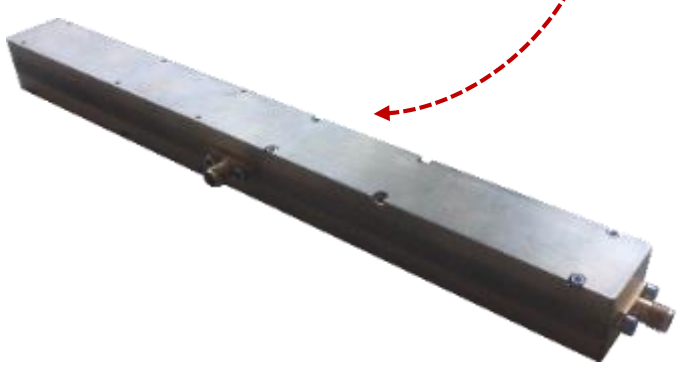
- Time multiplexing of electrode signals
  - Allows a single processing chain for both electrodes
  - Minimises the effect of aging and drift between channels
- Comb-filter
  - Signal extension by replication – more samples for ADC
- Digitization & FPGA processing
  - Calculation of bunch-by-bunch position (& intensity)



LHC Interlock BPMs – developments

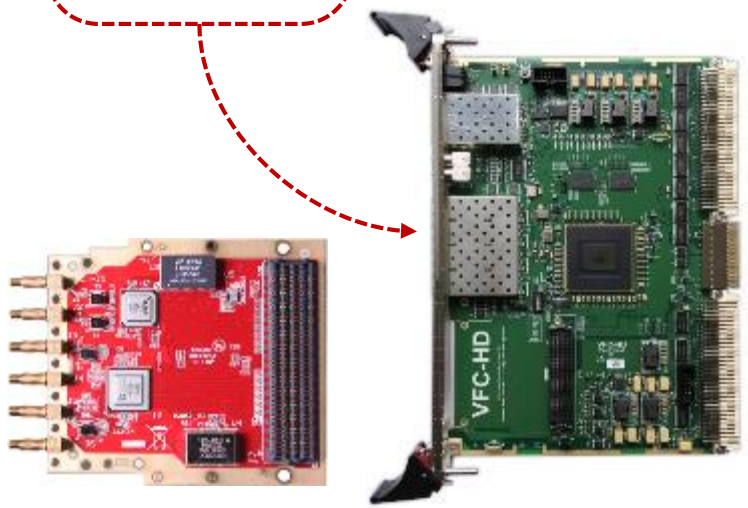
All major systems components developed and tested during Run 2:





Prototype of the (custom) high power combiner

Prototype of the (custom) delay line filter



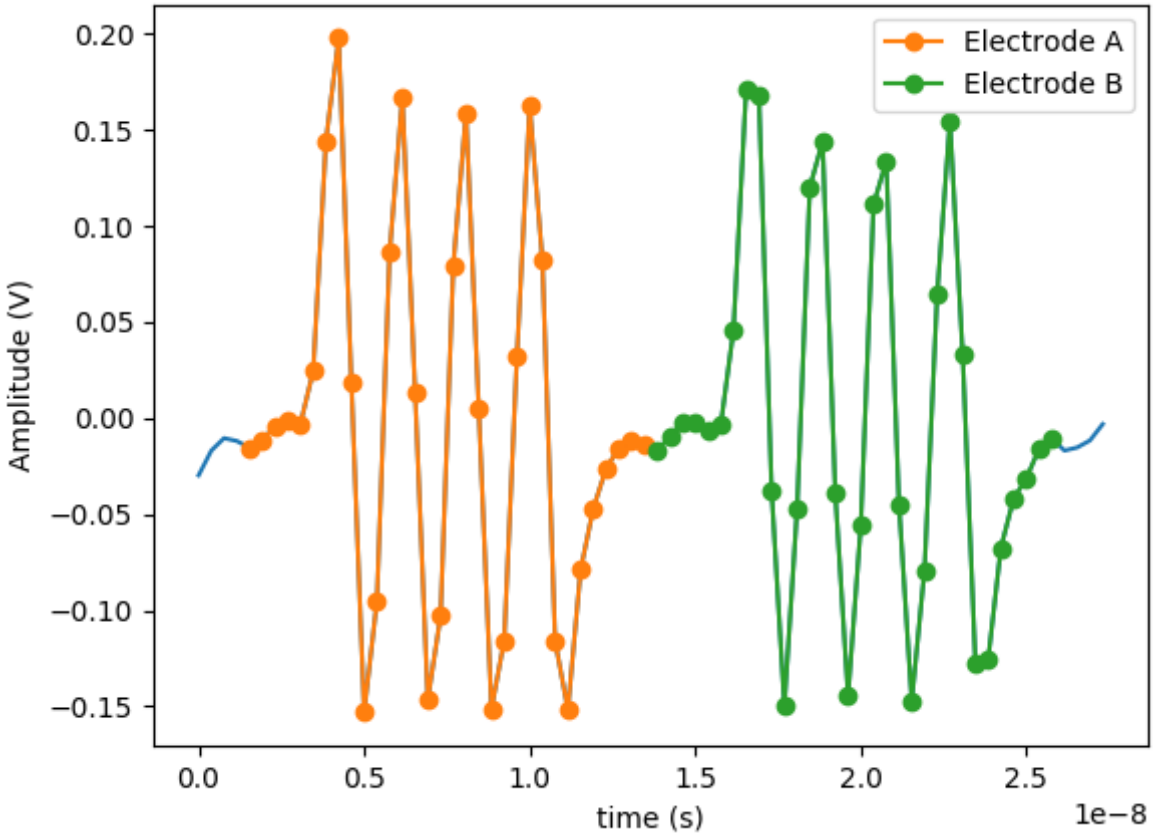
HTG-FMC-14ADC (commercial)
14 bits (9.6 ENOBS) @ 2.6 Gsps
+
BI standard VFC-HD carrier

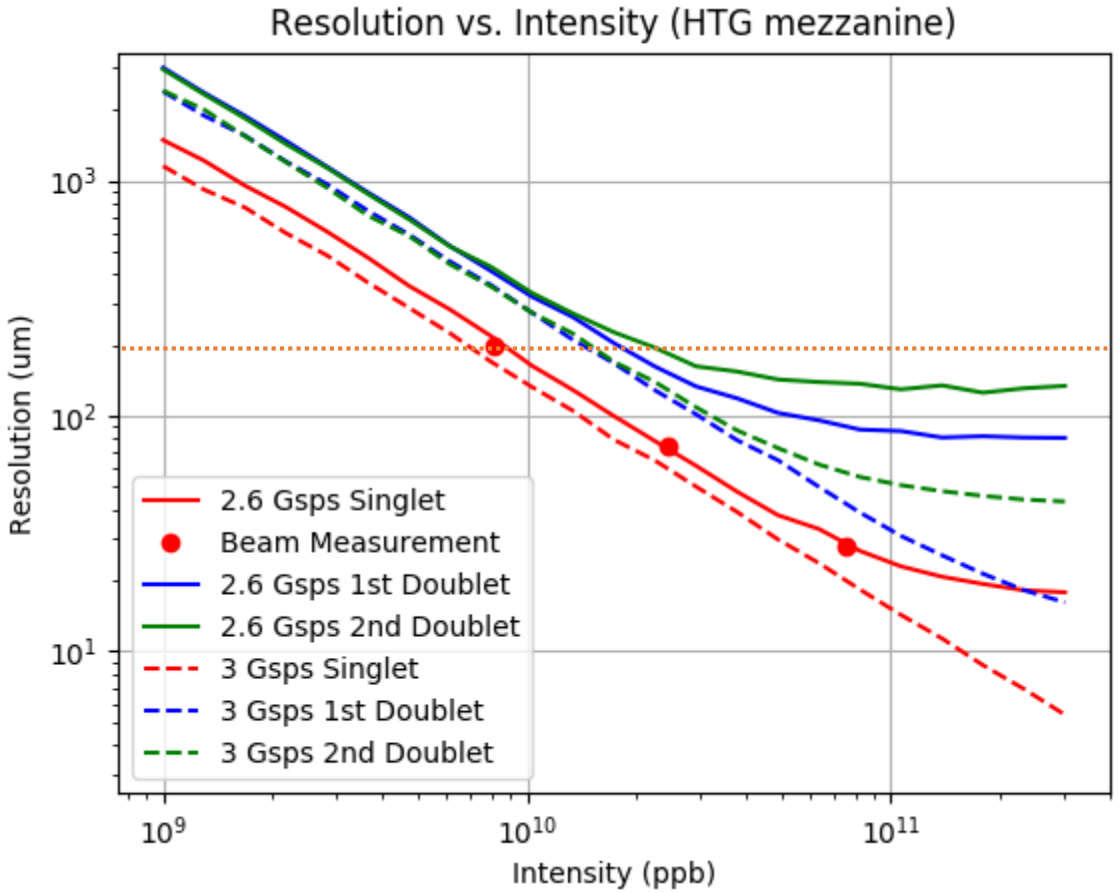
LHC Interlock BPMs – beam measurements

Configuration has been tested with beam the strip-line BPMSY.4L5

Resolution for bunch by bunch, turn by turn, for Intensity **> 1e10**:

- Singlet < **200 µm** (beam data)
- Doublet < **400 µm** (simulation)

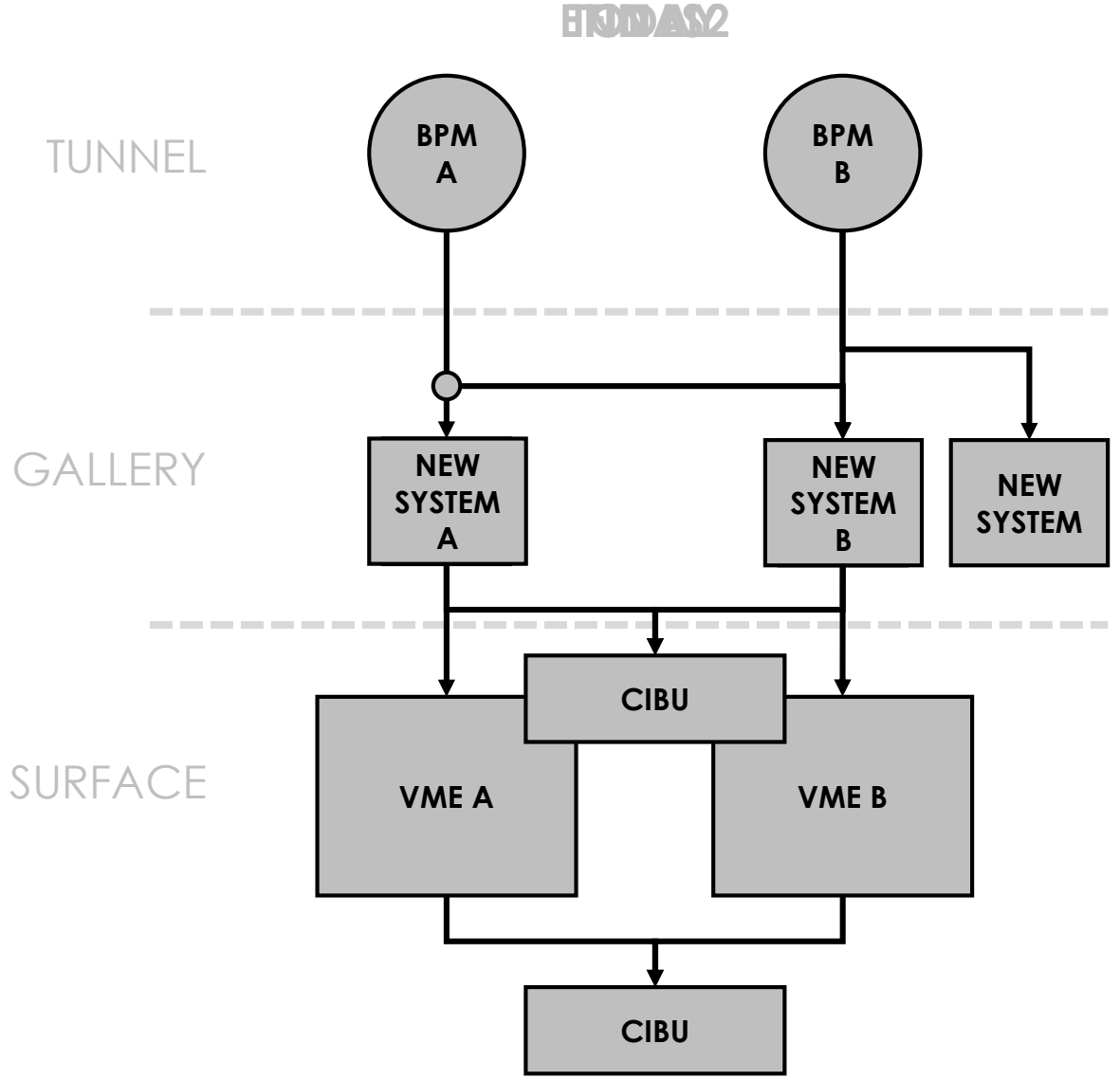




LHC Interlock BPMs – proposal for installation

Validation system to be installed during LS2 on a single BPM

- Propose to use one of the B system BPMs for the new prototype
- The A system BPM signal can be split to drive both WBTN systems
  - Keeps the existing system operational
  - Preserves redundancy to the pickup level (only passive elements shared)
- After system has been validated, a full installation will be made on both A & B systems (16 BPMs total)
  - Will require CIBUs to be moved from SR6 to UA63/UA67
  - New cabling requested
- Validation & commissioning procedure to be discussed further…



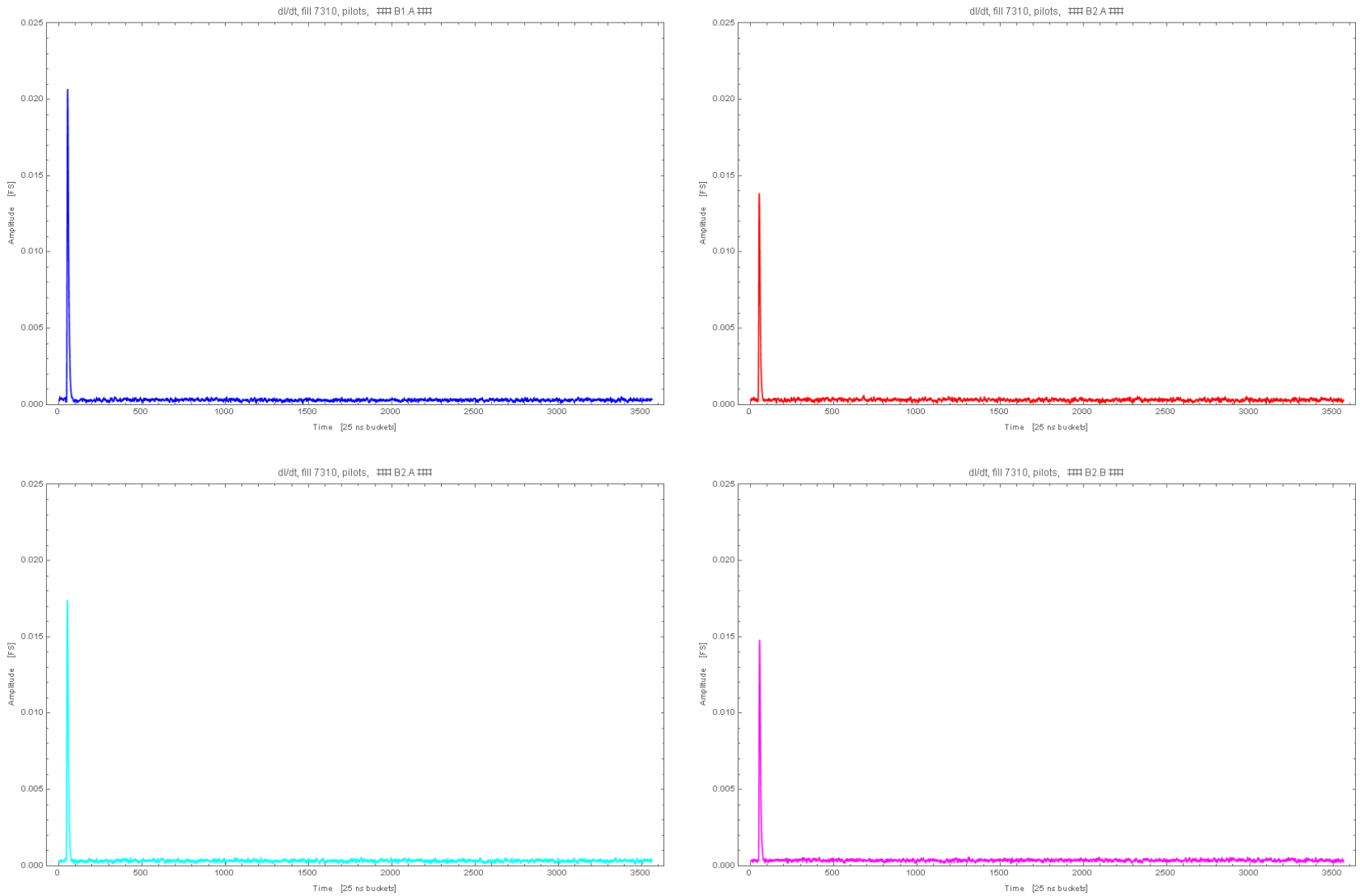
New LHC dI/dt (BCCM)

- Completely new system designed from scratch
  - Beam signal is the sum of four BPM electrode signals
  - RF envelope detection and low pass filtering
  - 16 bit, 40 MHz sampling (beam synchronous)
  - One-turn digital delay line + running subtraction of 40 MHz samples
- During 2018 run prototypes installed and tested with beam in the redundant configuration for both beams
  - Very promising performance, the most challenging spec (one turn sensitivity of 3e11) was achieved with a nice margin
  - Interlock logic was not implemented due to time constraints,
  - But off-line analysis of logged raw data did not show any expected false triggers

BCCM installation in UA47

New LHC dI/dt (BCCM) – measurements

Pilot bunches, raw data:



256 KS ≈ 73 turns:

256 ·1024 / 3564 ≅ 73.5

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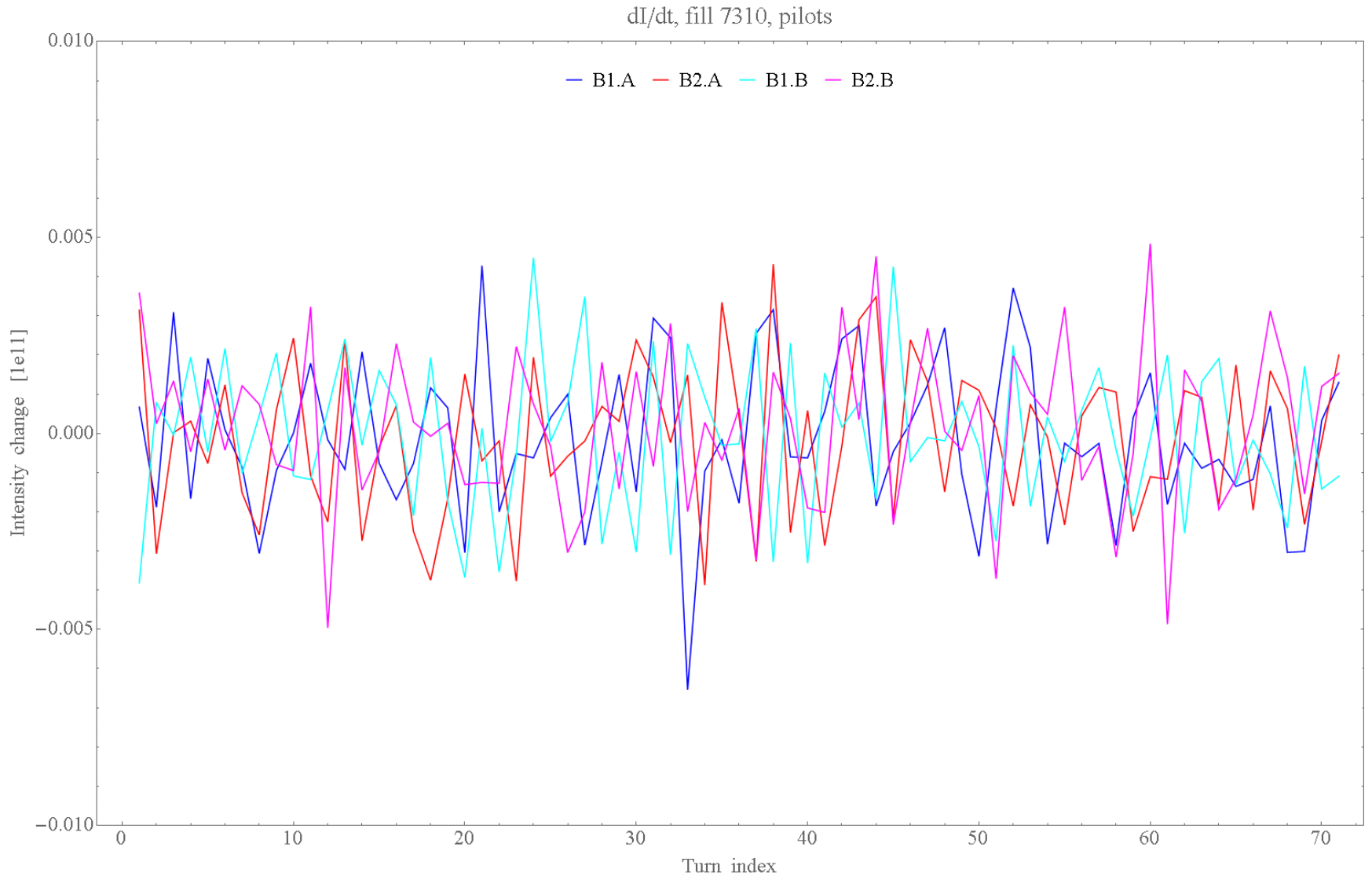
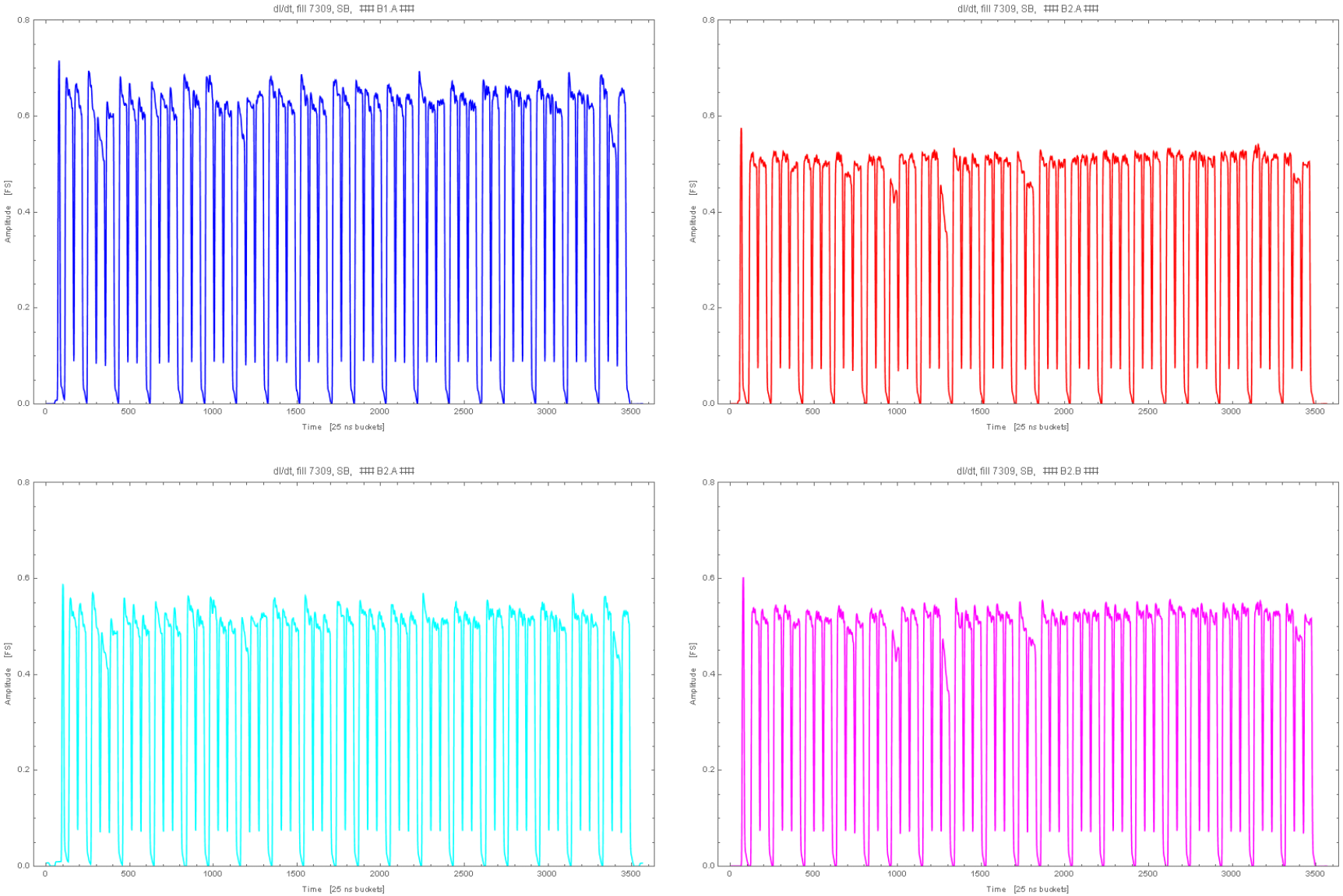


New LHC dI/dt (BCCM) – measurements

First captured stable beams (2556 bunches), raw data:



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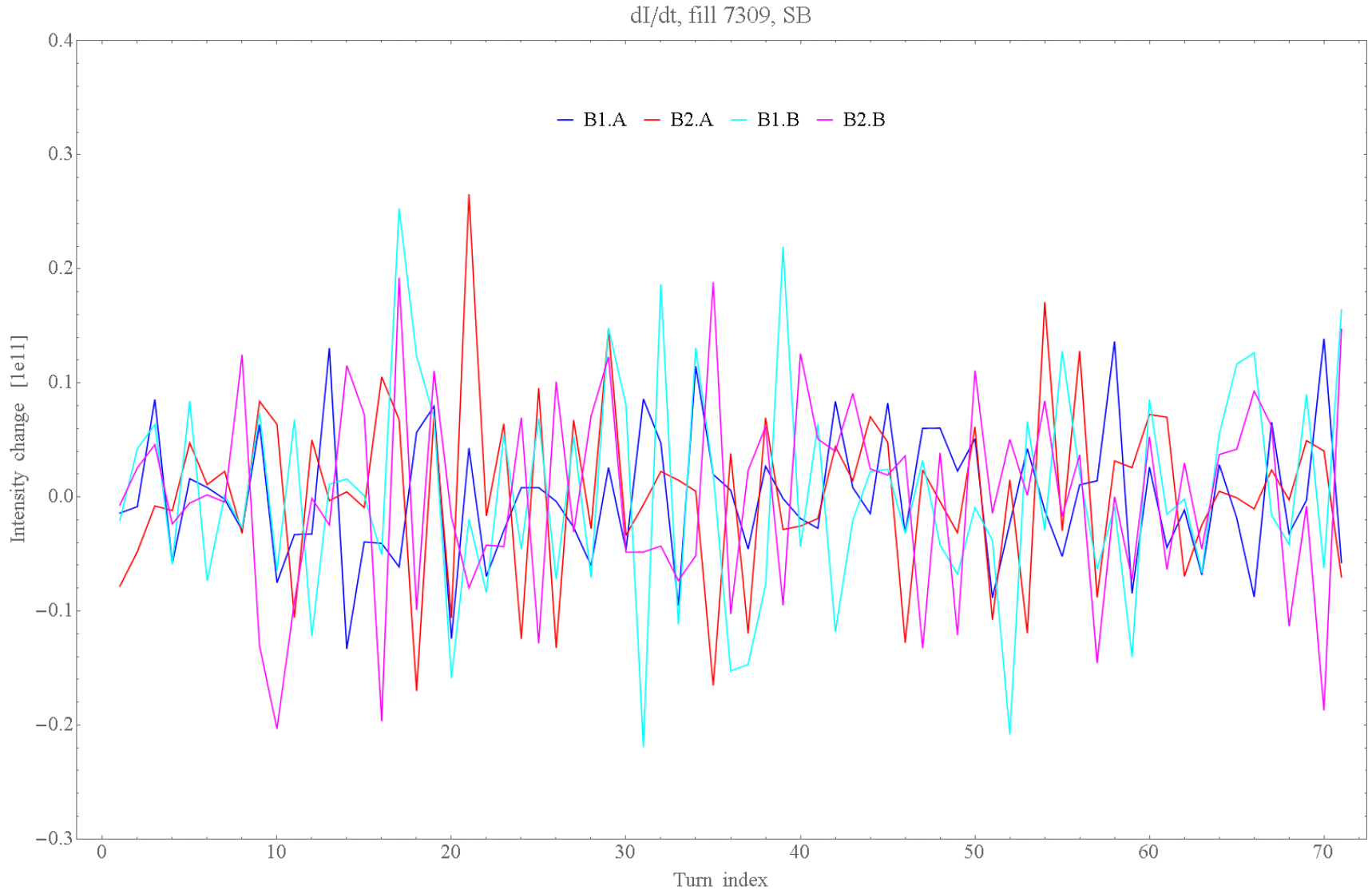
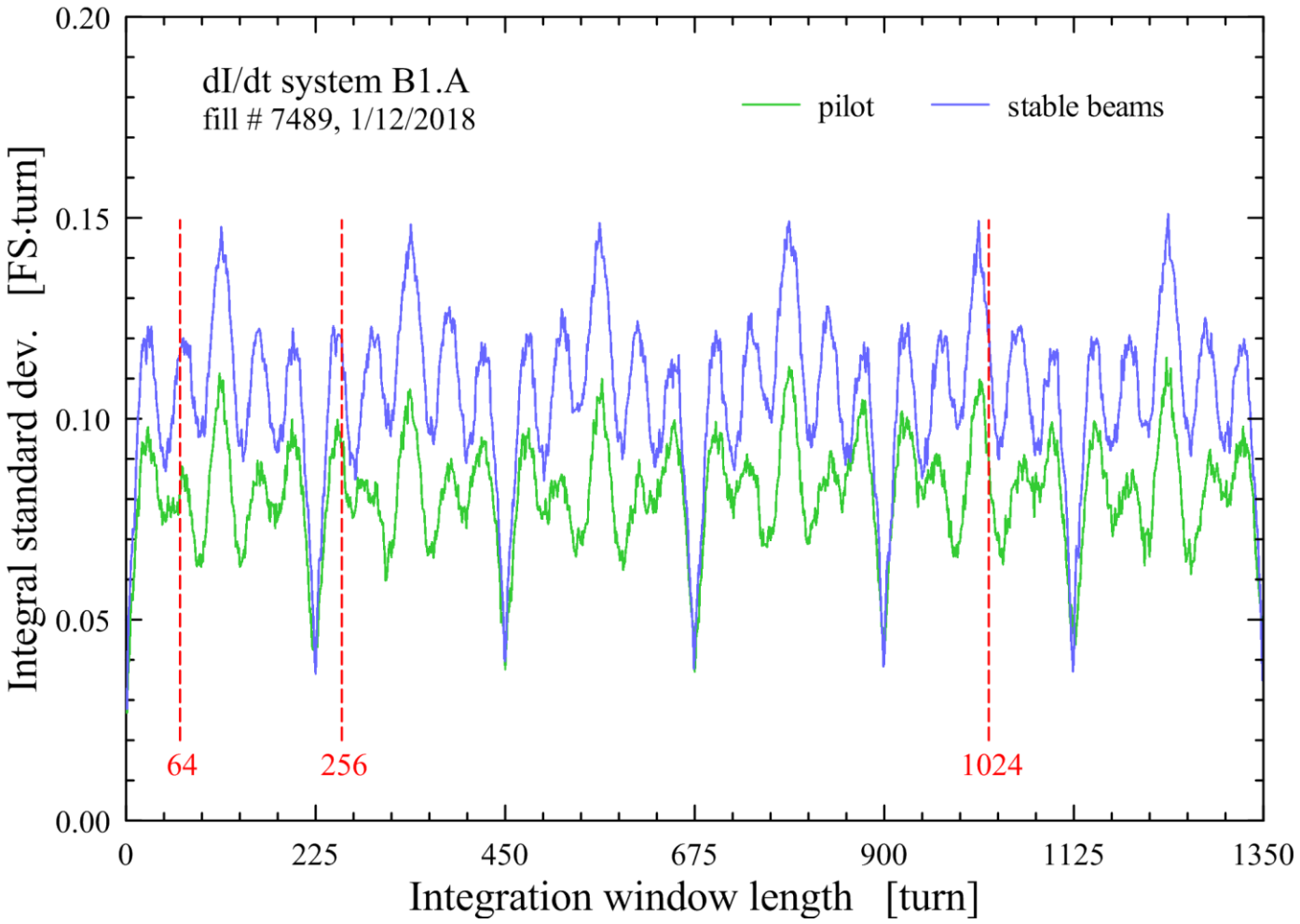


New LHC dI/dt (BCCM) – window length optimisation

- Current integration windows are 1, 4, 16, 64, 256 and 1024 turns
- Analysis of 2018 data shows that the system sensitivity can be improved if the integration time is a multiple of 20 ms (to average out mains interference)
- If windows 256 and 1024 are replaced by 225 and 1125, then the interference sensitivity can be decreased by some 300 %



New LHC dI/dt (BCCM) – plans

- During LS2:
  - Finalisation of the FPGA code to implement full interlock chain
  - Finalisation of the FESA software
  - Optimisation of the hardware installation to improve interference immunity and hardware robustness

- Plan to start up after LS2 in the same state as now
  - i.e. BIS input channels disabled (observation only, no beam-dump)

- When the system has been validated we would request them to be enabled

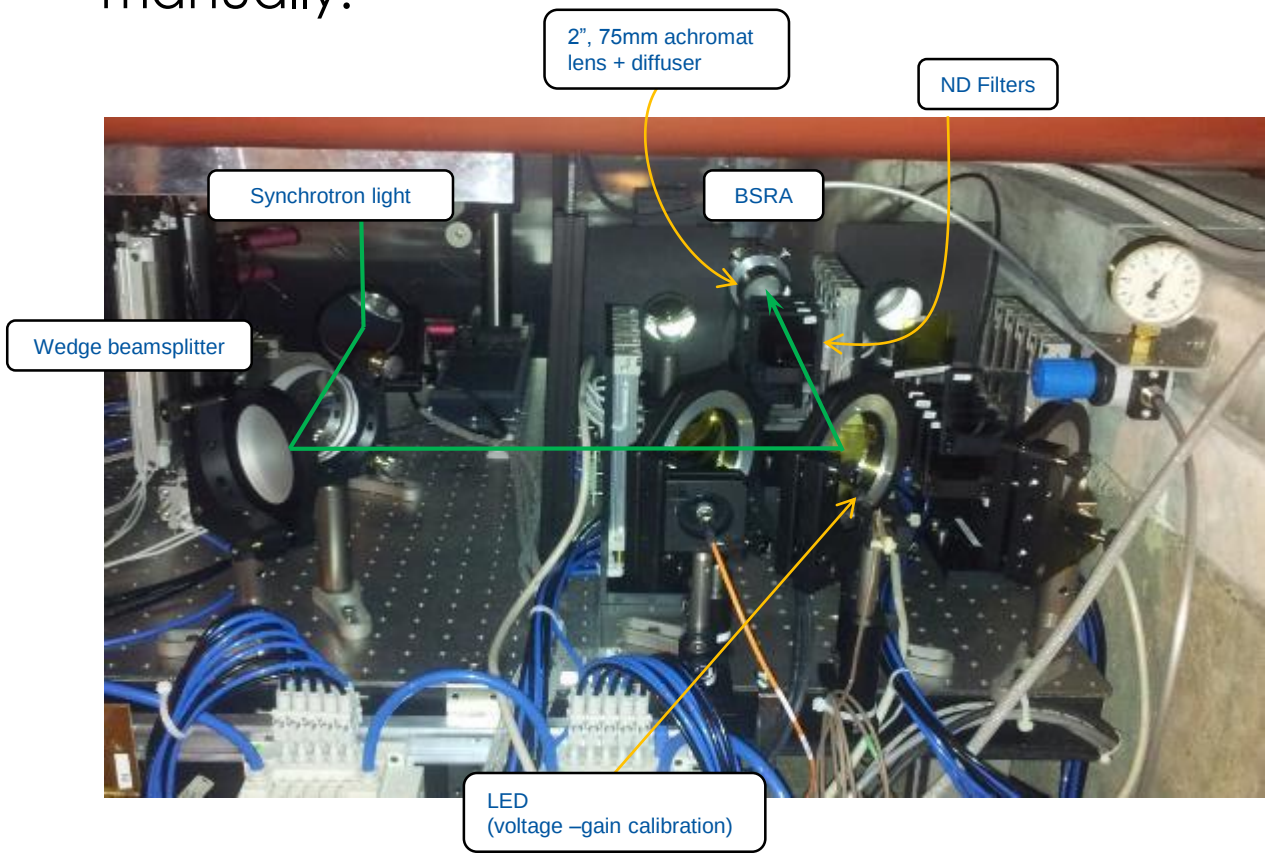
DOROS

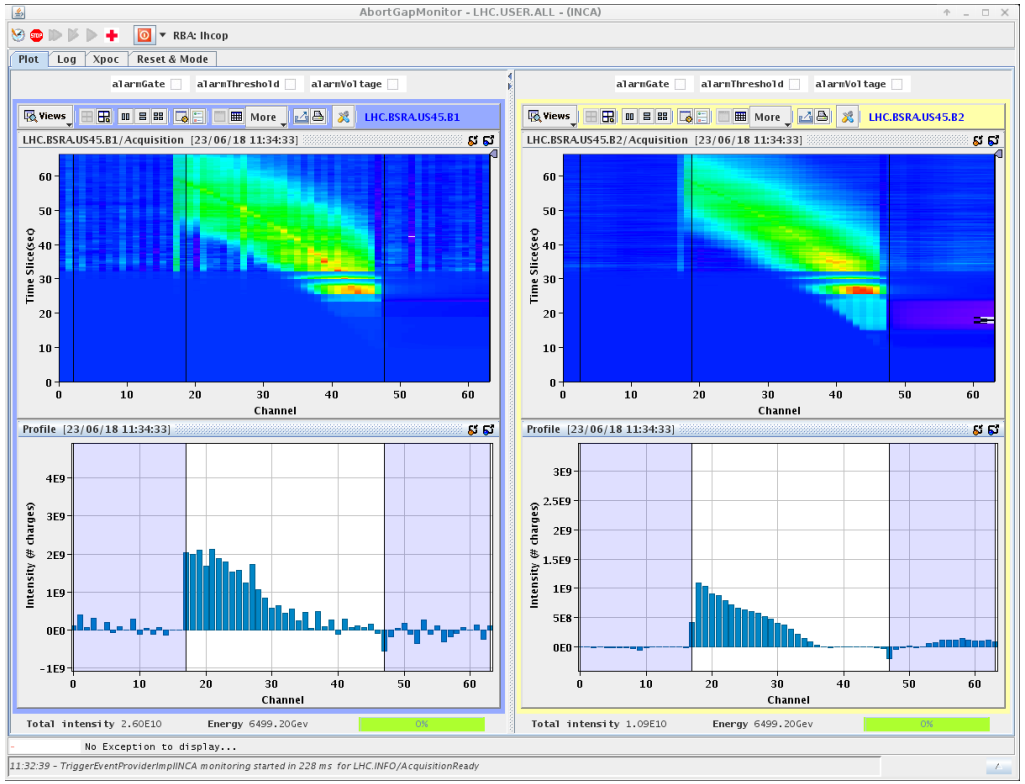
- Software interlocks on beam orbits in collimators with embedded BPMs:
  - 4 TCTs in P1
  - 4 TCTs in P5
  - 2 TCSs in P6
- Operational since TS2 in 2017 with 6 DOROS front-ends.
- Redundant DOROS front-ends added for the 2018 run, since then the system has in total 12 front-ends.
- Very good performance:
  - sub-micron orbit resolution
  - excellent long term stability
  - no single fault
  - no single false dump
  - 100.000000 % availability
- **No change foreseen for run 3…**
  - (So far) no request for additional interlocked channels

SIS DOROS front-ends in US152

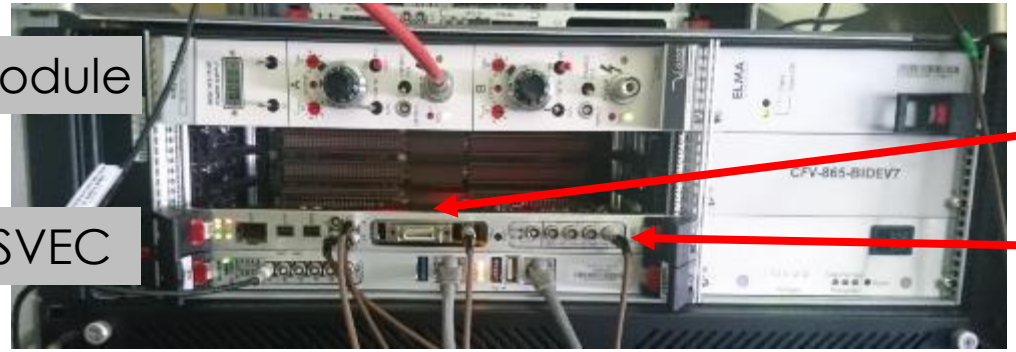
BSRA (Abort Gap Monitor)

- BSRA monitors population (both beams) in the 3 us LHC abort gap.
- Based on detection of SR with gated MCP-PMT.
- BSRA integrated in BSRT system, optical line re-designed in 2015.
- Automatic voltage-gain calibration. Absolute calibration against FBCT performed manually.





BSRA – modifications for LS2



BSRA amplifier and electronics will be upgraded during LS2

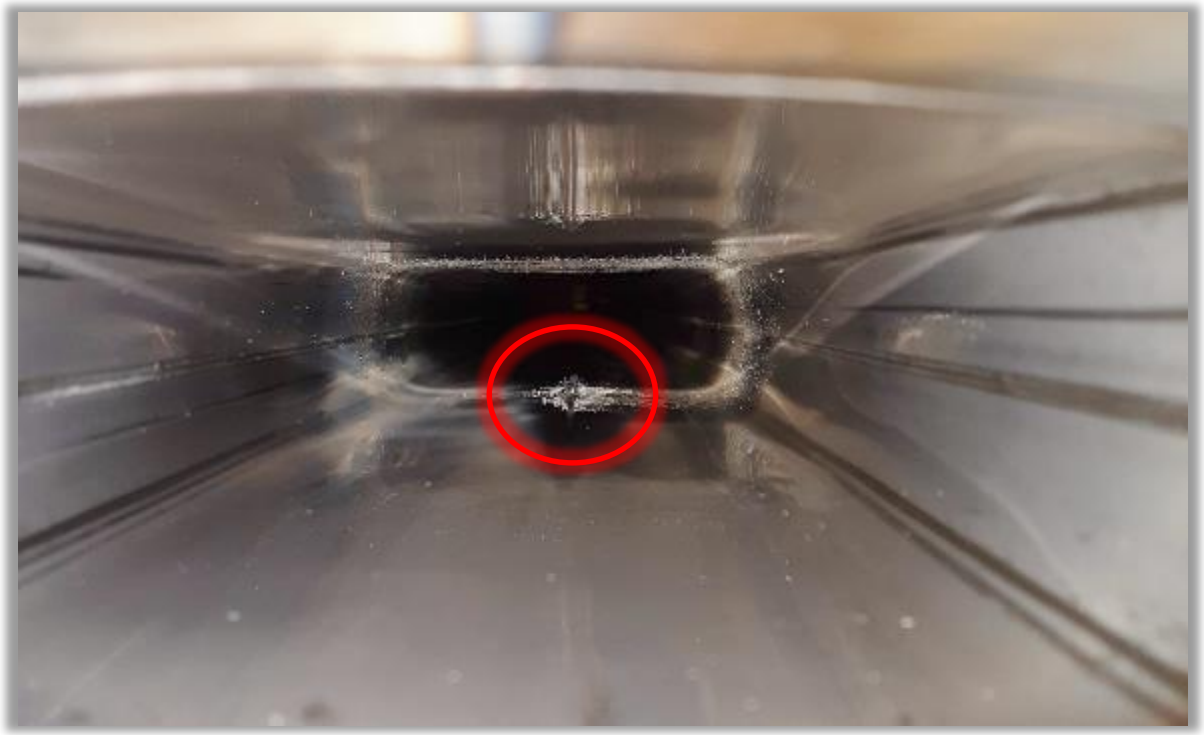
- New amplifier (G.J. Fokker): charge amplifier, 0-100 MHz BW, 1x-10x-100x-1000x gain.
  - BW more adapted to AG measurements (present amplifier lacks DC to 50 KHz response)
- Electronics (D. Belohrad): replace DAB (and BOBR) cards with VME FMC Carrier (SVEC)
  - Fully supported by BE/CO
  - Compatible FMC ADC adapted to BSRA data stream available and supported
  - Avoids artifacts due to parallel integrators

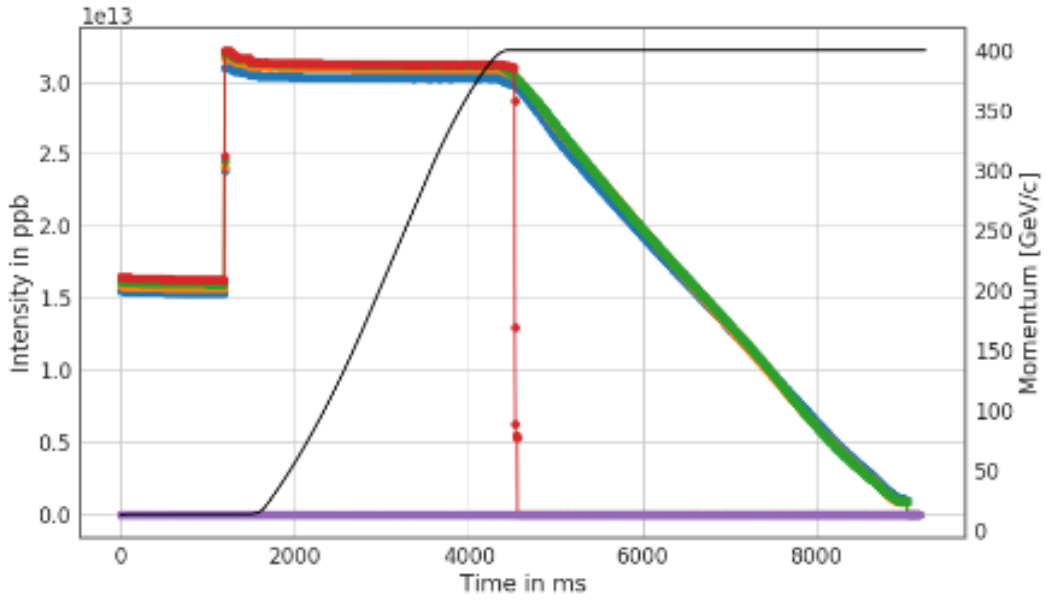
All functionalities of BSRA remain unchanged: outputs "AG clean" and "beam dump" flags depending on measured AG level (see "Calibration procedures and automated actions for the Abort Gap Monitors of LHC", LHC-BSRA-ES-0001).

Status: presently testing with BSRA lab model to improve amplifier performance. New FESA class should be developed end 2019 / beginning 2020.

SPS

- Following the incident in August 2018, request from SPS OP for additional interlocks to protect against fast losses.
- Document SPS-B-ES-0005 describing the requirements is under preparation…
- Request for:
  - dI/dt interlock
  - BPM interlocks
  - BLM software upgrade
- Presentation from Kevin tomorrow with more details…

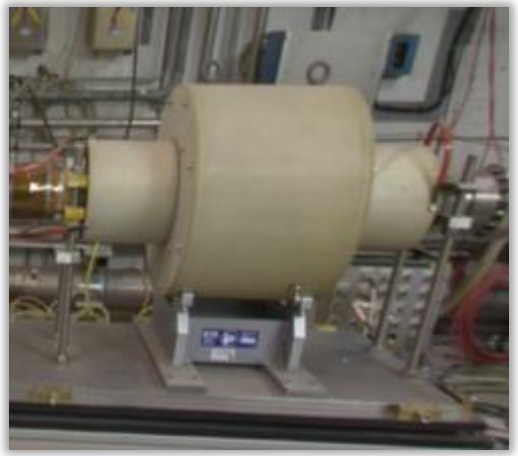




SPS dI/dt Interlock

Integration time	Total loss threshold	Average loss rate
1 ms	3e11 p+	3e11 p+/ms
10 ms	1e12 p+	1e11 p+/ms

- Note: must be able to detect losses during slow extraction (unbunched beam) → DCBCTs
- Propose to use the LSS5 DCBCT system
  - Used for NA ions personnel protection
  - Redundant detectors & acquisition chain
- Existing VME acquisition is too slow (200sps)
- New development using BI-standard VFC
  - Can reuse many parts of LHC DIDT (HW+FW)
- Requested 3e11 p+ in 1 ms is at the limit of the detector analogue performance
  - Relaxed specification to be finalised
- Plan to install first prototype during LS2
  - Need some commissioning time afterwards!
  - Longer term: looking into 24-bit system (as in LHC)



SPS BPM Interlocks

SPS BPM system will be completely renovated during LS2

- MOPOS → ALPS

Two interlocks requested from new system:

1. Interlock throughout the cycle from 8 arc BPMs
   - Fast turn-by-turn interlock (similar to LHC interlock BPMs)
   - Hardware input to BIS
2. Extraction bump interlock in LSS4 and LSS6
   - Orbit measured before extraction
   - Software interlock

Both interlocks are foreseen in the new ALPS firmware

- Hardware interlock will reuse the existing CIBU connection in BA1

Conclusions

Multiple BI systems related to machine protection will have modifications during LS2:

- New LHC interlock BPM validation system will be installed
  - Existing system will be maintained in parallel
  - Full installation after successful validation
- New LHC dI/dt system will be finalised
  - BIS channels initially disabled
- Upgraded LHC BSRA acquisition
- New SPS dI/dt system
- New SPS interlock BPMs

Adequate BI commissioning and validation time must be foreseen during machine commissioning!

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