Interlock Systems

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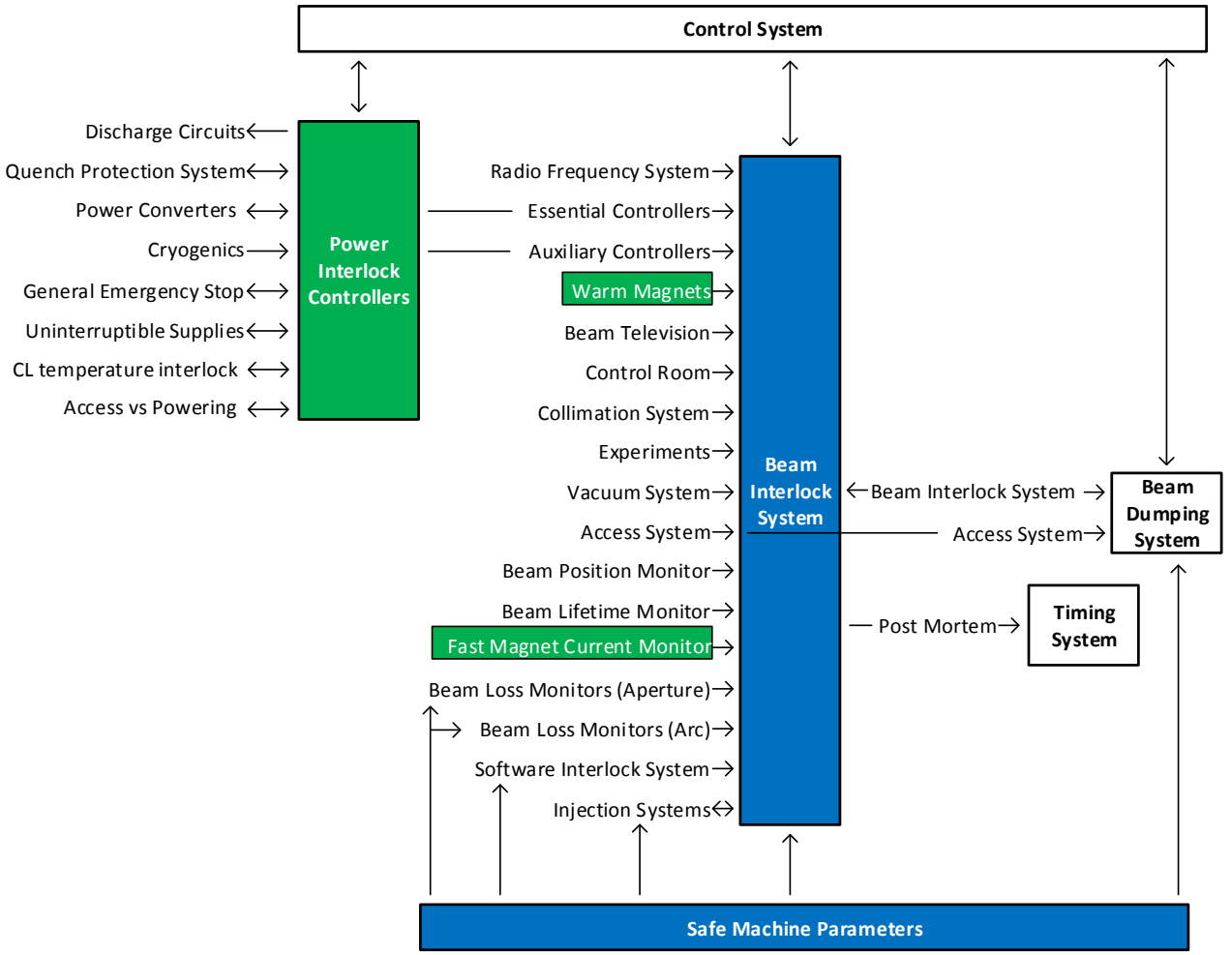
7-8 May 2019 - MPP Workshop 2019

LHC MPS layout



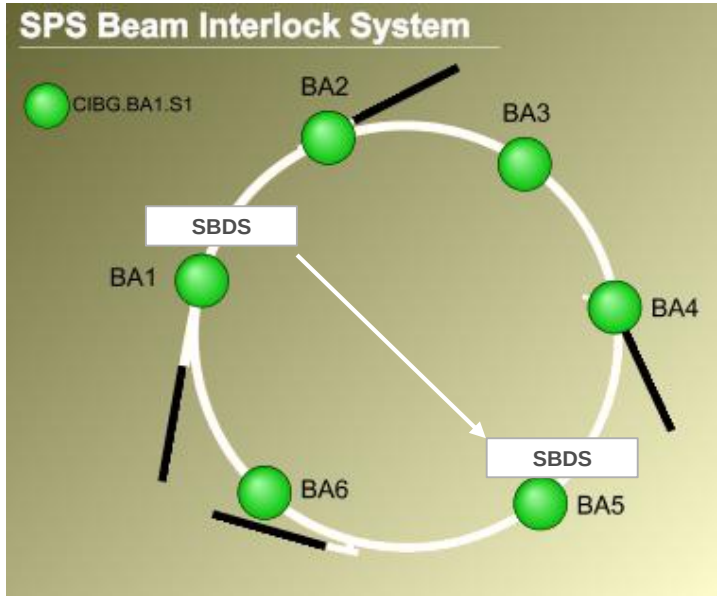
Beam Interlocks

Powering Interlocks

Beam Interlock System
BIS

SPS-ring BIS: Reconfiguration

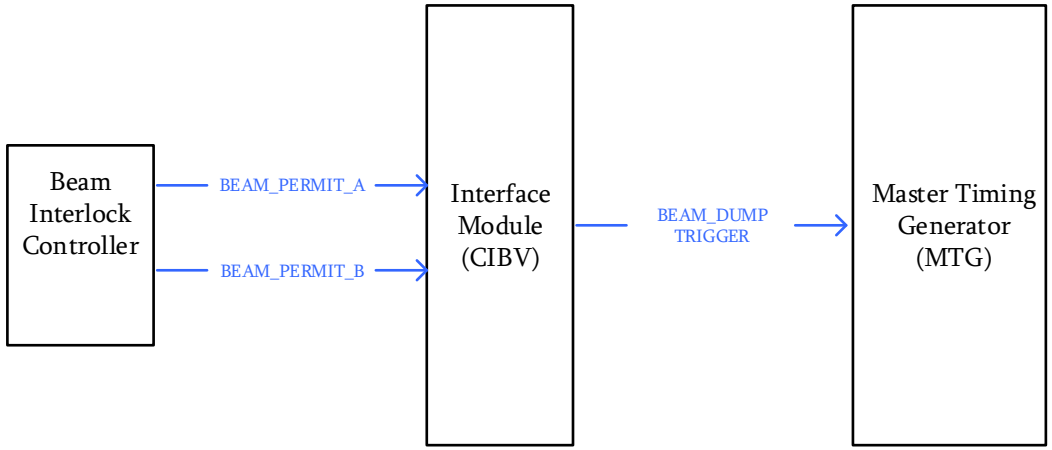
- Reconfiguration required following SBDS relocation:
  - New CIBU connection from SBDS in ECA5 to BIC in BA5
  - New fibre optics from SBDS in ECA5 to BIC in BA5
  - Frequency generator board (CIBG) to be relocated in BA5
  - TSU integration as client of the Beam Permit Loop
  - Reference DB and software tools to be updated
  - Dry run in collaboration with TE-ABT to test arming procedures, frequency detection, etc

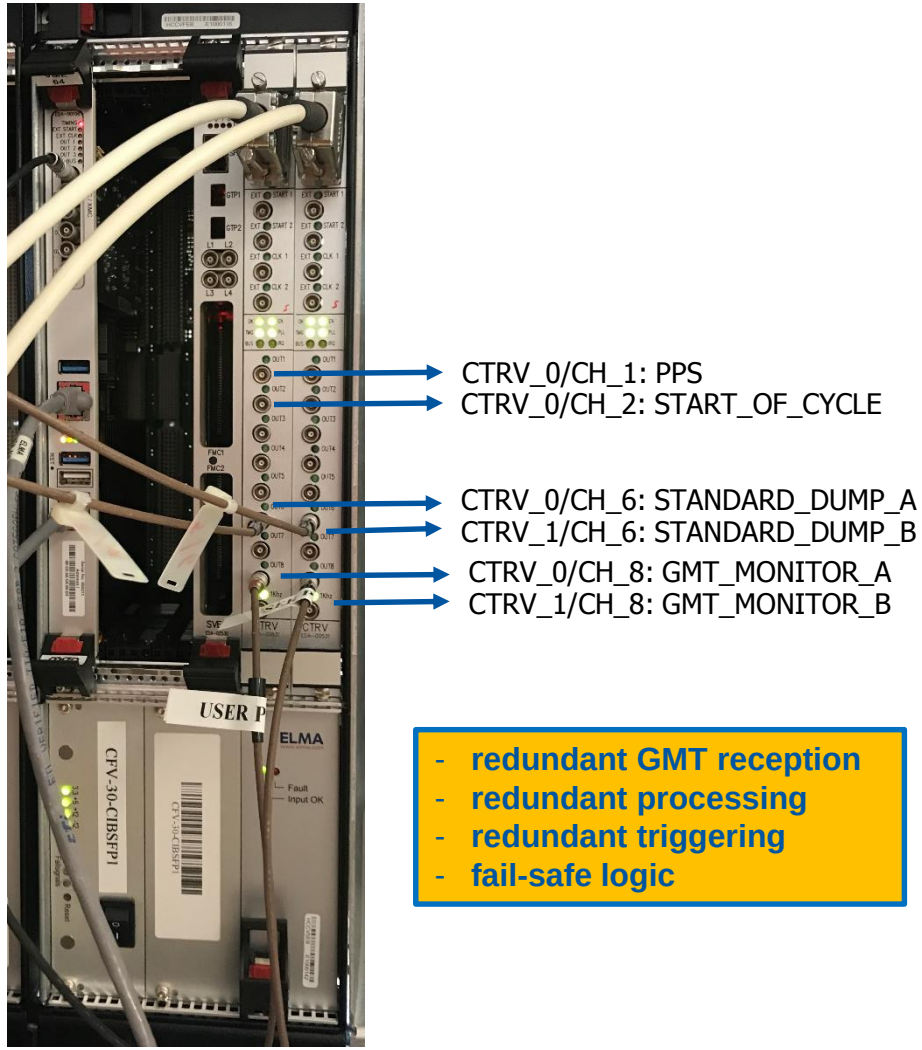


SPS-ring BIS: New connections

- **GMT monitoring**: aiming at detecting failures on timing distribution
- **Standard Dump**: “SX.KIKDMPTG-CT” timing event will trigger a beam dump request through the BIS (see G. Kruk’s talk)

- **Beam dump event**: beam dump trigger from BIS to GMT





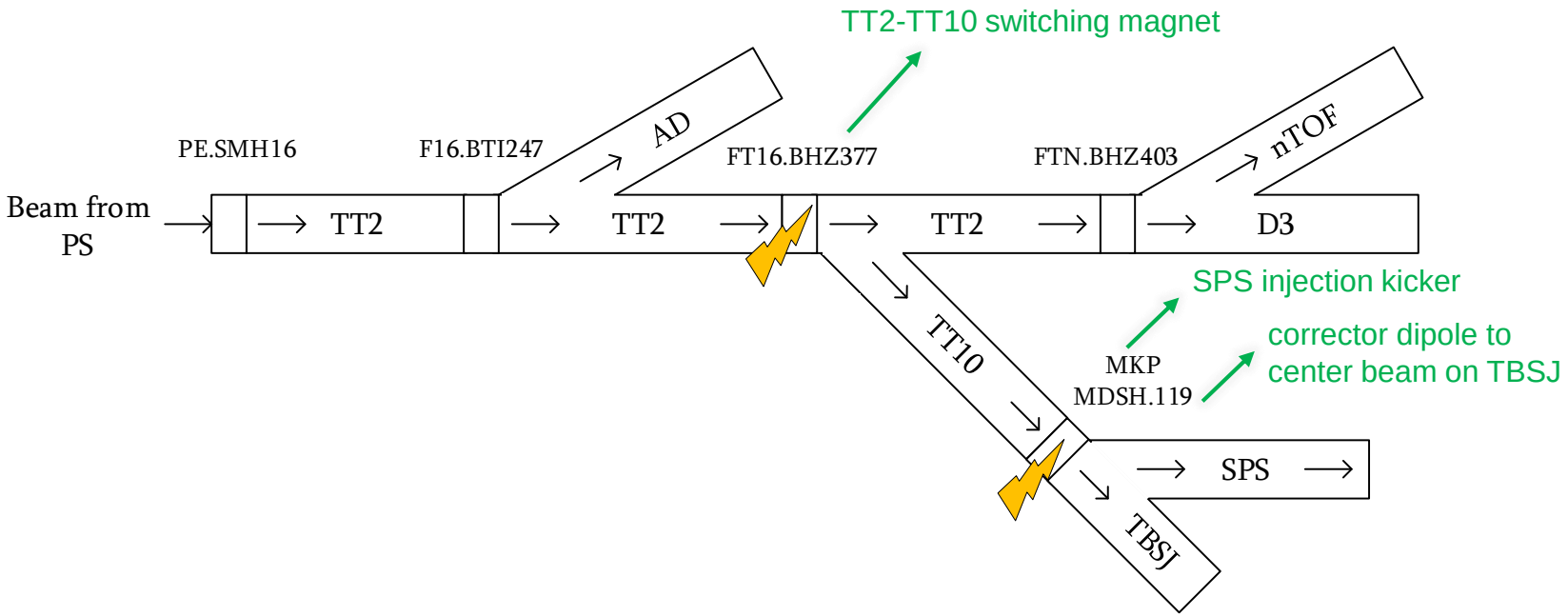
- redundant GMT reception
- redundant processing
- redundant triggering
- fail-safe logic

SPS Injection Interlocking - Motivation

1) the SPS Beam Dump System (SBDS) will be relocated from LSS1 to LSS5 and **the existing ABT link between the SBDS and the Injection kicker (MKP) will be removed** => injection inhibit through the SPS-Injection-BIS

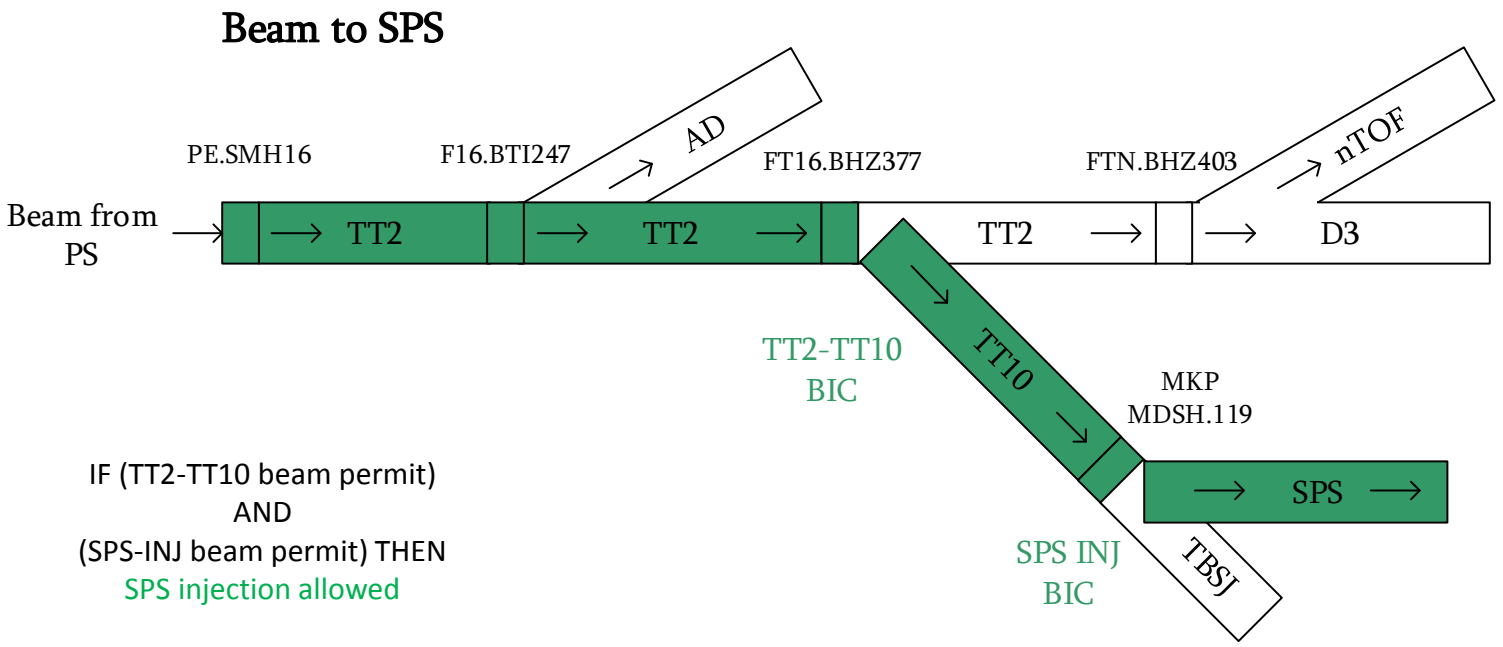
2) after the LIU consolidation, **beam brightness will increase and beam energy/intensity can reach damage thresholds at the TBSJ** (see Thermo-mechanical studies of the TBSJ for LIU beams) => a highly dependable interlocking solution has to be provided

SPS Injection Interlocking - From PS to SPS



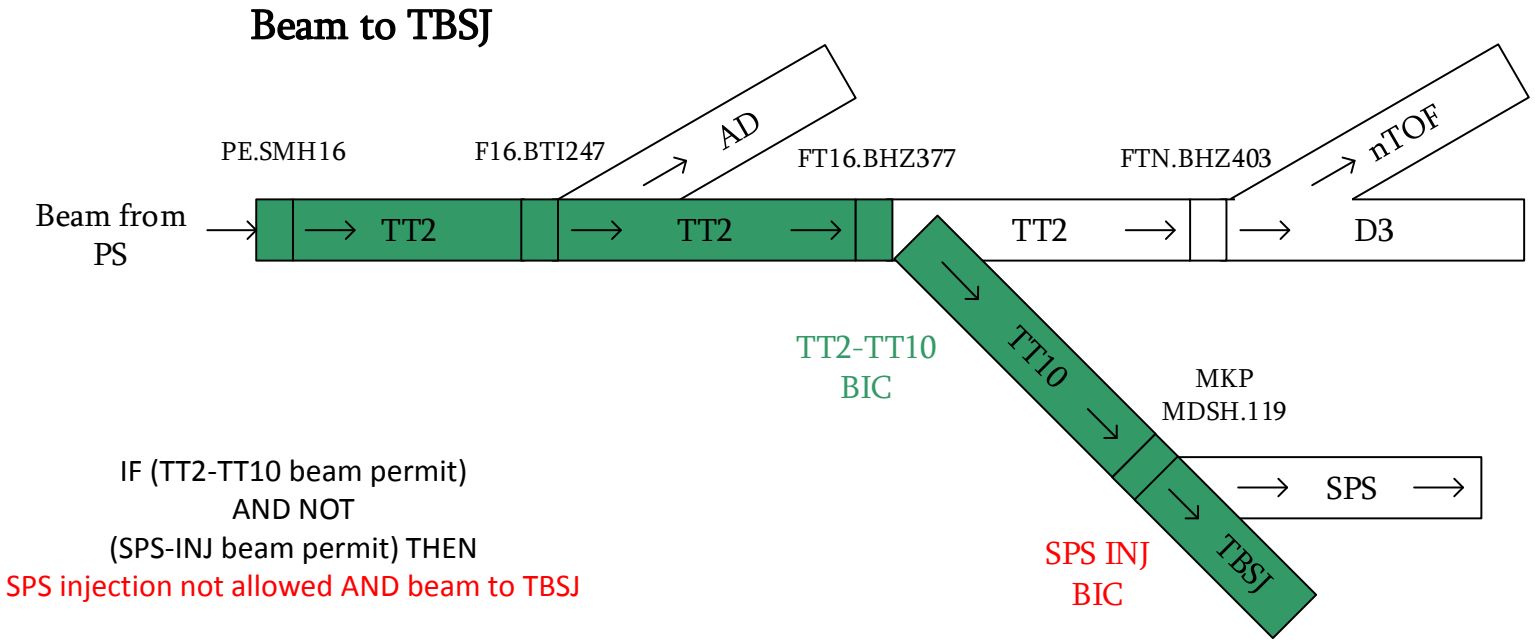
PS-TT10 Extraction Permit ⟵ SPS Injection Permit ⟵ SPS Beam Permit

SPS Injection Interlocking - Strategy (1/3)



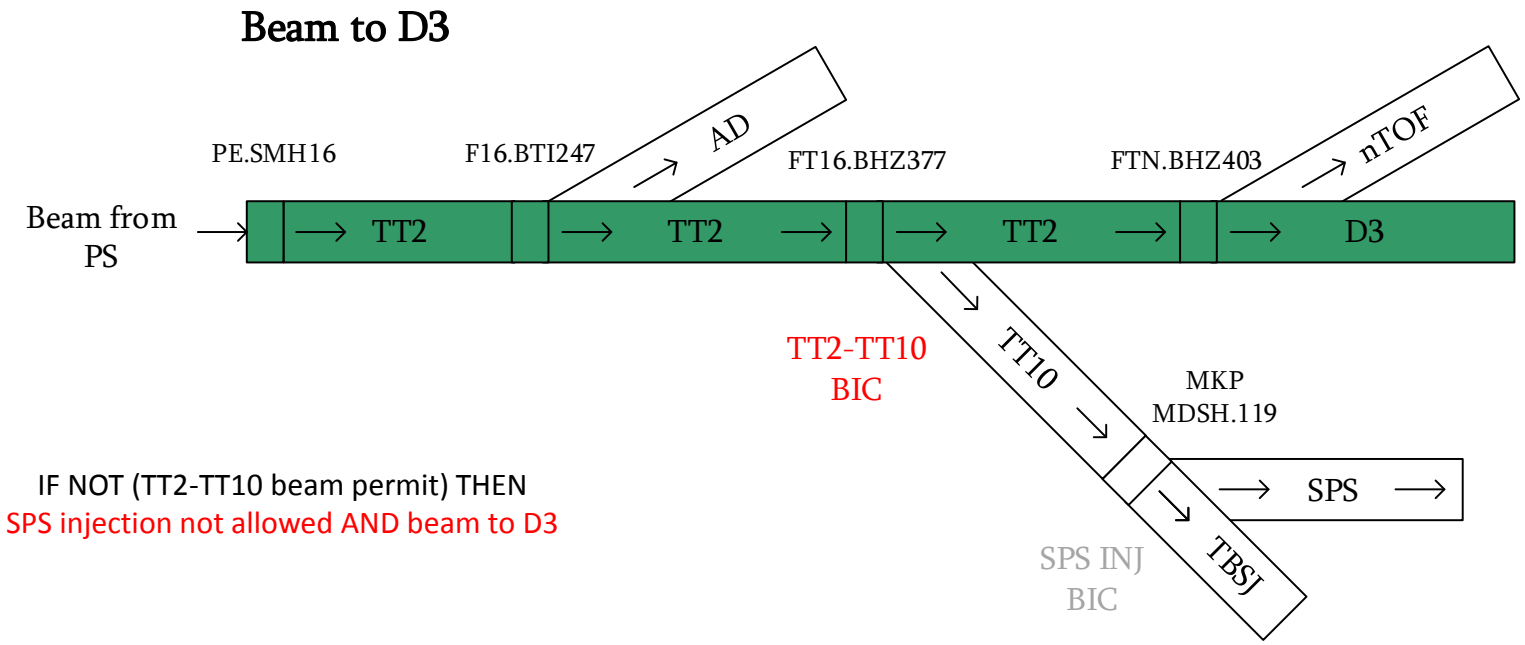
IF (TT2-TT10 beam permit)
AND
(SPS-INJ beam permit) THEN
SPS injection allowed

SPS Injection Interlocking - Strategy (2/3)

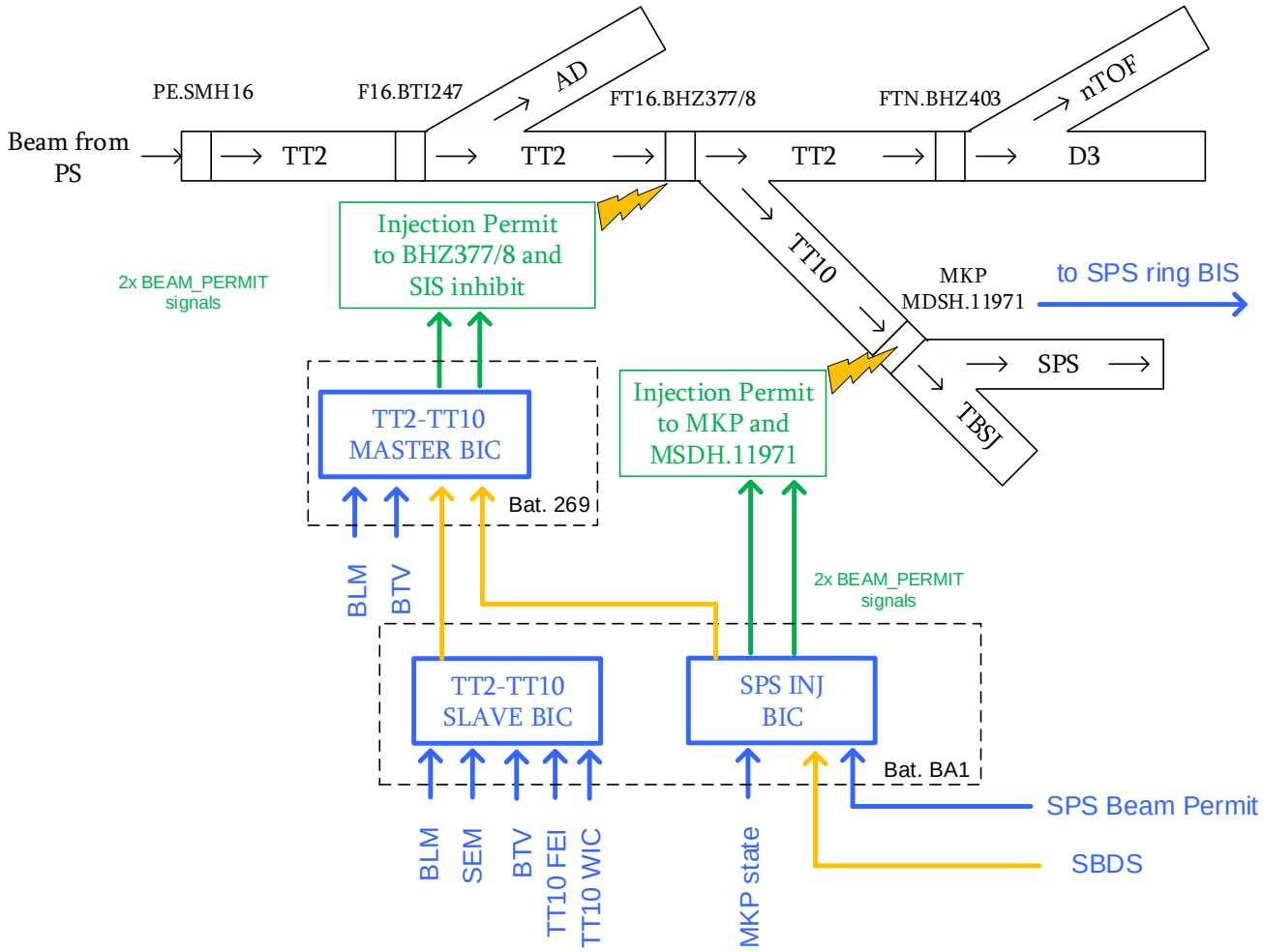


IF (TT2-TT10 beam permit)
AND NOT
(SPS-INJ beam permit) THEN
SPS injection not allowed AND beam to TBSJ

SPS Injection Interlocking - Strategy (3/3)



SPS Injection Interlocking - Architecture



SPS Injection Interlocking - New failure modes

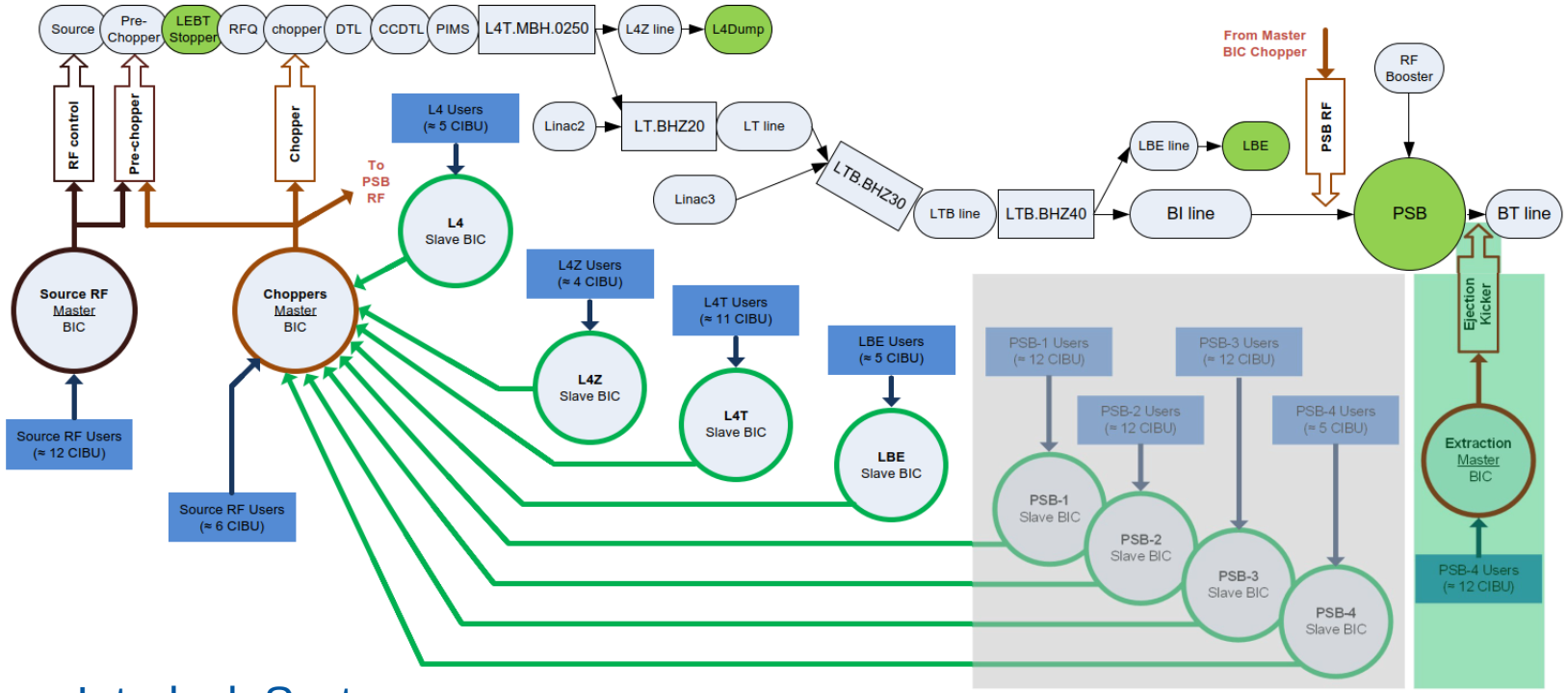
1) Impact of injecting a new beam when a **beam dump has just been triggered**
   a. Risk of injecting a new beam with no possibility to dump it
   b. Consequence of increased length between SBDS and MKP
   c. Mitigation: Proposal to implement a delay (2 turns) between the dump request and the dump trigger

More details by V. Kain tomorrow

2) Impact of injecting a new beam just after **MKDV erratic**
   a. Risk of injecting and accelerating a new beam with no possibility to dump it
   b. Consequence of additional delay required to inhibit injection (i.e. delay from ECA5 to BA1)
   c. Mitigation: Proposal to use the MDSH magnet to dissipate the beam in the ring

New BIS architecture in LINAC4 and PSB

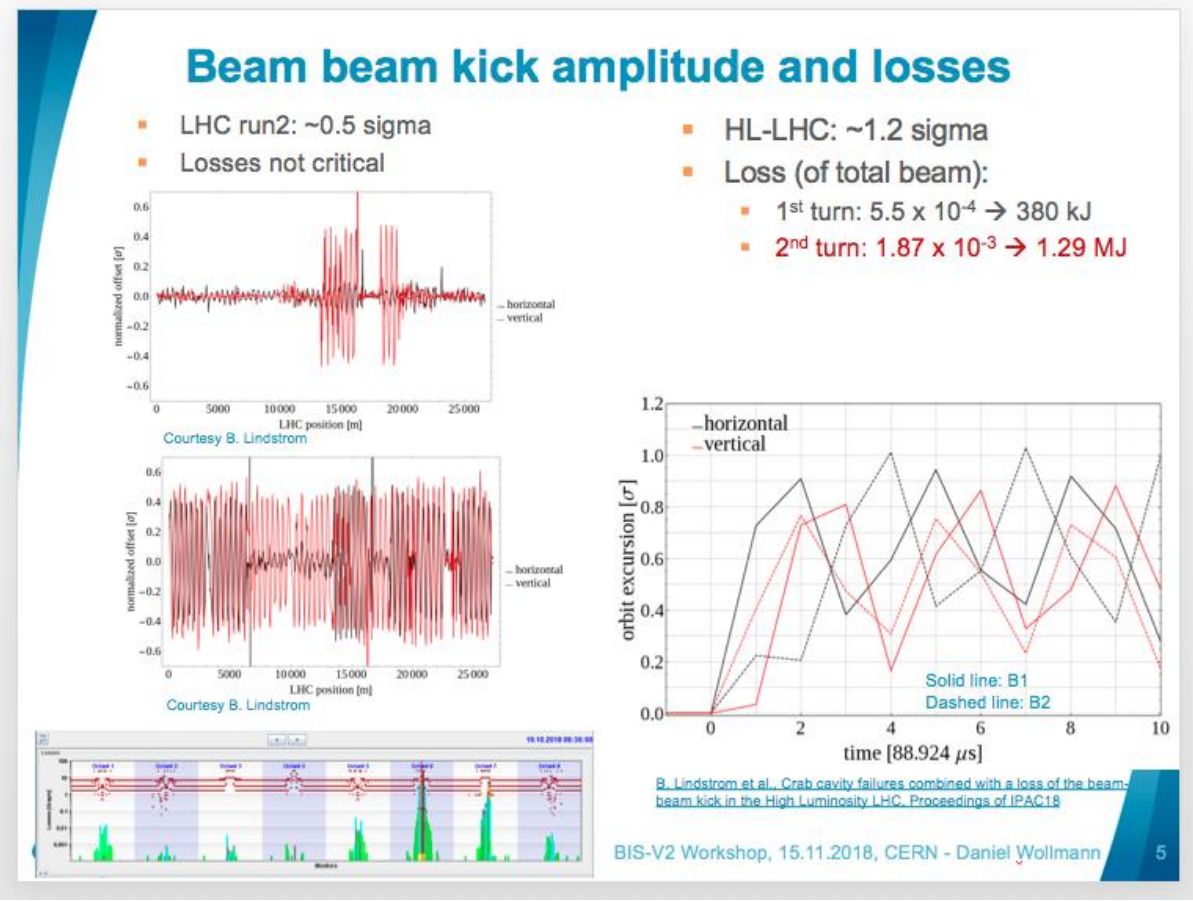
- New interlock architecture in Linac4, TLs and PSB
- 5 new slave BICs connected to Chopper Master BIC (PSB-1, PSB-2, PSB-3, PSB-4 and LBE)
- BIC Master equations re-configured



More details by B. Mikulec and D. Nisbet tomorrow

Beam-beam kick effects in LHC

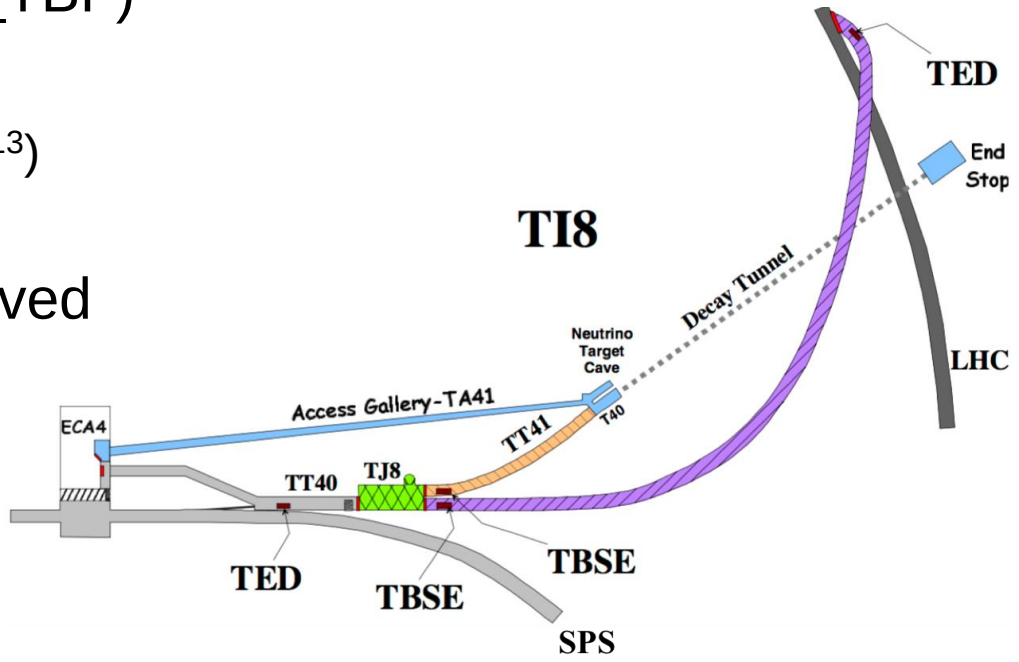
- Extraction of one beam causes a missing beam-beam kick in the other beam, i.e. ultra fast orbit offset, leading to beam losses in IR7 (see D. Wollmann at BIS 2v0 workshop)
- For HL-LHC, the beam-beam kick is reaching critical levels, risking to cause damage in the collimation system if beams are not dump swiftly after each other
- Reliable linking of the two beams required for high intensity operation
- **Clarify asap the consequences for Run 3!**



Safe Machine Parameters
SMP

SMP flag for SPS-LHC TL TED stoppers

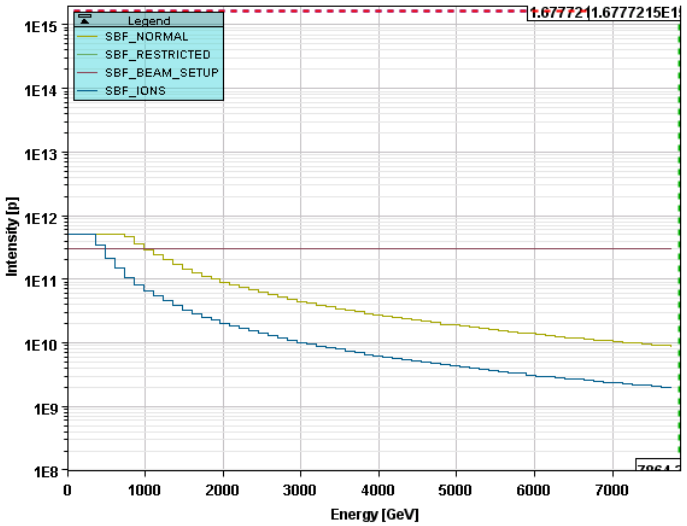
- TEDs will not be able to withstand a full 25 ns LIU batch consisting of 288b
- New machine protection strategy with LHC beams after LS2 (SPS-OTH-ES-0001)
- The maximum intensity to be extracted with TED in beam ≤ 3.34 x 10^{13} protons
- New SMP flag => SPS TED Beam Flag (SPS_TBF)
- Logic:
  - SPS_TBF = *true* when (SPS_INTENSITY ≤ 3.5 x 10^{13})
    else SPS_TBF = *false*
- SPS_TBF transmitted over the GMT and received via a standard timing board (CTR)
- 4 ELMA 3U VME chassis to be installed



SPS-LHC transfer line for beam 2

SMP flags in LHC

- Review Setup Beam Flag equations?
  - SBF_BEAM_SETUP (3x10^{11}p) is used for almost any MD.
  - Is that good in terms of safety?



- Suppression of UNSTABLE_BEAMS mode?
  - UNSTABLE BEAMS used for the calculation of the Moveable Devices In (MDI) flag

if (**PHYSICS_ENERGY** = TRUE)
AND
(BEAM_MODE = "**STABLE BEAMS**" OR BEAM_MODE = "**UNSTABLE BEAMS**" OR BEAM_MODE = "**BEAM DUMP**")
AND
(**BEAM_SQUEEZED** = TRUE) then
MDI = TRUE
else MDI = FALSE

  - Removing the UNSTABLE_BEAMS mode does not have an impact on the flag calculations, provided the beam mode enumeration is maintained as it is.

Other requests

- Reliable transmission of bunch intensity in HL-LHC:
  - For TCDQ levelling: due to the TCDQ damage limit, allowed TCDQ position depends on bunch intensity
  - For beam-beam kick effect: kick scales with bunch intensity
- Transmission of SPS energy and intensity:
  - For beam instrumentation equipment
- SMP v2.0 Workshop - 21 June 2019 at CERN

Powering Interlock System
PIC

Energy dependent masking of GPM

- Experience showed that 75% of the 600A EE openings in Run 2 were due to the activation of the GPM and only 25% due to individual openings
- In 30 % of the cases the activation was not necessary for protection due to the low energy stored in the magnets (i.e. at injection energy)
- In order to reduce the number of openings of the 600A EE and ultimately to reduce the maintenance cost, preserve and extend the life of the 600A EE systems, the GPM will be automatically disabled as a function of the current level in the main circuits
- Implementation options:
  - a) FESA class: get main circuit currents from PC gateway, calculate and communicate with PIC PLCs
  - b) SIS: get main circuits currents from PC gateway, calculate and communicate with PIC WinCC OA

Review criticality of electrical circuits

- **ESSENTIAL or UNMASKABLE** (if such a circuit fails, the beams will be dumped under any condition, also for safe beams): RB, RQD/F, RQX, RD1-4, RQ4-RQ10
- **AUXILIARY or MASKABLE** (if such a circuit fails, the beams will be dumped only if beams are unsafe. So for unsafe beams, an auxiliary circuit will do the same as an essential): RCS, RQT%, RSD%, RSF%, RQSX3, ROD, ROF, RCBXH/V and RCB%
- **NO IMPACT** (if such a circuit fails, the interlock will only stop powering but will not dump the beam): RCD, RCO, RQS.%, RSS

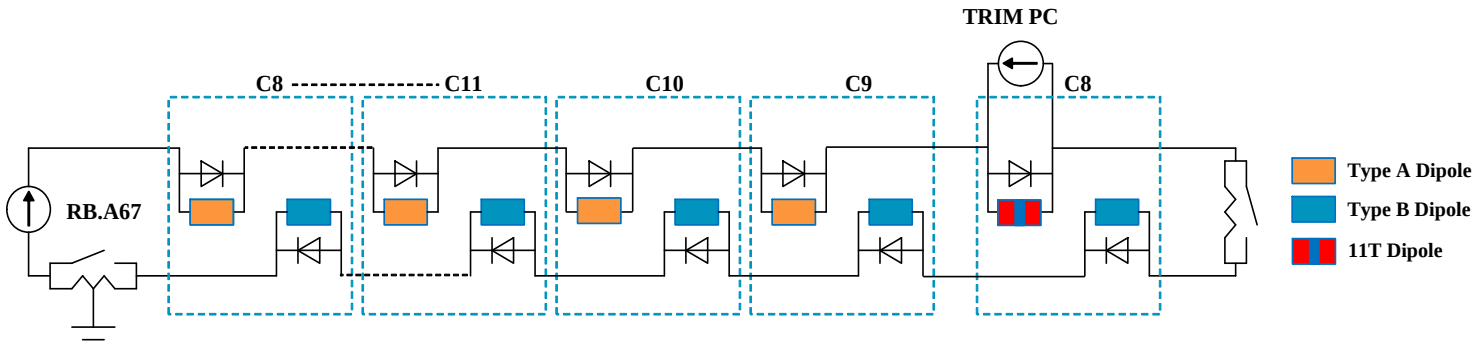
- In Run 1: RQSX3 family was included in the Maskable configuration after trip provoking fast orbit changes and beam losses in IP7 (EDMS 1203408)

- In Run 2: 2 trips of RQS.A81B1 @ 16.06.2017 that led to increasing losses and dumped on BLMs. This was presented at the MPP and no action was finally taken on the RQS family.

- For Run 3: Configuration reviewed by BE/ABP and proposed to keep as it is

New interlock for 11T dipole

- 11T trim circuit to be added as an independent circuit on the PIC (B1 type)
- FPA on the RB circuit will be propagated to 11T trim PC via GPM
- Quench detection for 11T current leads connected to PIC quench loop
- New trim Power Converter interfaces to be connected to PICs in RR73/77



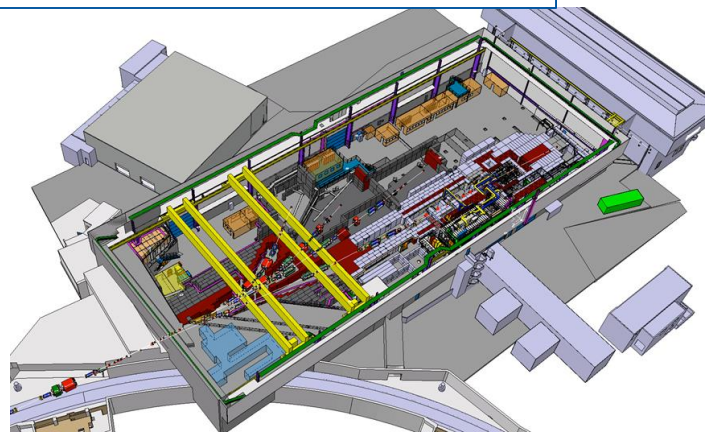
Main dipole circuit RB.A67 configuration for the HL-LHC with the 11T trim power converter.

Warm Magnet Interlock System
WIC

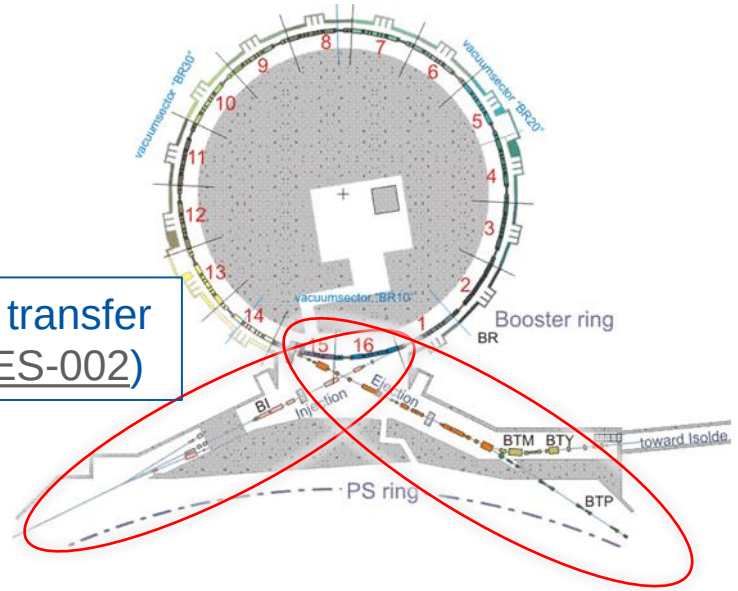
New installations for LS2

PS machine (PS-CIW-ES-001)

East Area (EA-CIW-ES-0001)

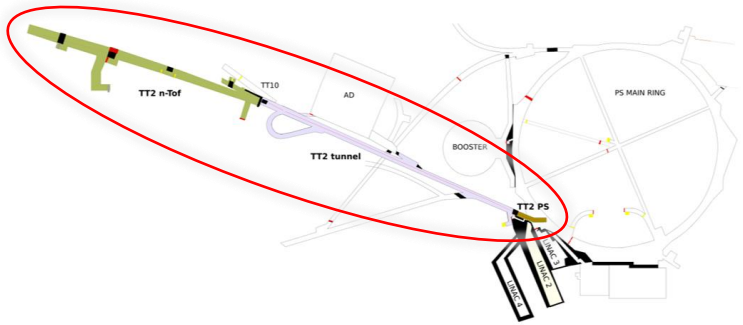


LT- LTB- LBE- BI transfer lines (CPS-CIW-ES-002)



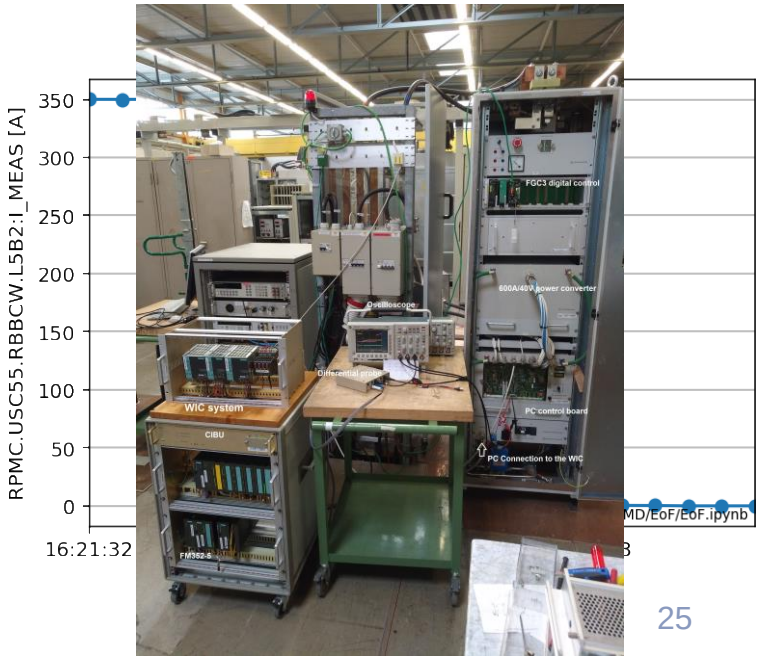
BT- BTM- BTP transfer lines (CPS-CIW-ES-003)

TT2- nTOF transfer lines (CPS-CIW-ES-001)



Connection to BIS of BBCW in LHC

- **Wire collimators for BBLR compensation (LHC-TC-EC-0019)**: Wire power converter added to the WIC Fast Boolean Processor to trigger a beam dump in case of internal PC failure
- Due to low inductance of the wire, the current decay and effect on the beam in case of powering failures is in the order of ~30 ms
- The WIC also protects the wire from overheating, by switching off the PC and dumping the beam
- SCADA-WinCC OA and PLC configuration need to be updated
- FGC3-BIS propagation time measured (~ 1.2 ms) is fast enough



New interface between SPS main PCs and BIS

- Upgrade of the obsolete interface between the main power converters of the SPS and the BIS (**SPS-CIW-EC-0001**)
- At present, in case of internal failures of the main power converters, the Hardware Interlock Loop (HIL) is responsible for switching off all other power converters of a given circuit and triggering a beam dump
- After LS2, the HIL will request the beam dump via the WIC – Fast Boolean Processors (response time <10 ms faster than present implementation)
- New FM352 modules to be added in BA3 and BB3 WICs

Fast Magnet Current Change Monitor FMCM

Activities in LS2

- No changes are foreseen on the FMCMs, beyond controls upgrades (i.e. FESA classes)
- For operation at 7 TeV, review circuit currents and re-adjust voltage dividers at the input stage of all FMCMs in the LHC
- Potential availability gain if improving electrical glitch rejection on sensitive power converters (i.e. RQ4.LR3/7 and RQ5.LR3/7) - see S. Uznanski at Evian ‘19

Conclusions

- All interlock related protection systems worked very reliably during Run 2
- For Run3, deployment of new interlock installations in LHC and injectors
  - Linac4 BIS/WIC, PSB WIC, SPS injection BIS, 11 T dipole, BBCW…
- Consolidation of BIS and SMP systems foreseen for LS3
- Future interlocking requirements for HL-LHC need to be clarified: SMP bunch intensity, linking of Beam Permit Loops…

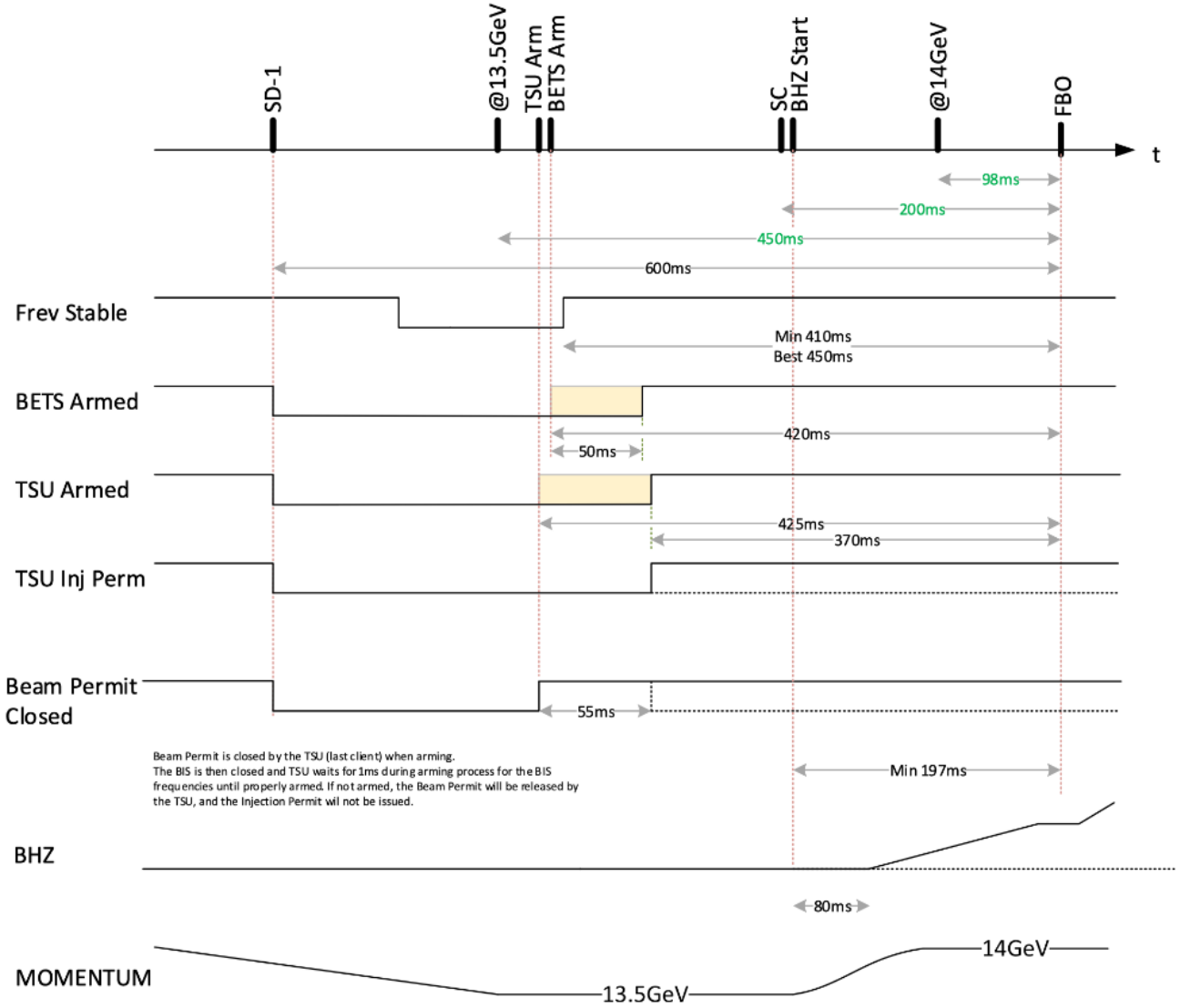
Thank you for your attention!

Spares

WIC beam dump matrix in Linac4 and TLs

- 3 WIC systems are installed to protect the resistive magnets in Linac4 and TLs up to PSB
- WICs connected to the Linac4 BIS to interrupt the beam in case of magnet overheating or power converter failures
- Proposed to exclude the status of certain power converters in the calculation of the “User Permit” signal sent to the BIS (**CPS-CIW-EC-0001**)
- Non-working corrector power converters should be possible to compensate with other correctors in order to restore an acceptable beam trajectory and help to maintain availability

SPS Injection Interlocking - Arming sequence



- TSU is the last client to rearm
- Only when TSU is armed, the SPS Beam Permit becomes TRUE
  - Frev stable
  - BETS armed
  - TSU armed
- SPS Injection Permit has to be given early enough for the Power Converters to play the required function (~350ms before beam)
  - Worst case will be SFTPro p+ (14 GeV)