Machine Protection Workshop 2019 Conclusions & wrap-up

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Follow-up topics1

- **TCDI positions versus optics changes** – interlocks, SIS check, distinct BP etc.
- **TL steering with full trains?** Or use 2x12b train in dedicated filling scheme? Timeline for use of automatic steering algorithms?
- BBLR wire finalization of interlocking spec for operational use & finalize tests on interlock delays with FGC2
- Automatic loss map checks, eventually integrated into EOFs and regular PM?
- Less invasive ways to proper setup of dump protection (new ATS optics changes a lot in IR6)
  - can asynch. dump tests be complemented with losses at each dump, bump method? What needs to be studied to answer this?
- (repetitive) automatic testing of BIS inputs integrated in AccTesting
- Reliable Diamond data as well in PM (NXCALS exists)?
- Max. allowed momentum losses in IR3 due to **lower RF voltage @ injection** (to mitigate power limit)
  - possibly update **thresholds in IR3**
  - **improved energy matching** between LHC & SPS
- Bypassing of 600 A EE systems (60) to increase powering system availability + equipment lifetime
  - prepare ECR & get input from EPC etc. for HW limitations of power converters
- Evaluate **criticality of missing beam-beam** kick in run 3
  - HW linking of BIS loops required via maskable input?
- New 600 A PC: test impact of failure in one redundant 400 A module on circuit protection (QPS)

Follow-up topics 2

- MKD-TCT & MKD-TCDQ phase advances
  - desired & minimal values
- **TCDQ – TCT – XRP during collide & squeeze with beta* levelling & crossing angle change**
  - Positions / thresholds / movement
  - Redundant limit: BETS, energy & beta* thresholds
  - How much complexity is necessary in Run3, what do we need to learn for HL?
  - Safe distribution of bunch intensity required
- TDE increased beam size at upstream window
  - bunch intensity and optics dependent limitations, will add complexity elsewhere
  - is that the way forward? Can it bridge time until we have new window (probably should not introduce such an additional constraint for a fairly easy HW change)? How can this be done safe and reliable? Impact on MDs?
- **Bunch intensity dependent limitations**
  - Do we need interlocks and whith which reliability?
  - How to use FBCT, DCBCT, BQM? SIS, SMP?
- TDE stresses on housing of DS window – complex simulations to be ctd
- Future material test in HiRadMat with LIU beams necessary, also include other dump line elements that were never tested for these intensity (BTVDD?)
  - Important to define damage limits for asynch dump cases for all involved materials
- TCTs: 5th axis?

Follow-up topics 3

- **DI/DT for LHC & SPS**, review & update interlock specs as input to BI
- BLMs: what is required as re-validation in case of (urgent) exchange from current processing board to new processing module during a run?
- What is needed for early commissioning of **injection interlock inhibit**?
- Would use of LICs in IR7 give us more ‘breathing’ space with fast losses, as this would allow an increase of short RS by factor 14?
  - what do we need to learn in run 3 in prep for HL-LHC?
- Diamond BLMs: do we need better specification of the use cases?
- BLM thresholds: update models for (new) collimators
- BCM thresholds versus BLM thresholds, ensure coherence!
- **BPMs in IR6**: specify **how to start with prototype system** in parallel to existing system in run 3 while assuring redundancy + define strategy how to switch if successful
- **DOROS** @ IR7 collimators: how many to interlock in future? Also for TCDS in IR6? SIS to BIS?!
- **SPS BPM extraction bump interlock**: HW or SW? – check and update specs!
  - could SIS do the job at all or is it too slow?

Follow-up topics 4

- **ADT** commissioning procedure? Define re-commissioning/**testing requirements** in case of changes/adaptations (especially for MD)?
- How to provide more transparency to OP after change of ADT firmware?
- Who decides to unlock ADT protections for MDs? How to assure no short-cuts are taken in procedures in particular for such potential critical equipment
- **MDs: Foresee dedicated slot for special MD conditions & preparations (ADT, COLL, …)**
- **Combined beta* & crossing angle leveling**: Define how collimator limits can be changed! Use discrete limit steps executed by outside instance such as e.g. sequencer, similar as in 2018? Sufficient, but not elegant? Leading into the future?
- **Define wish list priorities for collimation software upgrades with OP**. E.g. generation of collimators settings in LSA, revised temperature interlocks, ramp functions for crystals, …

Follow-up topics 5

- SIS masking policy to be extended by 'MD type' and automatic removal (e.g. PM injection interlock, …)?
- Which way to go for beta* reconstruction (LST or ki space)? Future solution ideally to work for all optics (high beta, ATS, flat,..)
- **Need to define asap data volume and latency requirements for SPSQC** use-case within **PM** if to become operational/interlocked (for the time being no 'official' PM use-case yet!)
- NXCALS latency impacting interlocking via XPOC, IQC & SPSQC & SPS quality checks as input for next cycle
- **rMPP** should be more involved during **Special Runs (MD like process)**?
- **Extension of MPP/rMPP to injectors? Starting with Linac4 LEB run?!**
- Propose major event template before end of LS2
- Mitigation of LVDT issues planned for ALFA (add cables)?
- Additional springs to be installed in AFT. Full changes to be discussed with MPP

Follow-up topics 6

- EXP magnets (solenoid/toroid) to be added to the PC interlock?
- **Alternative to broadcast energy and intensity SPS SMP** (only for SMP2)?
- Define interlocking strategy for SPS slow extraction
- Linac4: Continuous caesiation strategy/parameters to be determined and risks to be evaluated
- **Linac4 & PSB settings management**. Where and how to define appropriate settings?
- For criticial settings could MSC be used?
- External conditions upgrade: Hardware link or JAPC/CMW
- Should in the **longterm interlocking** be taken over by BIS and SIS or still done by central timing
- Implementation of a BIC for the PS in LS3 to replace external conditions for systems affecting all PS cycles? Harmonize interlocking strategy in accelerator complex?

Thank you

- Sabina for organizational support
- Session chairs
- Speakers
- All participants for active and valuable discussions

Follow-up topics will be taken into MPP

Session chairs to compile an executive summary by 7th June for inclusion in common workshop report (please use JACoW template)

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