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Silizium Labor Bonn

RD53A WAFER PROBING
SPECIAL PLOTS

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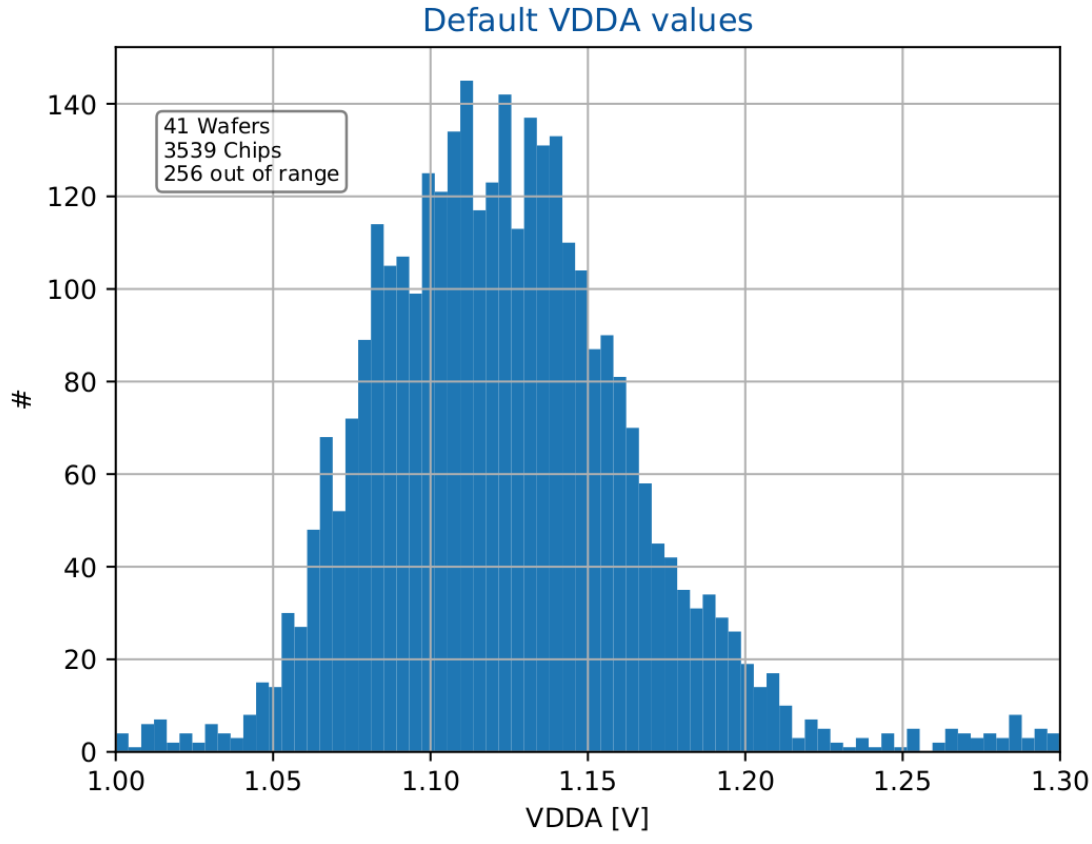
OVERVIEW

- Coming back to Aleksandra's observation from April 1st
  - VDDA slightly lower on the right-hand side of wafer?

- Waferprobing data:
  - Probed 41 wafers by now
  - 3500 chips for statistical analysis

  - So far only looked at **trimmed** VDDs (VDD @ optimal trim bit)
  - Now: Compare VDD at **default** trim bit (16)

VDDA


Default VDDA values
41 Wafers
3539 Chips
256 out of range
#
VDDA [V]
0
20
40
60
80
100
120
140
1.00
1.05
1.10
1.15
1.20
1.25
1.30

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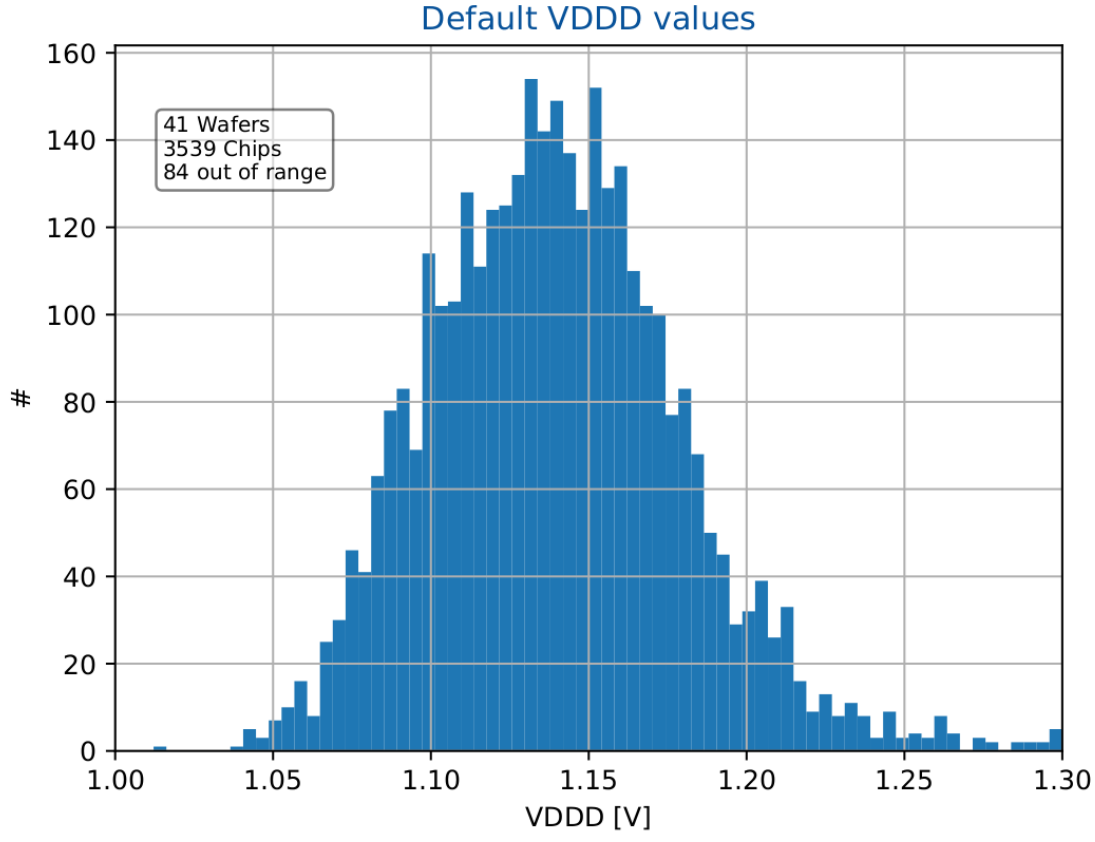
VDDD



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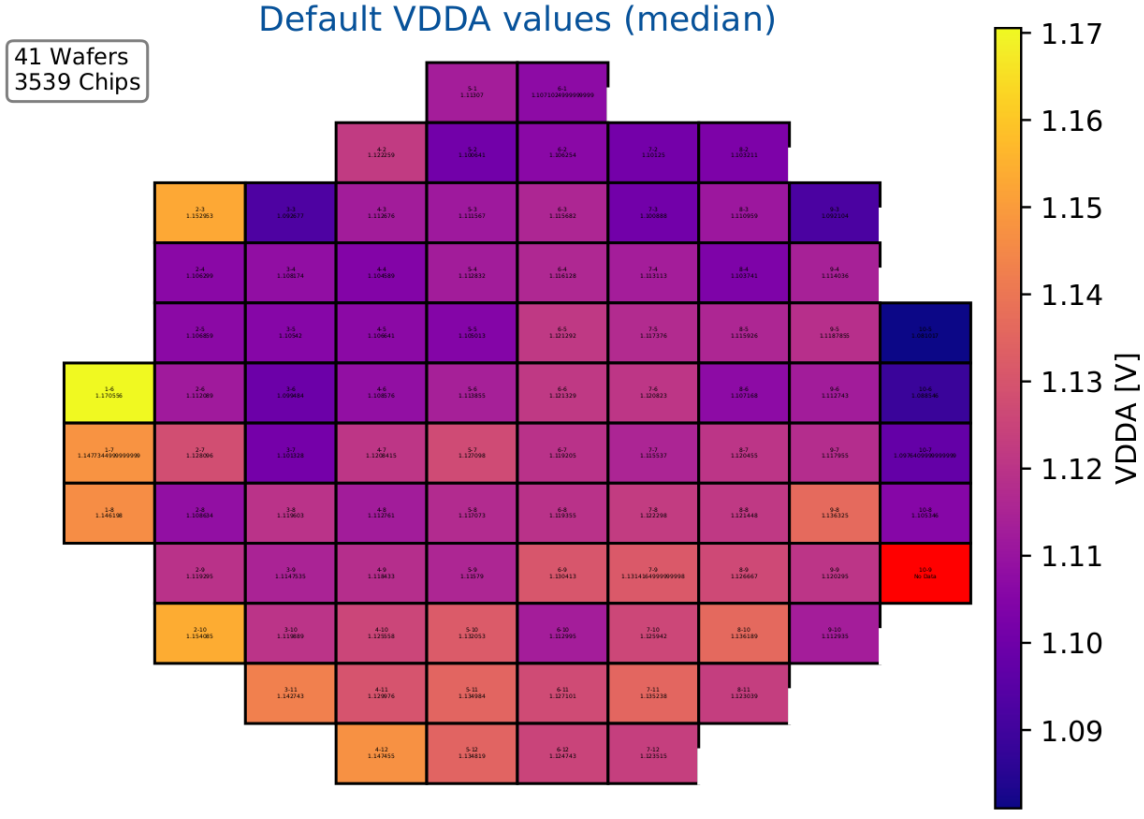
VDDA



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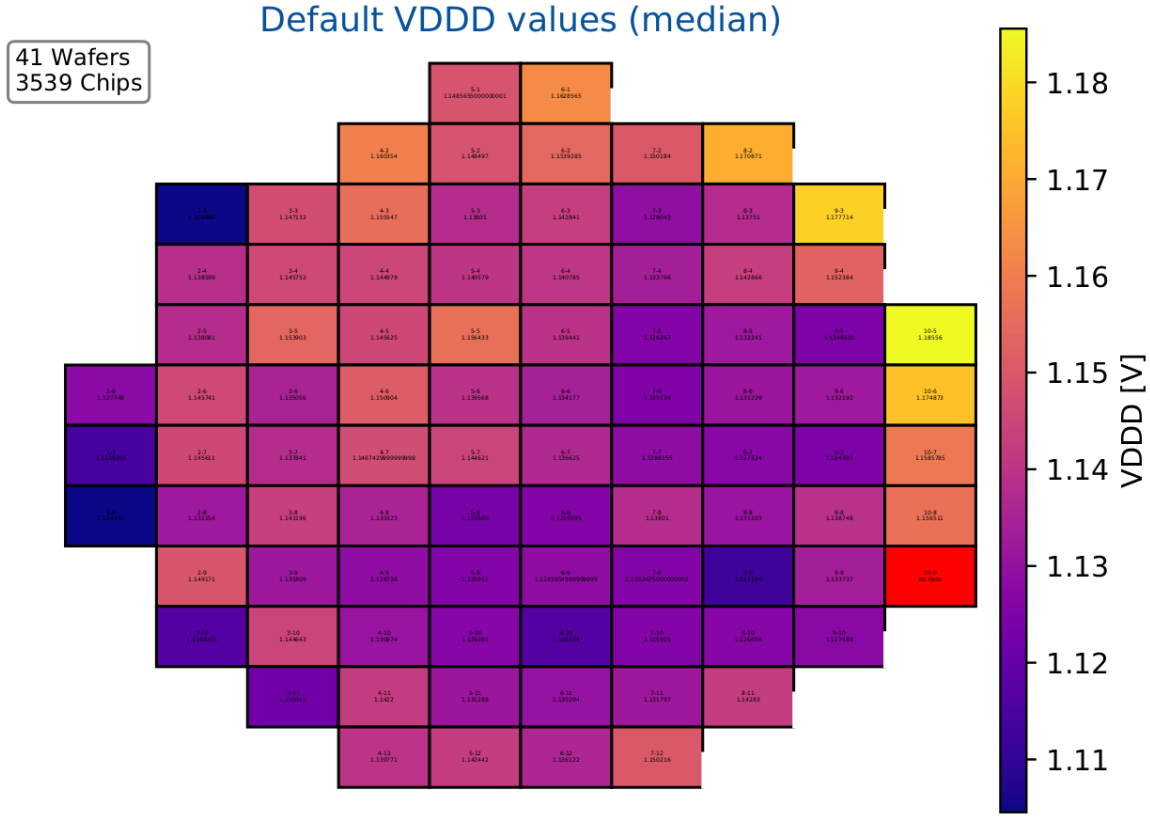
VDDD



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OBSERVATIONS

- **Positional dependence** of VDDA and VDDD on the chip position on the wafer
  - Overall **gradient ~ 80mV**

  - Sign of gradient is **opposite** for analog and digital
  - Possible explanation:
    - Master cells of analog and digital regulators are mirrored
    - Process variations might have opposite effect

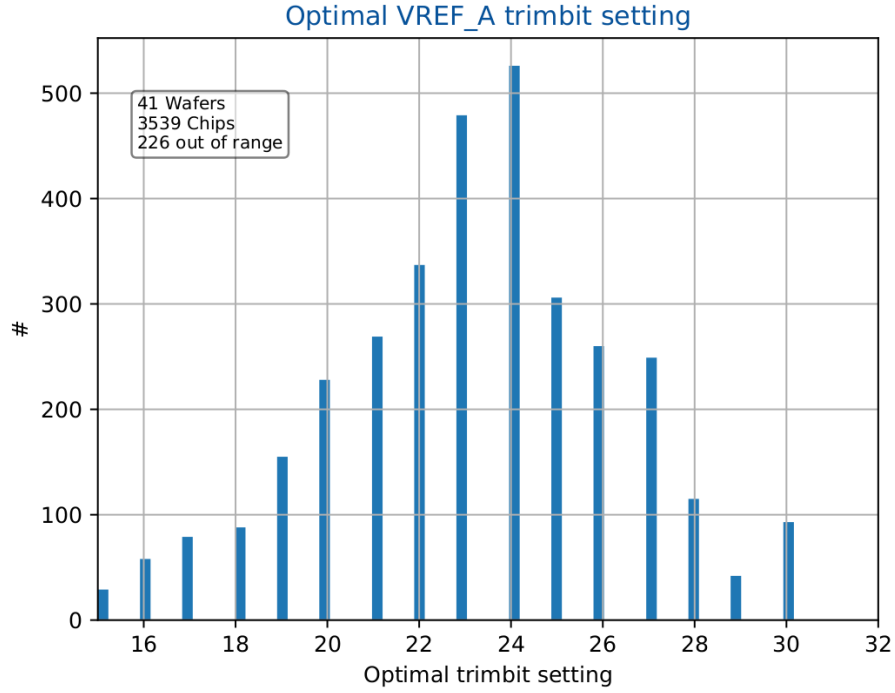
Conclusion

- There is an effect observed
- No reason to worry
- Absolute values of both VDD too low without trimming
  - Mitigate by higher default trim value from software?

VREF_A_TRIM

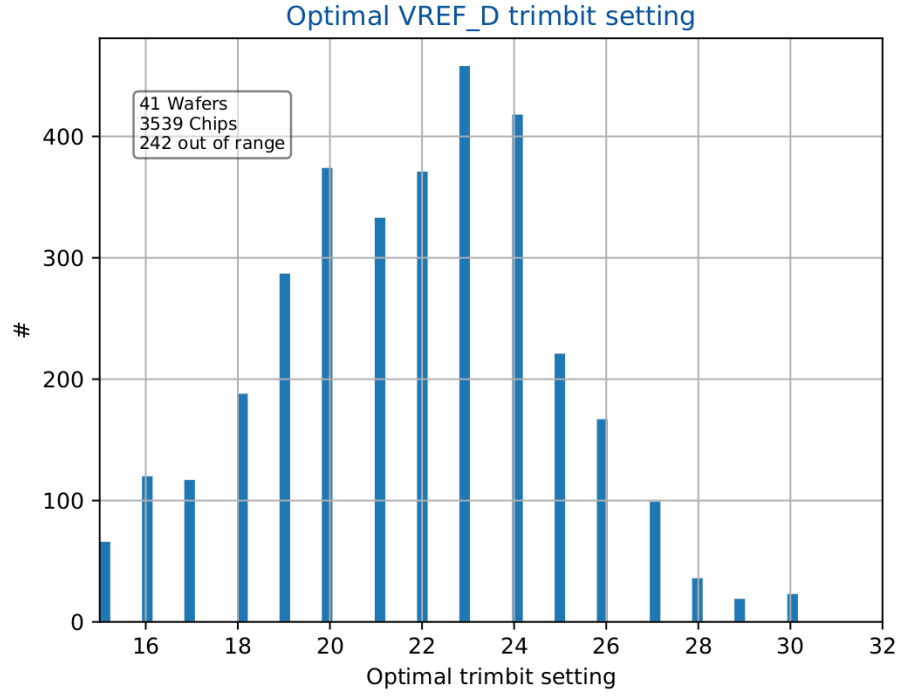
- Look again at optimal (VDD closest to 1.2V) trimbit setting

- Use VREF_A_TRIM = 24 as new default setting in software?
- Does not replace proper calibration but make initial communication easier
- Only concerns unprobed chips
  - Will get optimal value from database

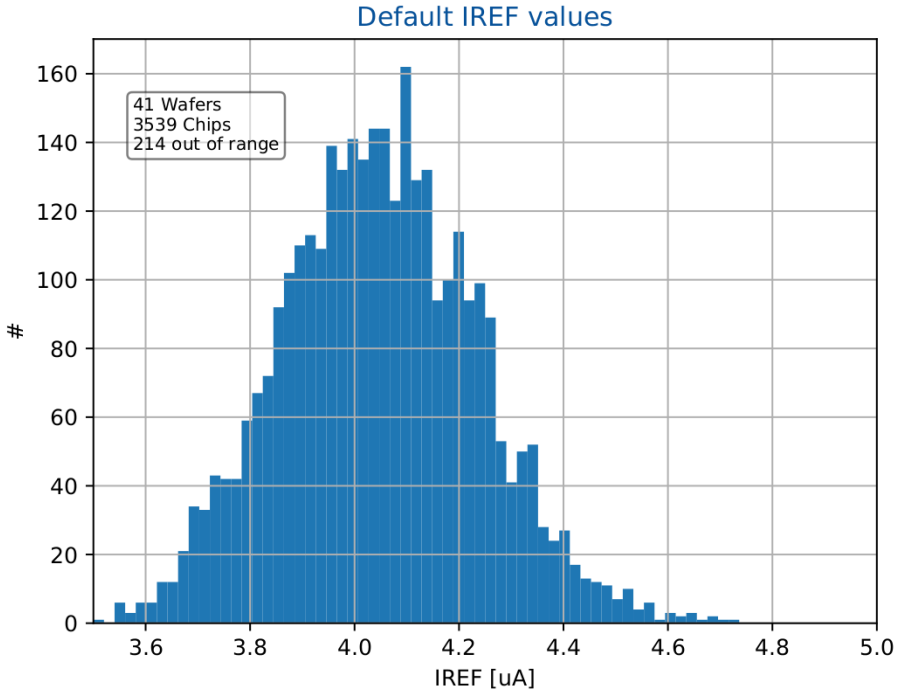


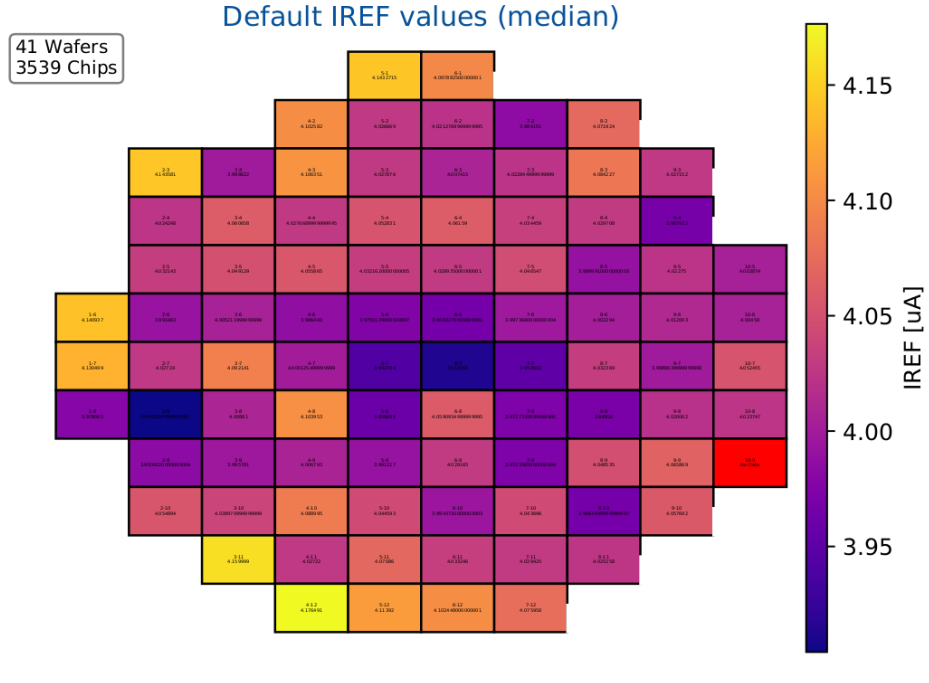
VREF_D_TRIM

- Use VREF_D_TRIM = 23 as new default setting in software?

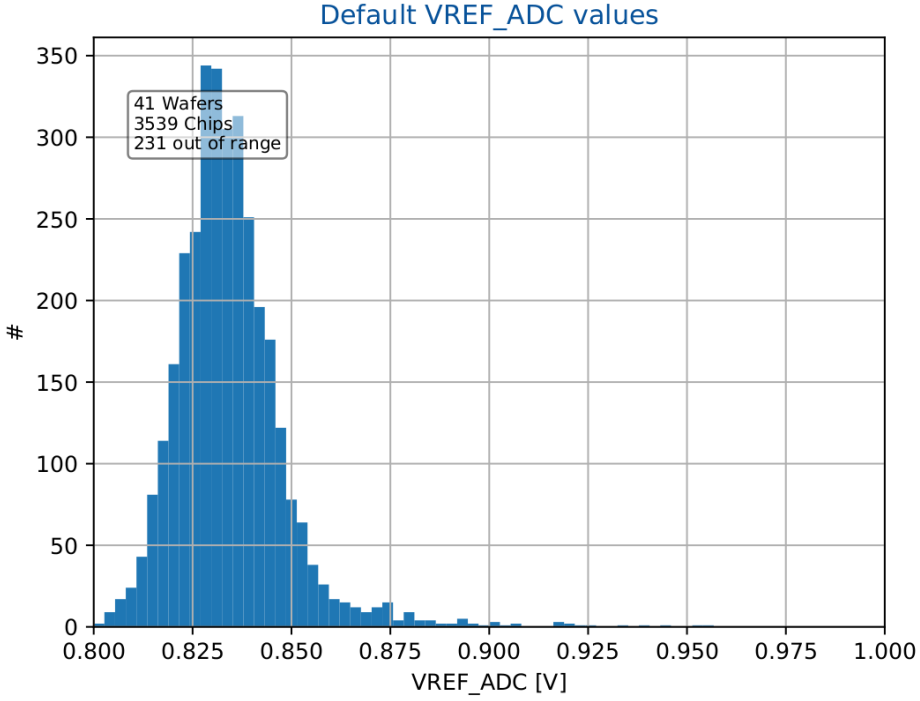


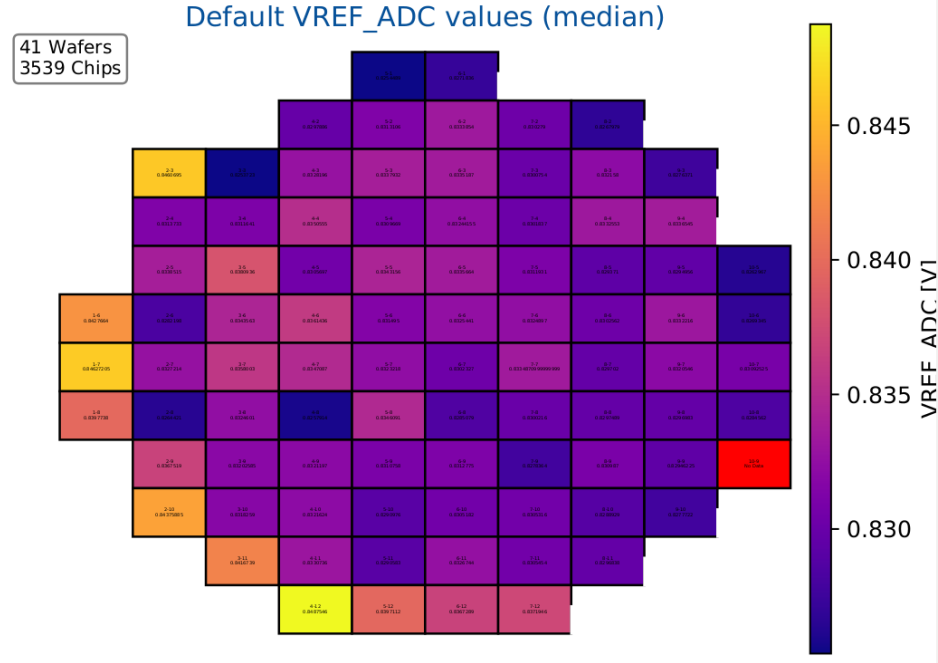
IREF


Default IREF values
41 Wafers
3539 Chips
214 out of range
#
IREF [uA]
0
20
40
60
80
100
120
140
160
3.6
3.8
4.0
4.2
4.4
4.6
4.8
5.0


Default IREF values (median)
41 Wafers
3539 Chips
IREF [uA]
4.15
4.10
4.05
4.00
3.95

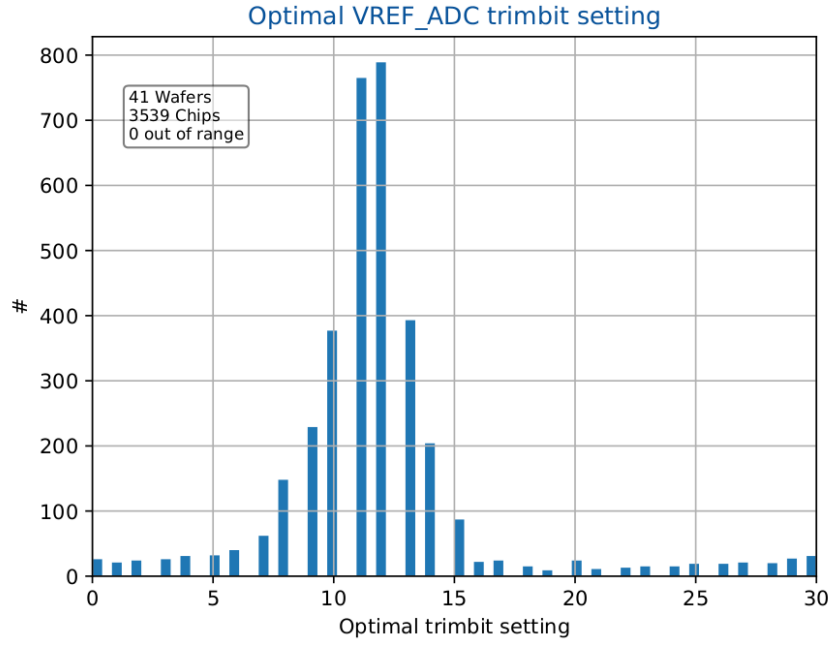
VREF_ADC


Default VREF_ADC values
41 Wafers
3539 Chips
231 out of range
#
VREF_ADC [V]
0
50
100
150
200
250
300
350
0.800
0.825
0.850
0.875
0.900
0.925
0.950
0.975
1.000


Default VREF_ADC values (median)
41 Wafers
3539 Chips
VREF_ADC [V]
0.830
0.835
0.840
0.845

VDDD

- Default trimbit setting is 0
- Use MON_BG_TRIM = 12 as new default setting in software?



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Backup

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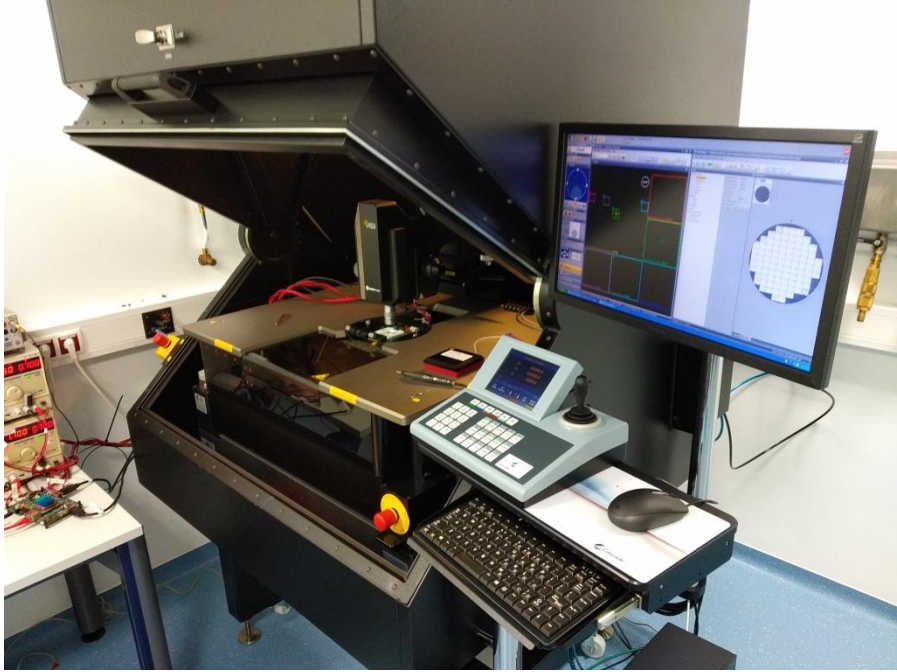
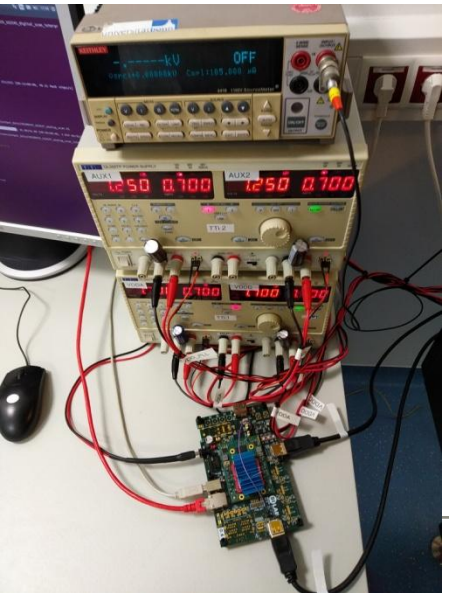
SETUP

- Cascade Microtech (formerly Karl Suss)
  PA-300-II semi-automatic 300mm probe station
- Generic LV power supplies (TTi QL355TP)
- Keithley SMU for analog measurements





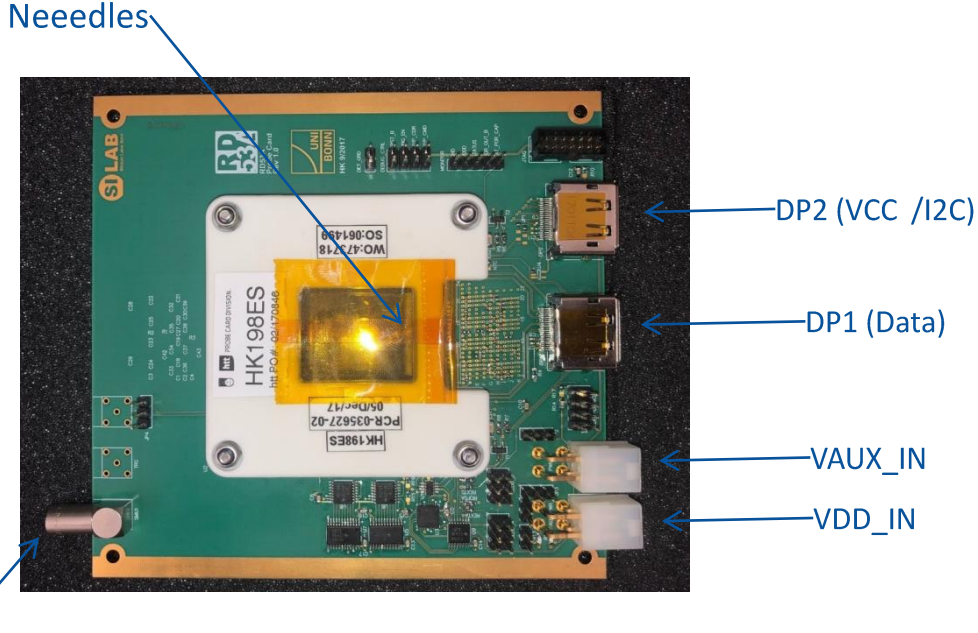
- Probe card connected to BDAQ53 readout system
- Connection to BDAQ53 on one lane at 640 Mbit/s
- BDAQ53 software
- Communication with hardware based on basil
  - Possible to implement / add different devices (Power supplies, SMUs, probe stations) as long as it has some kind of documented interface

PROBE CARD

- Probe card modifications fixed
  - Standard SCC mods: PLL_RESET – POR
  - Two additional transistors to switch between Shunt- and LDO modes

- 11 cards produced, about ready to be distributed
  - 3 for CERN, one already received
  - 2 for Glasgow
  - 2 for Torino
  - 1 for LBNL

- All cards tested, some issues found
  - Broken cards fixed by manufacturer
  - To be tested again



TEST PROCEDURE