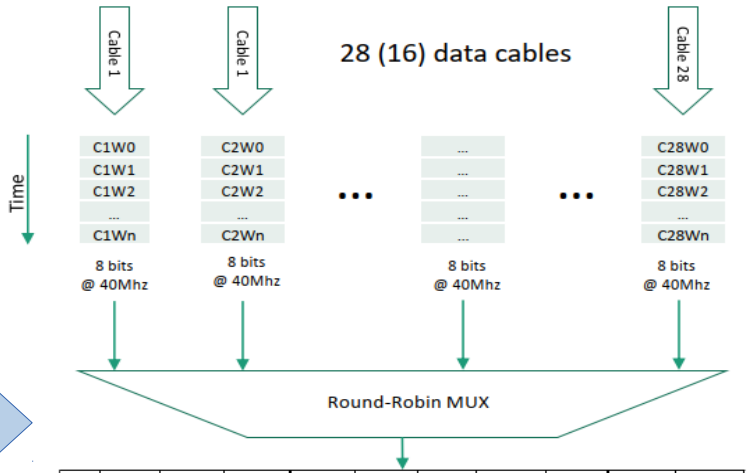
Update on the ITS run3 sim & rec

- **Detector geometry**
  - classical and sagged
- **Simulations:**
  - digitization & cluster topology
- **Reconstruction:**
  - raw-data decoding (encoding)
  - cluster / track finding in DPL
  - fixes in Cooked-Matrix tracker
  - primary vertex reconstruction
- **Quality Control**
- **Event Display**
  - raw data / clusters / tracks
- **Overall status & plans**



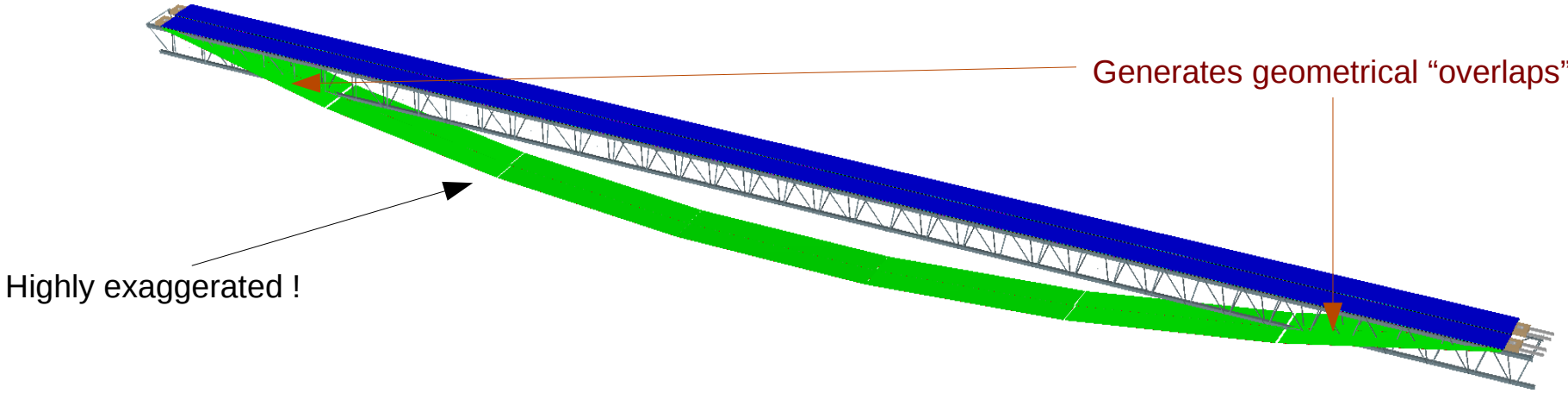
Data Valid	72	64	56	48	40	32	24	16	8	0
0	SOP	Length		TTS Busy			0			
1	0		0	Priority Bit	FEE ID		Block Length		Header Size	Header Version
1	0	HB Orbit					TRG Orbit			
1	0	TRG TYPE				0	HB BC	0	TRG BC	
1	0		0	Pages Counter		STOP BIT	PAR		Detector Field	
1	St1_Id	Status (e.g. busy)								
1	C1_Id	C1W8							C1W1	C1W0
1	C2_Id	C2W8							C2W1	C2W0
1	...	...							...	...
1	C28_Id	C28W8							C28W1	C28W0
1	C1_Id	C1W17							C1W10	C1W9
1	C2_Id	C2W17							C2W10	C2W9
1	...	...								...
1	C28_Id	C28W17							C28W10	C28W9
1	...	...							...	...
1	...	...							...	...
1	C28_Id	C28W(n)							C28W(n-7)	C28W(n-8)
1	St2_ID	Status (e.g. missing data)								
0	EOP	Length		Checksum			End Flag	0		
0	IDLE	0								

Outer Barrel Data Format

Geometry

- Classical
  - **Several important fixes in row / chip / module numberings, local chip coordinate system.**
  - Several little changes in dimensions and positions inside the acceptance
  - No services yet : cables, patch panels.

    Little impact on the physics performance (outside the acceptance).
- Sagged
  - Will be started soon. We do not expect any unrecoverable impact on the tracking.



Digitization and cluster-topology handling

- Configurable parameters for the DPL digitization
  - Continuous / triggered
  - Noise level
  - Threshold
  - Strobe length
  - ...
- Cluster topology decoupled from the availability of MC info
  - COG offset evaluation for “interesting” hits only
  - Dictionary / shape / frequency for all data including noise and QED e’s

Common code with MFT

Raw-data decoding

Processing speed (on single core of **i7-8700k @ 4.3 GHz**)
1000 PbPb MB events at 50kHz + QED with 6µs strobes and 10^{-7} noise
~10^8 fired pixels (30x10^6 clusters) in 13x10^6 non-empty chips
DMA memory allocation rate (with fixed 8KB page size) : **280 GB/s**

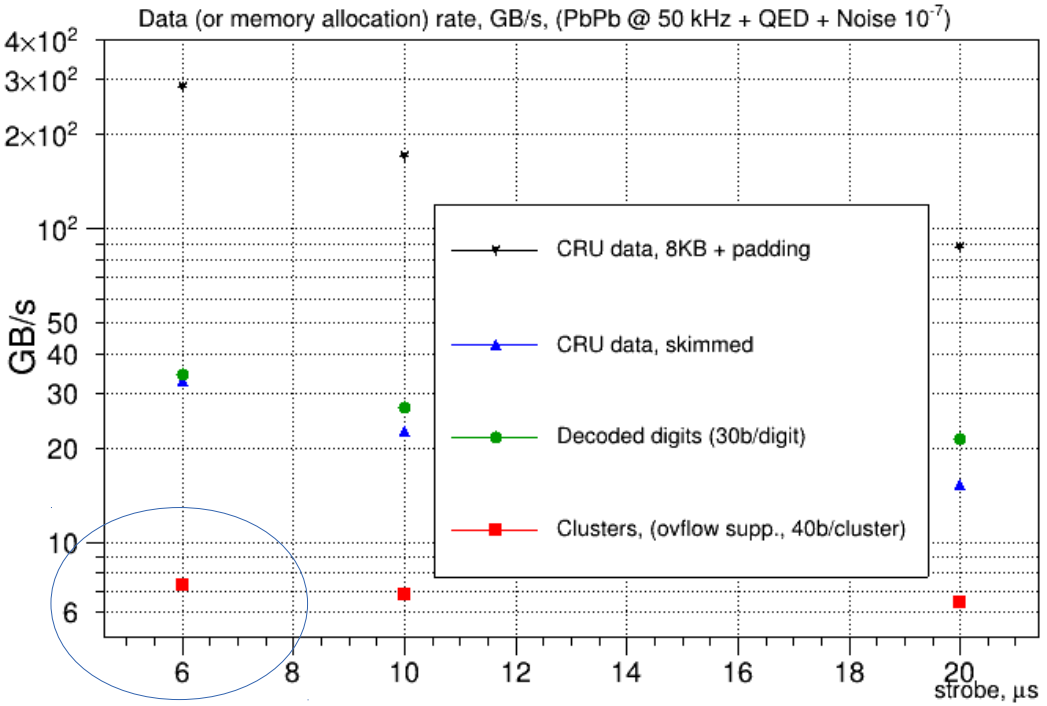
Processing scenarios:

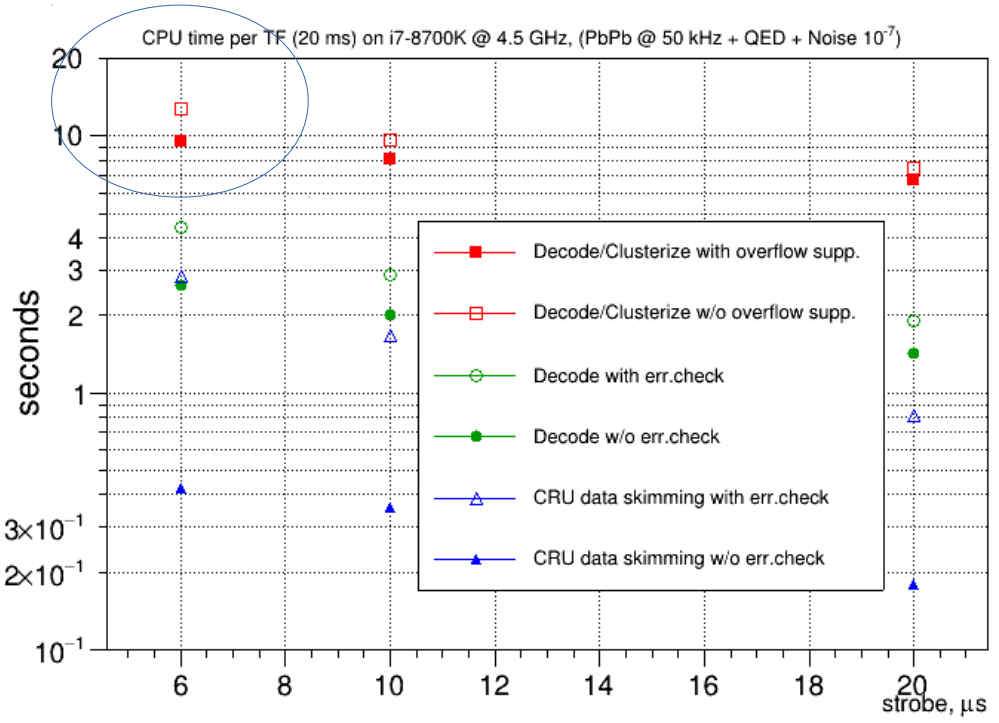
- Clusterization/compactification on FLP → EPN receives compact clusters, ~7 GB/s
- Decoding on FLP → EPN receives hits (row/col, chip, trigger ID), ~25 GB/s
- CRU data skimming on FLP → EPN receives CRU-like data w/o 80b->128b padding and page size corresponding to real payload, ~25 GB/s

	With checking errors In CPU seconds excluding overhead of reading from disk	**W/o checking errors**	**Minimal N Cores for online processing**
Full clusterization (suppressing of overflow pixels)	10.20	8.45	430
Full Decoding	3.20	1.63	82
Removal of 80->120bit padding, skimming to real payload	2.73	0.4	20

Note: this benchmark was done with single CPU core processing input of the whole detector, need to account for the difference in load from different CRUs.

Raw-data handling scenarios

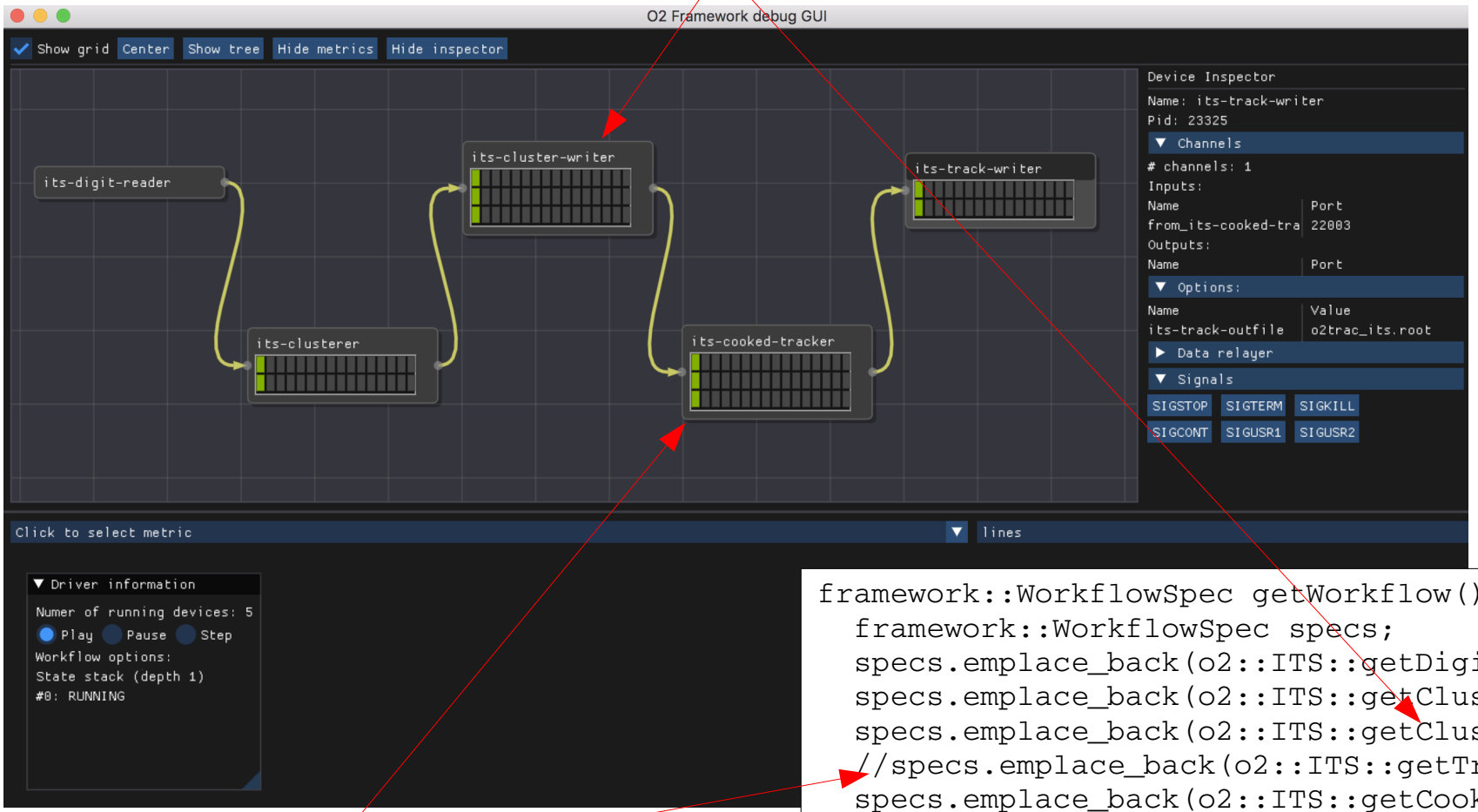




Most likely: The cluster finding will have to be done on EPNs

ITS reconstruction workflow: 6 devices

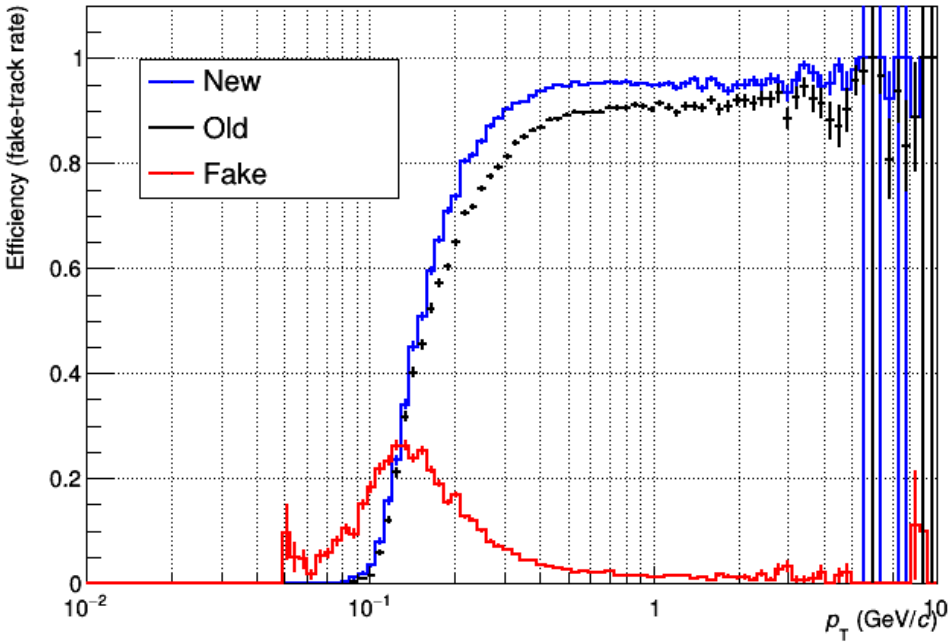
The ClusterWriter needed for the checking macros only (can be commented out)

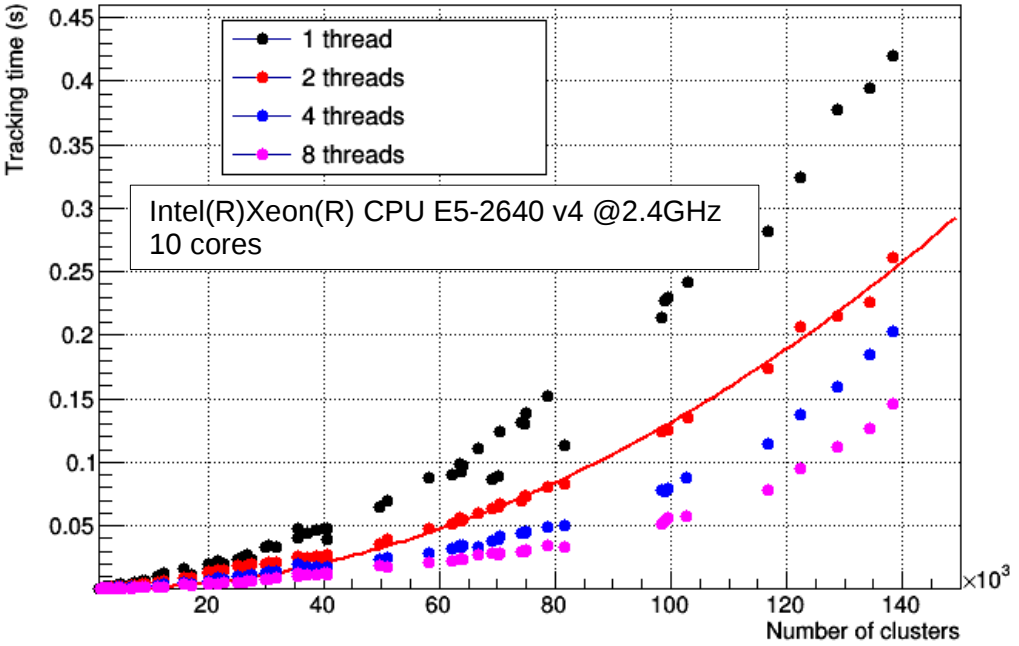



```
framework::WorkflowSpec getWorkflow() {
  framework::WorkflowSpec specs;
  specs.emplace_back(o2::ITS::getDigitReaderSpec());
  specs.emplace_back(o2::ITS::getClustererSpec());
  specs.emplace_back(o2::ITS::getClusterWriterSpec());
  //specs.emplace_back(o2::ITS::getTrackerSpec());
  specs.emplace_back(o2::ITS::getCookedTrackerSpec());
  specs.emplace_back(o2::ITS::getTrackWriterSpec());
  return specs;
}
```

Can as well be a CA tracker “DataProcessor” (inspired by run_trac_ca_its.C)

Fixes in Cooked-Matrix tracker





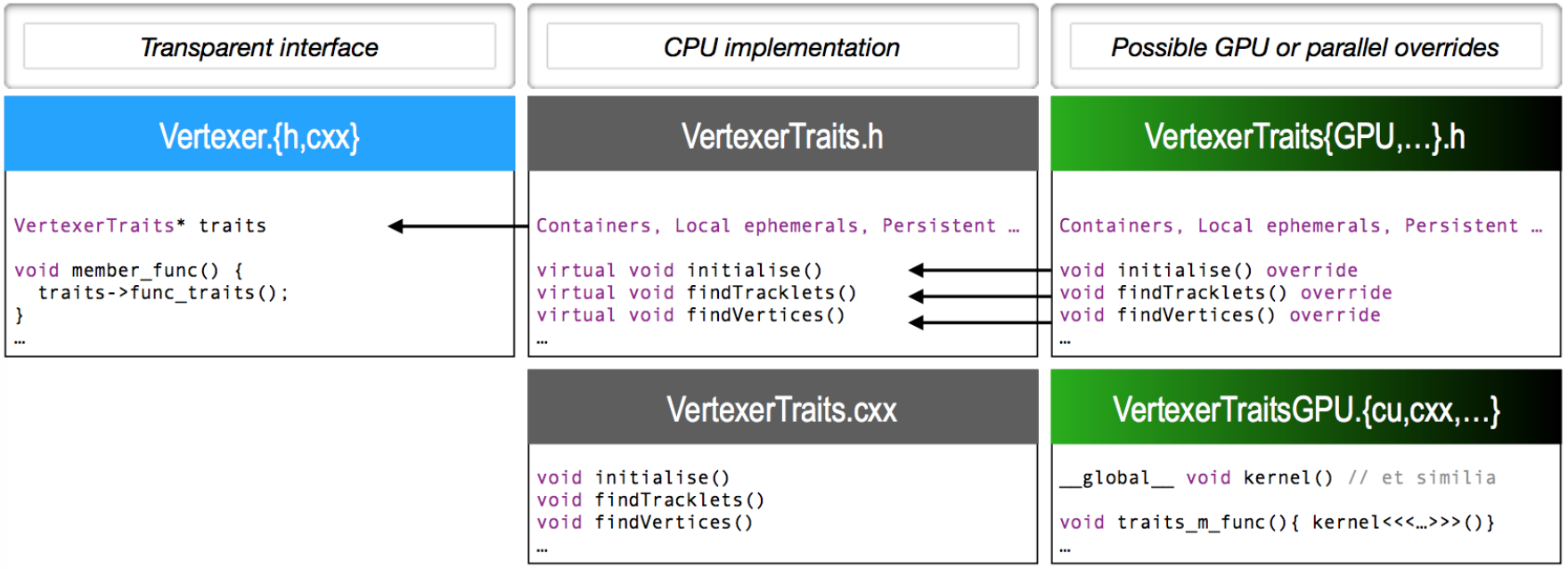
Most peripheral Pb-Pb

Most central Pb-Pb

- The tracking time includes: primary-track finding, track fitting at the innermost layer
- The tracking time does not include: primary-vertex finding, secondary track finding, propagation to the outermost layer

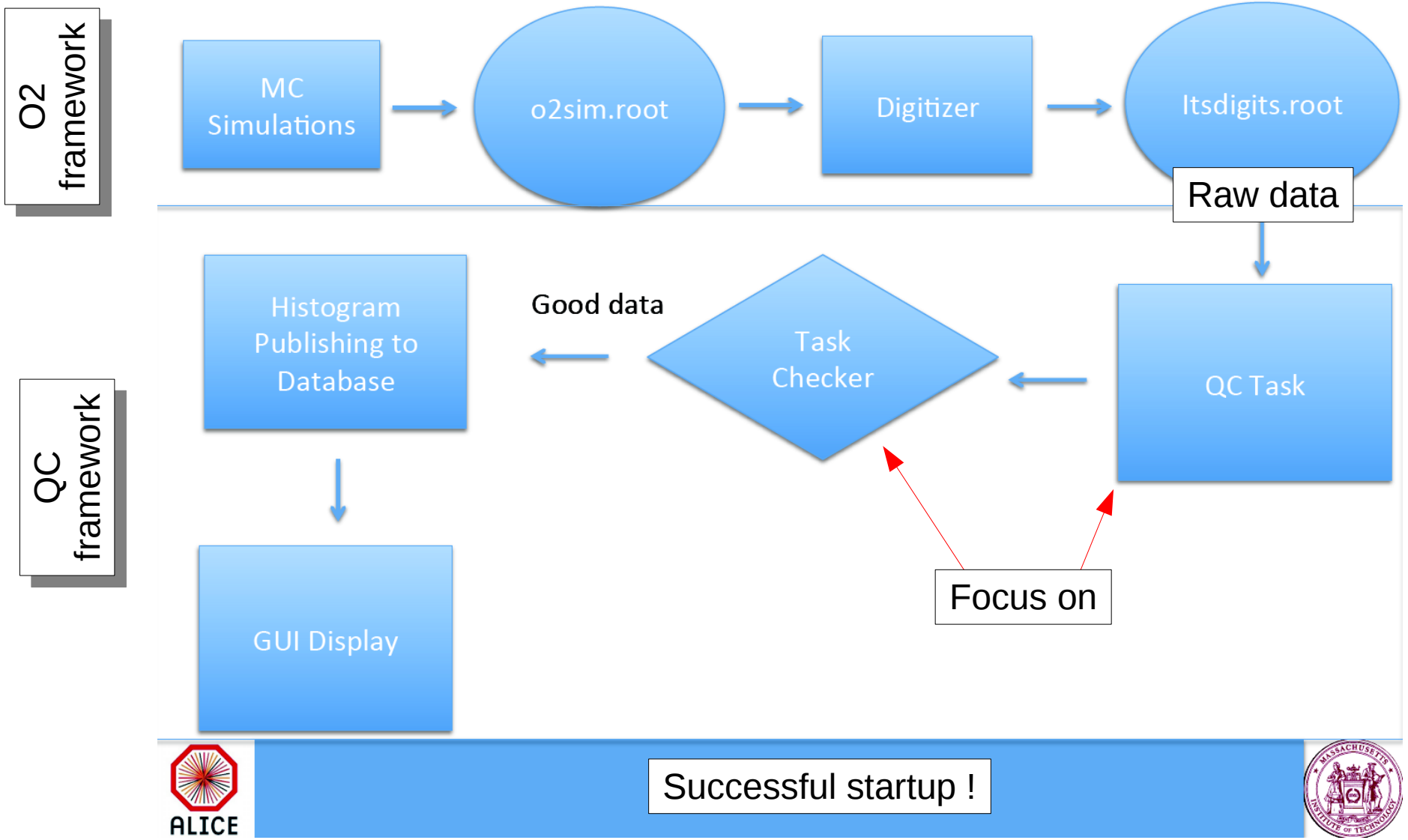
Primary vertex reconstruction

- Transparent and clean `Vertexer` interface
- Streamlined w.r.t. tracker structure ← no *TraitsCPU class (+)
- Inheritance allows for integrating different implementations (overrides)



It works ! But: It is the slowest part of the reco chain. Also: Efficiency vs fake pileup.

Quality Control

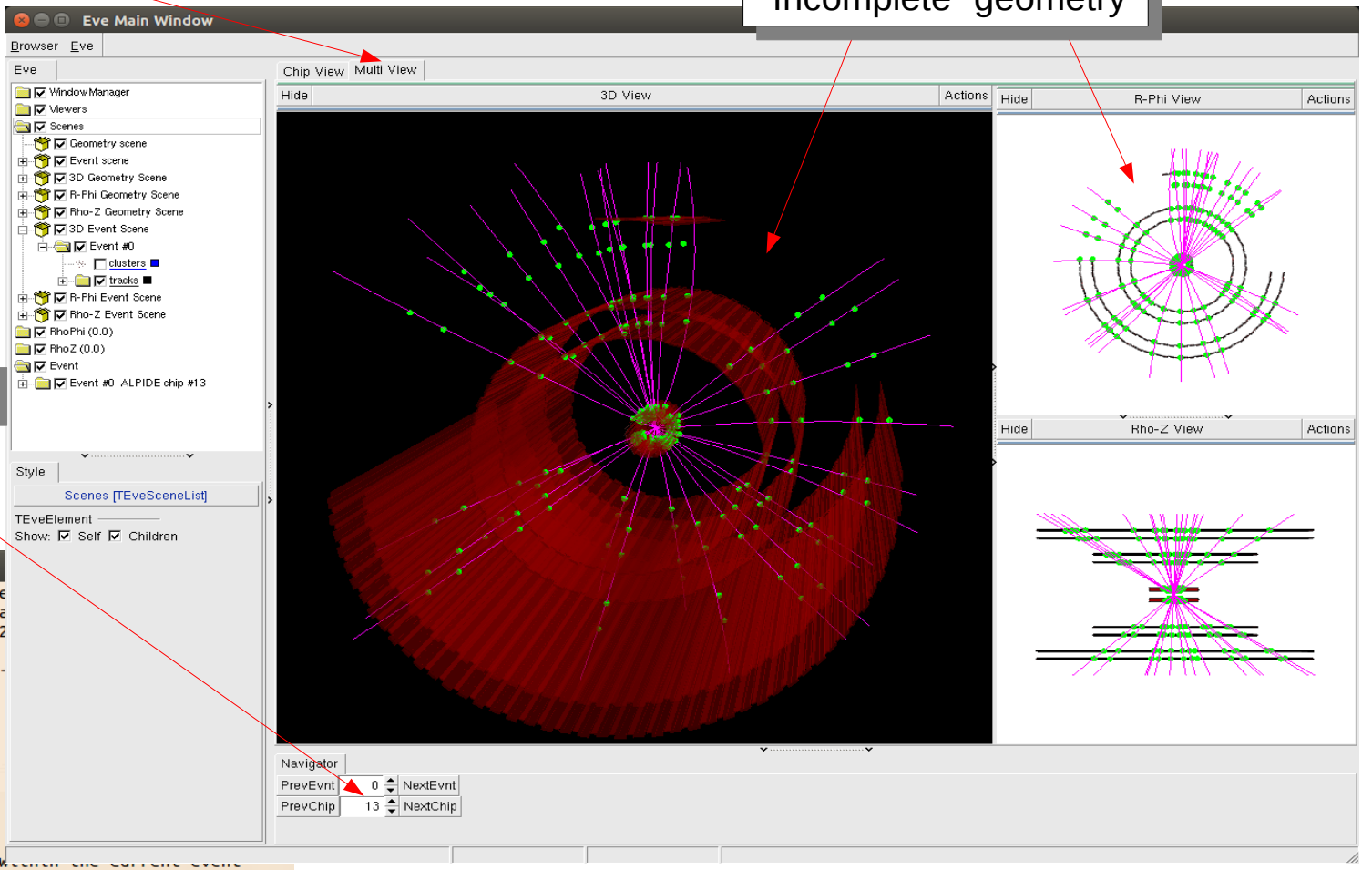


Event display for the commissioning

- **Functionality :**
  - All of ROOT's TEve (rotating, zooming, picking objects with mouse, etc)
  - Reading data from local files (MC digits, raw data, clusters, tracks)
  - **Detector view**
    - Three ALICE projections (3D, r-phi, rho-z)
    - Display of clusters (all, and attached to tracks only)
    - Display of reconstructed tracks
  - **Single-chip view**
    - Zoom down to the pixel level
    - Display of fired pixels
    - Display of reconstructed clusters (bounding box, ...)
  - Navigation over events and chips (command line, and GUI)

Detector view (attached clusters only)

"Incomplete" geometry

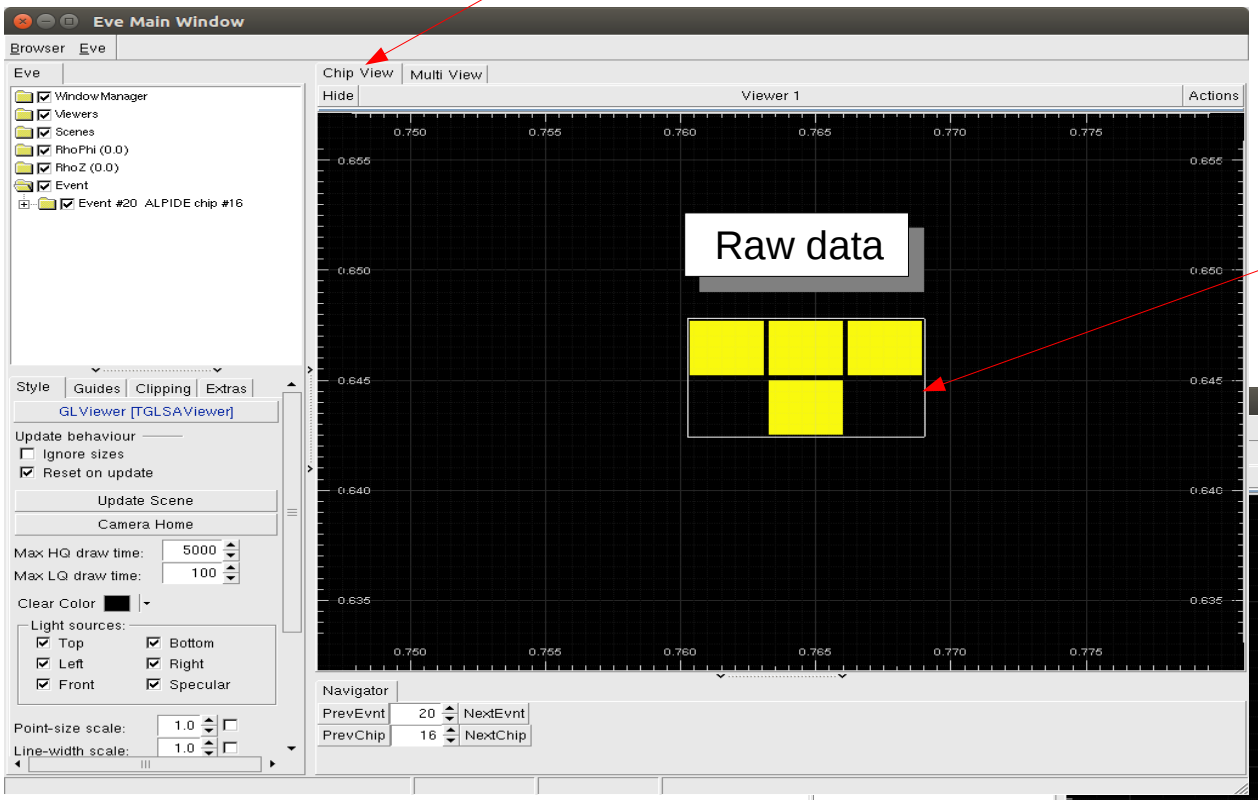


Navigation : events and chips

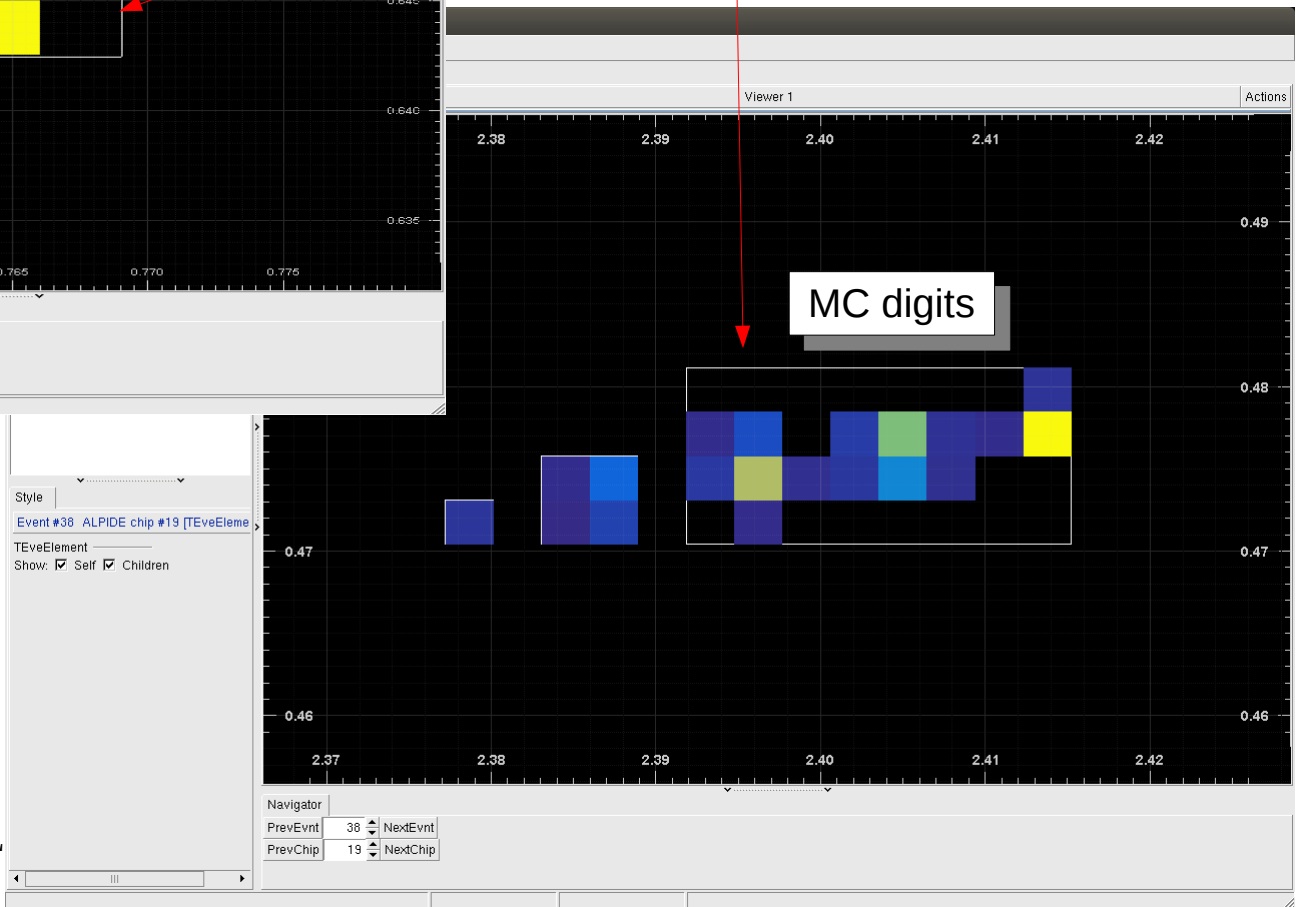
```
Terminal
Info in <TGeoManager::CloseGeometry>: Voxelization re
Info in <TGeoManager::CountLevels>: max level = 8, ma
Info in <TGeoManager::CloseGeometry>: 179073 nodes/ 2
metry
Info in <TGeoManager::CloseGeometry>: ---------------
---
[INFO] Loading ITS L2G matrices from TGeo
[INFO] Loading ITS T2L matrices from TGeo
[INFO] Loading ITS T2G rotation 2D matrices

 **** Navigation over events and chips ****
 load(event, chip)       jump to the specified event
 next()                  load next event
 prev()                  load previous event
 loadChip(chip)          jump to the specified chip within the current event
 nextChip()              load the next chip within the current event
 prevChip()              load the previous chip within the current event

*** Event #0 ***
Number of ITSDigits: 2784
Number of ITSClusters: 1762
Number of ITSTracks: 32
Most occupied chip: 142 (28 digits)
root [0]
```

Information about the displayed event

Single-chip view (digits, clusters)



Cluster bounding boxes



The cluster finder seems to work fine !

Overall status & plans

Task	Contact	People	When	Comments
General ITS geometry	Mario Sitta	Chinorat Kobdaj	Done	No services yet
Sagging geometry	Mario Sitta	Cristina Bedda	Q4 2019	
ALPIDE response simulation	Artem Isakov	Miljenko Suljic	Q2 2019	Vbb=0 missing
Time dependent digitiser	Ruben Shahoyan		Done	
Digitisation in DPL			Done	
Raw data decoder	Ruben Shahoyan		Done	Ongoing discussions with WP10
Cluster finder (CPU)	Iouri Belikov	Ruben Shahoyan	Done	
Time effects in clusterisation	Ruben Shahoyan		Done	
Clusterisation in DPL			Done	
Cluster finder (FPGA)	Anisa Qazi ?		Done ?	Repetitive signal handling in FPGA ?
Cluster-topology handling	Luca Barioglio		Done	Integrated with the Cluster Finder
Primary vertex finder (CPU)	Matteo Concas	Ruben Shahoyan	Done	May need a new approach
Primary vertex finder (GPU)	Matteo Concas	David Rohr	Q2 2019	May take longer
CA tracker (CPU)	Maximiliano Puccio		Done	
CA tracker (GPU)	Maximiliano Puccio	Matteo Concas, David Rohr	Q2 2019	
Tracking in DPL			Done	Without the primary vertexer in DPL
Comparison with Monte Carlo	Arthur Gal	Iouri Belikov	Q4 2019	Service task (~30% of time)
Event display	Iouri Belikov		Done	Needed: Simplified geomety, data convertor
Calibration (noise, dead)	Markus Keil			
Quality Control	Ivan Amos Cali	Zhaozhong Shi	Q2 2020	