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Book of Abstracts

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3D integration of readout chip for the SOI pixel sensors

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SOI is a CMOS LSI technology to insulate each MOSFET by using a thin oxide layer in the silicon wafer, allowing high-performance CMOS circuit because of the low parasitic capacitance. The SOI pixel sensor utilizes the silicon wafer as the radiation sensor. Because of the small detector capacitance and the industry-standard CMOS technology, high-performance pixel sensors can be developed.
In recent high-luminosity collider experiments, huge number of signal and background tracks enter the pixel detector. We have to implement a complex circuit in each pixel to reduce the hits to be read out. There is also demands to keep or reduce the pixel size from the physics view point.
A solution to this issue is the 3D integration of readout chip, where, the additional CMOS chip is produced, integrated to the sensor chip, and the circuit signals are connected pixel by pixel. With this technology, the functions of each pixel can be improved significantly. The first SOI pixel sensor with 3D integration was submitted in 2018 and the evaluation of the chip are in progress.

In this presentation, the 3D integration technology for the pixel sensors is reviewed briefly. Then the R&D status of the SOI 3D pixel sensor will be discussed.

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50 ps timing with SiGe Bi-CMOS monolithic pixel sensors

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The proof-of-concept of a monolithic silicon pixel detector in SiGe Bi-CMOS technology for outstanding tracking and timing performance was produced in the SG13G2 process of IHP Mikroelektronik. Measurements with a 90Sr source show a time resolution of 50ps for hexagonal pixels of 130µm side. The performance of the front-end electronics is compatible with Cadence Spectre simulations and shows the potential of this technology to be used in future tracking detectors with precise 4D measurement capability.

Timing detectors / **2**

A High-Granularity Timing Detector for the Phase-II upgrade of the ATLAS Calorimeter system: detector concept, design, and readout

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The large increase of pile-up interactions is one of the main experimental challenges for the HL-LHC physics program. A powerful new way to mitigate the effects of pile-up is to use high-precision timing information to distinguish between collisions occurring close in space but well-separated in time. A High-Granularity Timing Detector, based on low-gain avalanche detector technology, is proposed for the ATLAS Phase-II upgrade. Covering the pseudo-rapidity region 2.4–4.0, this device will complement the ATLAS Inner Tracker (ITk) in this region. The time resolution per track targeted for a minimum-ionising particle will be 30 ps on average at the start of lifetime, increasing to 50 ps on average at the end of HL-LHC operation. This high-precision timing information will improve track-to-vertex association and object reconstruction in the forward region. In addition, the HGTD offers unique capabilities for the online and offline luminosity determination, an important requirement for precision physics measurements.

An overview of the requirements, specifications, design, and expected performance of the HGTD will be presented. Some key technical challenges will also be discussed, including the front-end electronics and subsequent readout chain.

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A program for fast calculation of capacitances, in planar pixel and strip silicon sensors

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We present a program for fast calculation of capacitances in planar silicon pixel (strip) sensors, based on a 3D (2D) numerical solution of the Laplace equation. A comparison between calculated capacitances and measurements on pixel and strip sensors, along with simulation results obtained with the TCAD Sentaurus suite are presented. The agreement between calculations and measurements better than ~20%, while CPU time for a typical 2 GHz, 4 Core processor is below 5 min for pixel and below 1 min for strip calculations. In addition, our work includes calculations for various configurations of pixel and strip geometries associated with HL-LHC experiments. The program is a useful tool for fast estimation of interstrip, interpixel and backplane capacitances before an embarkation to more sophisticated programs is launched.

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AIDA Innovation Pilot Call

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ALICE ITS: Operational Experience, Performance and Lessons Learned

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ALICE (A Large Ion Collider Experiment) is one of the four main experiments at the CERN LHC. It is dedicated to the study of heavy-ion collisions, to address the physics of strongly-interacting matter at extreme energy densities, where the formation of the quark-gluon plasma (QGP), a deconfined phase of matter, is expected.

During the LHC Run1 and Run2 periods, the innermost detector of ALICE was the Inner Tracking System (ITS), a six-layer silicon vertex detector that provided primary vertex reconstruction as well as secondary vertex reconstruction of heavy-flavour and strange particle decays, particle identification and tracking of low-momentum particles and precise determination of the impact parameter. It was based on three different technologies: moving outward from the beam line, two layers of Silicon Pixel Detector (SPD), two Silicon Drift Detector (SDD) layers and two Silicon Strip Detector (SSD) layers forming the ITS cylinder. In the LHC Run3 period it will be replaced by an upgraded version with seven layers of monolithic pixel detectors.

In this report, the status and performance of the first version of the ALICE ITS detector during Run2 are summarized and the final operational experience and lessons learned to ensure optimum data quality and data taking efficiency are described.

Large detectors / **63**

ATLAS Pixel Detector upgrade at High Luminosity LHC

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In 2025 the Large Hadron Collider will be shut down to allow upgrades to the accelerator and the experiments. After this “Phase-II” shutdown the LHC is expected to reach unprecedented values of instantaneous luminosity, with hundreds of interactions in each bunch crossing. This means much higher data rates and occupancies and increased radiation damage for the experiments. During the Phase-II shutdown the entire ATLAS Inner Detector will be replaced by an all-silicon system called the Inner Tracker (ITk). The innermost part of the ITk will be a state-of-the-art pixel detector comprising about 14 m² of active silicon, which will provide precision tracking capability up to $|\eta|=4$. The outermost layers of the ITk pixel detector are being designed to last the lifetime of the HL-LHC, collecting up to 4000fb-1 of Integrated Luminosity; the innermost layers will be replaced once, after about 2000fb-1.
The ITk pixel detector will be instrumented with new sensors and readout electronics to provide improved tracking performance and radiation hardness compared to the current detector. The sensor type will be dependent upon location in the detector: most of the detector will be populated with thin planar silicon sensors, but 3D-silicon sensors will be used in the innermost layer, due to their higher radiation tolerance and lower power consumption which eases demands on the support structures. The sensors will be read out by new ASICs, based on the one currently being developed by the RD53 Collaboration, which will be thinned to 150μm or less to save material.
Support structures will be made of carbon-based materials, chosen for low mass, high stability and high thermal conductivity. They will be cooled by evaporative carbon dioxide flowing in thin-walled titanium pipes. Servicing the detector reliably within the limited space available, and without introducing excessive amounts of material, is a significant challenge. Data will be transported electrically

inside the detector, on cables carrying 1.28 Gb/s; conversion to optical signals will take place at larger radii where the radiation background is less intense. Serial powering has been chosen as the baseline for the system as it minimises service cable mass. Close attention must be paid to grounding and shielding in the detector to minimise cross-talk and common mode noise.
The ITk pixel detector is currently in the final stages of R&D, with production scheduled to start in 2021.
The speaker will present an overview of all of the above.

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Ageing tests of the Hybrid Modules for the ALICE ITS Upgrade

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The ALICE experiment foresees a comprehensive upgrade during the ongoing long LHC shutdown. A key element is the replacement of the Inner Tracking System (ITS) with a newly constructed silicon based detector. The new "ALPIDE" chips made from Monolithic Active Pixel Sensors (50 μm thick) have already shown excellent performances in terms of power consumption and spatial precision. Once installed in the ALICE detector they will allow a remarkable improvement of the tracking and vertexing capabilities.
Several institutions were involved in the assembly of the modules (HICs, Hybrid Integrated Circuits) of the new ITS. Through a unified procedure, the chips were aligned (with < 5 μm precision) and glued on aluminium based Flexible Printed Circuits (175 μm thick). The aluminium pads of the chips were then bonded to the FPC for power supply and I/O connections. Dedicated hardware and software were developed in order to qualify the modules at different stages after the assembly. Some HICs underwent more invasive tests designed to check their mechanical strength. These include ageing tests: keeping modules in a temperature- and humidity-controlled environment, their ageing in the ALICE cavern can be simulated. The pixel response and the quality of the HICs before and after different ageing periods were measured and compared, drawing conclusions on their stability over time during the data taking period.
In this contribution the HICs qualification procedure will be presented and particular emphasis will be given to the ageing tests. The methods adopted will be described in detail and the collected results will be presented and discussed.

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Assembly and Commissioning of the ALICE ITS Upgrade

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The major upgrade of the Inner Tracking System (ITS) of the ALICE detector is being carried out to meet the challenges of the physics program of the ALICE experiment after the LHC Long Shutdown 2.The strategy of the ALICE ITS upgrade is based on the application of Monolithic Active Pixel Sensors (MAPS) developed by the ALICE collaboration using 0.18 μm TowerJazz technology. These sensors form seven concentric layers resulting in an overall detection area of 10 m^2. The layers of the upgraded ITS are split into the Inner and Outer Barrels.

Currently, the ITS modernization is entering its terminal phase, which means finalization of the production and construction together with the beginning of the on-surface commissioning.

The on-surface commisioning activity is meant to obtain a comprehensive view of the detector performance before installation inside the cavern. It includes the quality control of the main systems and components, namely the tests of the Inner and Outer Barrels, Electronics, Power System, Cooling System as well as detector calibration. Commissioning shifts are ongoing for the detector monitoring running for 24 hours per day. The shift crew is carrying out particularly threshold tests, tests of the noise performance and monitors the key parameters of voltages, currents and temperatures. For the assembled layers cosmic muon data are already being gathered.

The status of the ongoing assembly will be presented together with the first results of the detector performance obtained during the commissioning.

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Beam test measurements of radiation hard monolithic CMOS sensors for the ATLAS experiment at the HL-LHC

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Monolithic Active Pixel Sensor prototypes developed in the TowerJazz 180 nm CMOS imaging process have been designed in the context of the ATLAS upgrade Phase-II at the High-Luminosity LHC. These are characterized by a small collection electrode design (3 um), and a small pixel size (36.4 um), on high resistivity substrates and large voltage bias. The latest prototype of this technology, so-called Mini-MALTA, addresses the pixel in-efficiencies observed in previous designs to meet the radiation hardness requirements. This contribution will highlight recent results from characterization of the sensors in particle beam tests, where full efficiency up to 1E15 neq/cm2 and 70 Mrad is observed.

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Belle II Pixel Detector Commissioning and Operational Experience

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The Belle 2 experiment at the super flavour factory SuperKEKB in Tsukuba, Japan, has started regular operation with its final detector setup in spring 2019. The Belle 2 vertexing system consists of four layers of double sided silicon strips (SVD) and two layers of DEPFET pixel sensors (PXD). These inner most pixel layers are arranged at radii of 14mm and 22mm around the beam pipe. The sensors with pixel sizes down to 50um times 55um are thinned down to 75um thickness to minimize multiple scattering. They are most crucial for reconstructing the secondary decay vertices of short lived B and D mesons with a precision of better than 15 microns. The high luminosity and harsh background conditions impose challenges on the operation of the detector close to the interaction point.

In this talk, we will review the commissioning and operation experience during the first months of data taking, including performance figures of first data.

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Belle II Vertex Detector Performance

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The Belle II experiment at the SuperKEKB accelerator (KEK, Tsukuba, Japan) collected the first physics data in the spring 2019. With the aim to
accumulate 50 times larger data sample from electron-positron collisions than the previous generation of B-Factories, both the collider and detector
are facing substantial challenges, requiring not only state-of-the art hardware, but also modern software methods from track finding algorithms to alignment.
The broad physics program and namely precision measurements in the field of time-dependent CP-violation, require excellent performance
of the detector and in particular its vertexing device, designed as two layers of DEPFET pixels and four layers of double sided strip sensors.
In this contribution, an overview of the vertex detector of Belle II, our methods to ensure its high performance and the first results and experiences from the first physics run will be presented.

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CMS Inner Tracker Upgrade

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The LHC is preparing an upgrade, which will bring the luminosity of the machine to 5-7 × 10^34cm^−2s^−1 reaching an integraded luminosity of 3000 by the end of 2037. This High Luminosity LHC scenario, HL-LHC, will require extensive upgrades to the experiments to fully exploit the physics potential of the accelerator. In this so-called Phase-2 upgrade, CMS detector will require improved radiation hardness, higher detector granularity to reduce occupancy, increased bandwidth to accommodate higher data rates, and an improved trigger capability in order to maintain an acceptable trigger rate. Thus, the entire tracking system will need to be replaced to deal with the HL-LHC environment and to maintain the excellent performance of the current CMS detector.

The Phase-2 Inner Tracker (IT) is designed to maintain or even improve the tracking and vertexing capabilities under the high pileup (140 - 200 collisions per bunch crossing) conditions of the HL-LHC. The detectors should have the required radiation tolerance and capability of delivering the desired performance in terms of detector resolution, occupancy, and track separation. IT will be built from thin silicon pixel detectors segmented into pixel sizes of 25 x 100 μm2 or 50 x 50 μm2. IT is composed of a barrel part with four cylindrical layers and eight small and four large disc-like structures in each forward direction. The design also includes the possibility to extract and replace the degraded parts of the detector without removing the beam pipe. The Tracker Endcap Pixel detector (TEPX), installed within the extended space, will enable the measurement of real-time instantaneous luminosity as an added functionality. The extended geometrical coverage of up to η < 4.0 provides large forward acceptance to mitigate the pileup especially in the endcap calorimeters.

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CMS Inner Tracker: Operational Experience, Performance and Lessons Learned

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The CMS Phase-1 Pixel Detector was designed to cope with an instantaneous luminosity 2e34 cm-2 s-1 and 25 ns bunch spacing with very small efficiency loss. The upgraded detector has one additional hit coverage featuring 4 barrel layers and 3 endcap disks, almost doubling the pixel count to 124M. DCDC converters were used to deliver more power to the detector without the need of replacing the cable plant. CO2 based cooling was implemented and carbon based structures were used to reduce material in the tracking volume. The data acquisition (DAQ) system was upgraded to accept higher event rates and a new, digital data format from the detector front ends. The detector was installed in early 2017 and has been successfully operated since. The LHC is now going through a planned long shutdown period during 2019-2020. The pixel detector was extracted in early 2019 after the end of Run-2 data taking and has been kept cold to protect the silicon sensors. The innermost barrel layer will be replaced during this shutdown period and will feature improved ASICs and circuit boards to rectify issues discovered during data taking. This talk will focus on the operational experience of the detector in 2018, highlighting the detector performance and addressing the lessons learned. The current status of the detector and the refurbishment plan will also be discussed.

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CMS Outer Tracker Upgrade

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The LHC machine is planning an upgrade program which will smoothly bring the luminosity to about $5-7.5\times10^{34}\text{cm}^{-2}\text{s}^{-1}$ in 2028, to possibly reach an integrated luminosity of $3000-4500$ fb^{-1} by the end of 2039. This High Luminosity LHC scenario, HL-LHC, will require an upgrade program of the LHC detectors known as Phase-2 upgrade. The current CMS Outer Tracker, already running beyond design specifications, and CMS Phase-1 Pixel Detector will not be able to survive HL-LHC radiation conditions and CMS will need completely new devices, in order to fully exploit the highly demanding conditions and the delivered luminosity.

The Phase-2 Outer Tracker (OT) is designed in order to ensure at least the same performances of the Phase-1, in terms of tracking and vertexing capabilities, at the high pileup (100-200 collisions per bunch crossing) expected at HL-LHC. The Phase-2 OT will have higher radition tollerance, granularity and track separation power with respect to the Phase-1. Moreover the Phase-2 OT will have also trigger capabilities since tracking information will be used at L1 trigger stage. In order to achieve such capabilities Phase-2 OT should be able to perform a data reduction directly on front end electronics. This has been implemented through the p_T discriminating module concept, each OT module will be composed by two silicon sensors, with a small spacing, read out by a single ASIC which correlates data from both sensors selecting tracker "stubs". These stubs will then be used to perform the tracking for L1 trigger.

This report is focusing on the replacement of the CMS Outer Tracker system, describing new layout and technological choices together with some highlights of research and development activities.

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CMS Outer Tracker: Operational Experience, Performance and Lessons Learned

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The CMS Tracker consists of two tracking devices utilizing advanced silicon technology: the inner tracker with pixel detectors and the outer tracker composed of strip detectors. The outer tracker with its more than 15000 silicon modules and 200m2 of active silicon area is in its tenth year of operation at the LHC. We present the performance of the detector in the LHC Run 2 data taking. Results for signal-to-noise, hit efficiency and single hit resolution will be presented. We review the behavior of the system when running at beyond-design instantaneous luminosity and describe challenges observed under these conditions. The evolution of detector parameters under the LHC conditions will also be discussed.

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CMS Phase-1 Pixel Detector: Layer 1 Issues and Solutions

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The first CMS pixel detector performed very well. Nevertheless it showed inefficiencies at high data rates when operated at luminosities above the planned LHC value of 10^34. Therefore it was decided to replace it with an improved version, the so called "phase-1" detector. It was constructed in 2013-2016 and installed in early 2017, during the LHC extended winter shutdown. The overall performance of the detector has been good and it delivered high quality data in the 2017-18 period. However some problem appeared, especially during the initial running period.
This talk will present the problems encountered and the ways in which they were resolved. It will explain how changes in the detector operation minimized the negative impact caused by these problems.

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Cobalt-60 gamma irradiation of silicon test structures for high-luminosity collider experiments

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During the era of the High-Luminosity (HL) LHC the experimental devices will be subjected to enhanced radiation levels with fluxes of neutrons and charge hadrons in the inner detectors up to ~2.3x1016 neq/cm2 and total ionization doses up to ~1.2 Grad. A systematic program of radiation tests with neutrons and charge hadrons is being run by the CMS and ATLAS collaborations in view of the upgrade of the experiments, in order to cope with the higher luminosity of HL-LHC and the associated increase in pile-up events and radiation fluxes. In this work we present results from complementary radiation studies with gamma photon with a 60Co source in which the doses are equivalent to those that the outer layers of the silicon tracker systems of the two experiments will be subjected. CV and IV measurements are complemented by time-resolved current transient measurements will be subjected. The devices under test are p-type diodes and MOS capacitors.

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DAQ and Level-1 Track Finding for the CMS HL-LHC Upgrade

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The LHC will be upgraded to the High Luminosity (HL-LHC) in the late 2020 in order to reach an instantaneous luminosity as high as $7x10^{34}cm^{-2}s^{-1}$, hence increasing the discovery potential of the machine. In order to preserve its physics reach, the CMS detector will be significantly upgraded. A key component of the upgrade is the Outer Tracker detector that will be able to identify tracks with transverse momentum above ~2 GeV/c and provide them to the Level-1 trigger algorithm, thus maintaining manageable trigger rates and good performance. One of the main challenges of the Level-1 track finding is being able to reconstruct charged particles trajectories from a 40 MHz collision rate with a few microsecond latency budget. Dedicated FPGA hardware systems have been developed for track finding to address this challenge. Another stringent requirement on the Tracker DAQ system is set by the unprecedented number of channels, reaching 2 billions for the Inner Tracker only. To handle this, the Tracker DAQ back-end boards will be equipped with commercial CPUs that will guarantee the system scalability and ensure an effective monitoring of the detector conditions. The DAQ proposal to handle this distributed computational power as well as the design choices of the Level 1 track finding will be presented.

Sensor/ASICs technology / **28**

Depleted Monolithic Active Pixel Sensors in the LFoundry 150 nm and TowerJazz 180 nm CMOS technologies

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The key ingredient to enhance the radiation tolerance and timing precision for CMOS pixel sensors is to achieve a fully depleted sensitive layer, where the charge collection is guided by strong drifting field. Such sensor concepts have been progressively demonstrated by recent R&D achievements with monolithic prototypes in large formats. These sensors are often referred to as DMAPS (Depleted Monolithic Active Pixel Sensor), and this talk will summarize the DMAPS development in LFoundry 150 nm and TowerJazz 150 nm CMOS processes.

The development of DMAPS in LFoundry 150 nm CMOS technology makes use of a so-called large electrode design to achieve a depleted sensitive layer by combining high resistive substrate (> 2 kΩ·cm) as sensitive layer and high bias voltage (> 200 V). The implemented sensor structure mimics the standard planar sensor, and it incorporates a large-area implant as the collection node, thus is an intrinsically radiation-hard structure with uniform drifting field. The in-pixel electronics is integrated in the collection well thanks to the multiple nested wells offered by the foundry. The TowerJazz development line uses a small collection diode, and the resulting sensor capacitance can be as small as ~ 5 fF, a value typically an order of magnitude smaller than that in the large electrode design case. A major benefit of small sensor capacitance is the possibility to employ an ultra-low power analog front-end design (~ 1 μW/pixel), maintaining at the same time good noise, threshold and timing performances. In order to achieve a fully depleted sensitive layer, together with enhanced lateral collection field, dedicated process modifications are needed in such small electrode designs.

This talk will mostly focus on the two large scale demonstrator chips fabricated in the aforementioned two technologies, named LF-Monopix and TJ-Monopix. They both have the same column based, synchronous readout architecture, which is similar to the one implemented in the current ATLAS pixel detector (FE-I3). The design and characterization results, both in lab and in beam, will be presented. Issues for the current designs and fixes planned for the future will be discussed. Submission plans for the next-generation chips, i.e. LF-Monopix2 and TJ-Monopix2, will also be given.

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Design of a Segmented LGAD Sensor for Development of 4-D Tracking Detector

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The tracking detector capable of recording the hit-time information in a precision of O(10ps) should become a breakthrough device in future hadron collider experiments to resolve signal tracks in the harsh environment with enormous background tracks. LGAD (low-gain avalanche detector) is one of such candidates, which is expected to provide fine spatial resolution at the same time; hence to realize a 4-D tracking detector. We have fabricated LGAD diodes and segmented strip-type detectors at Hamamatsu Photonics. The performance other than the timing resolution has been reported elsewhere [1]. Recently the pad type detectors were tested in a proton beam and we obtained a time resolution better than 30 ps for the devices with 50 μm active thickness. The gain non uniformity across the strip [1] was modeled in a TCAD simulation, which was then used to design segmented LGAD sensors with uniform gain. The study suggests that uniform LGAD sensors can be made maintaining a wider operation bias voltage range. We report the test beam and the TCAD simulation results.

Timing detectors / 30

Design of the CMS MTD Endcap Timing Layer

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The MIP Timing Detector (MTD) of the Compact Muon Solenoid (CMS) with hermetic coverage up to a pseudo-rapidity of |η|=3 is designed to provide precision timing information (with resolution of ~40 ps per layer) for charged particles. This upgrade will reduce the effects of pile-up expected under the High Luminosity LHC running conditions and brings new and unique capabilities to the CMS detector. The time information assigned to each track will enable the use of 4D reconstruction algorithms and will further discriminate in the time domain interaction vertices within the same bunch crossing to recover the track purity of vertices in current LHC conditions. The endcap region of the MTD, called the Endcap Timing Layer (ETL) will be instrumented with silicon-based low gain avalanche detectors (LGADs), covering the high radiation pseudo-rapidity region between |η|=1.6 and 3.0. Each endcap will be instrumented with a two-disk system of LGADs, read out by Endcap Timing Readout Chips (ETROCs), being designed for precision timing measurements. We present the status of the R&D for the MTD ETL and report on recent test beam results.

Sensor/ASICs technology / 5

Development of the radiation hard high-speed monolithic CMOS sensors for the ATLAS experiment at the HL-LHC

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The upgrade of the ATLAS tracking detector for the High-Luminosity Large Hadron Collider at CERN requires the development of novel radiation hard silicon sensor technologies.
The MALTA Monolithic Active Pixel Sensor prototypes have been developed with the 180 nm TowerJazz CMOS imaging technology. This combines the engineering of high-resistivity substrates with

on-chip high-voltage biasing to achieve a large depleted active sensor volumes, to meet the radiation hardness requirements of the outer barrel layers of the ATLAS ITK Pixel detector (1.5E15 1 MeV neq/cm2). MALTA combines low noise (ENC < 20 e) and low power operation (1 uW / pixel) with a fast signal response (25 ns bunch crossing) in small pixel size (36.4 x 36.4 um2), and a small collection electrode (3 um), with a novel high-speed asynchronous readout architecture to cope with the high hit rates expected at HL-LHC.
The latest developments, embedded in so-called Mini-MALTA chip, address the issues observed in previous designs to meet the desired radiation hardness requirements. This contribution will summarize the design and recent improvements of this technology, together with the measurements of analog and digital performance, as obtained in lab tests and radioactive source tests.

Excursion to Dubrovnik / **74**

Free time (dinner in local restaurants)

Excursion to Dubrovnik / **72**

Free time (museums, visit to city walls, etc.)

Excursion to Dubrovnik / **73**

Guided tours

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High performance 4D tracking with 100% fill-factor and very fine pitch silicon detectors

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In our contribution we present the performance of RSD (Resistive AC-Coupled Silicon Detectors), an evolution of the LGAD (Low-Gain Avalanche Diode) technology, developed through a collaboration between the Torino division of INFN (the Italian National Institute for Nuclear Physics) and Fondazione Bruno Kessler (FBK), Trento. In this new design, the multiplied charges are slowed down on the detector surface by a resistive n^+ implant and then they induce a signal on the readout metal pads thanks to a dielectric layer, acting as a coupling capacitor. Having a continuous p-gain implant over the whole detector area, the RSD technology gets rid of all the isolation structures used to produce standard pixelated trackers by simply transferring the segmentation from the multiplication layer to the readout scheme, given by the AC-pad size and pitch. By properly designing such scheme, we achieved the challenging goal of producing detectors for 4D tracking with very high spatial granularity (up to 50 μm pitch) and 100% fill-factor while maintaining good timing performances proper of LGAD-based devices (few tens of ps). After reviewing the RSD paradigm and presenting

the first batch of sensors fabricated by FBK, we will show several characterizations before and after irradiation.

Sensor/ASICs technology / 3

High-Granularity Timing Detector for the Phase-II upgrade of the ATLAS Calorimeter system: Low-Gain Avalanche Diode silicon sensors and characterization in test beam

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Abstract: The large increase of pile-up interactions is one of the main experimental challenges for the HL-LHC physics program. A powerful new way to mitigate the effects of pile-up is to use high-precision timing information to distinguish between collisions occurring close in space but well-separated in time. A High-Granularity Timing Detector (HGTD) , based on low-gain avalanche detector (LGAD) technology, is proposed for the ATLAS Phase-II upgrade.LGAD is innovative silicon sensors optimised for timing measurements based on the Low-Gain Avalanche Diode design. Using this technology, the time resolution per track for a minimum-ionising particle can reach 50 ps on average at the end of HL-LHC operation. LGAD also attracted for fast response for realizing a 4D tracker in future experiment and for possible other applications.

This talk will show beam test results and measurements of irradiated LGAD sensors, such as timing resolution, efficiency and collected charge. It will also cover a variety of strategies to improve its radiation hardness.

Sensor/ASICs technology / 14

Hybridization of the Planar Pixel Modules for ATLAS ITK upgrade

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In the development of pixel detectors for the HL-LHC ATLAS Inner Tracking Detector upgrade (ITk), thin and finer granularity pitch planar pixel detector has been developed by HPK/KEK and is ready for the production. The hybridization optimization was started using the FE-I4 ASIC (250um x 50um pitch) for the current ATLAS pixel detector. Recently a half size but final pitch readout ASIC, RD53A (50um x 50um pitch), which is supposed to be the last prototype before the pre-production chip, became available and the modules with this ASICs have been tested in testbeam before and after irradiation.
In this presentation, I will summarize the progress in the HPK/KEK hybridization development using sensor UBM and Sn/Ag solder bumps and related sensor development targeting to implement on-pixel biasing structures. The sensor module producton plan is also covered.

Timing detectors / **42**

LGAD and 3D as timing detectors

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In view of the High Luminosity upgrade of the CERN Large Hadron Collider (HL-LHC), radiation tolerant silicon sensors are being developed in the framework of ATLAS, CMS, RD50 and other sensor R&D projects. The HL-LHC beam parameters and hardware configuration should enable the collider to reach a peak instantaneous luminosity of 5×10^{34} cm^{-2}s^{-1}, and an integrated luminosity (total collisions created) of 250 fb^{-1}/year with the goal of 3000 fb^{-1} after about 12 years of operation. This will imply a factor 5 increase in instantaneous luminosity, and 10 in integrated luminosity with respect to the LHC. This increase in luminosity will also imply a factor 4 rise in the expected pile-up with respect to that observed during Run 2 of the LHC in ATLAS and CMS. Lastly, at the end of the operation period, radiation levels are expected to reach values above 1.6×10^{16} fast hadrons/cm^2 at the innermost detectors.

To cope with the increase in pile-up, silicon sensors with timing capabilities of the order of ~ 10 ps are being developed. Given the expected radiation levels, the radiation-tolerance of these devices is of the utmost importance. In order to tackle these issues, one line of research investigates the possibility of producing radiation tolerant silicon sensors with intrinsic charge gain: Low Gain Avalanche Detectors (LGADs). The aim is to improve the signal height after irradiation as well as the timing capabilities of silicon sensors. Another approach is the use of 3D sensors. The implementation of 3D devices would resolve some of the issues arising from using LGADs such as gain-loss, radiation hardness at fluences beyond 10^{15}cm^{-2}, or a reduced fill factor.

The aim of this presentation is to give an overview of both technologies, their performance, and their current development status for timing applications.

Large detectors / **64**

LHCb VELO and Silicon Tracker: Operational experience, performance and lessons learned

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The Large Hadron Collider Beauty (LHCb) detector is a single-arm forward spectrometer, designed to detect decays of beauty and charm hadrons. High-precision track and vertex reconstruction in regions with the highest particle occupancies are enabled by a set of silicon-strip detectors: the VErtex LOcator (VELO) surrounding the interaction region, a large-area Tracker Turicensis (TT) located upstream of the LHCb dipole magnet, and the Inner Tracker (IT) placed around the beam pipe in the three tracking stations downstream of the magnet.
These detectors have successfully operated for the last 10 years, maintaining a high data-taking efficiency even with the reduced bunch separation and higher particle multiplicities of the LHC Run 2 environment. The cumulative radiation damage poses challenges in reaching full depletion in the most irradiated zones of the detectors, which have highly non-uniform exposure, with fluences of $0.01 - 4 \times 10^{14}$ 1 MeV-n$_{eq}$ cm^{-2} in the same sensor. Radiation damage in the detectors is monitored using multiple methods, including measurements of bias current versus voltage and temperature, and periodic charge collection efficiency (CCE) scans. This talk will summarise the operational experience and performance of the detectors from 2010-2018. In particular, a recent

analysis of the correlation of cluster finding efficiency with the distance of the silicon strip to a second metal layer routing line in the VELO and comparisons with 2D and 3D TCAD simulations will be presented.

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Low dose rate 60Co facility in Zagreb

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The Co-60 irradiation facility at the Ruder Boskovic Institute in Zagreb will be presented. Preliminary results of the irradiation of an ATLAS and CMS pixel detector prototype readout chip, called RD53A, will be discussed.
Recent results have shown evidence of enhanced low dose-rate radiation sensitivity (ELDRS) to the total ionizing dose (TID) induced damage in 130- and 65-nm CMOS technologies. ELDRS has serious implications on the design of electronic circuits for High Luminosity Large Hadron Collider (HL-LHC) considering radiation hardness, where characterization and performance assessment are normally done with much higher dose-rates than foreseen during the operation. The Co-60 irradiation facility is equipped with a setup for irradiation at dose-rates similar to those at HL-LHC, close to the interaction point. Radiation hardness studies performed with this facility will therefore be a great complement to the ones performed at high-dose rates. The experimental setup is composed of two styrofoam boxes, a chiller, dry air system, a few power supplies and PCs. The setup is currently used to irradiate six RD53A chips. Three of them at room temperature and three of them cooled.

Vertex detector subsystems / **32**

Mechanics & Cooling Challenges for the ATLAS ITk Upgrade for HL-LHC

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In a continuous effort to push the energy frontier, CERN's Large Hadron Collider (LHC) will undergo a major upgrade which will extend its service life and boost the potential for new discoveries beyond 2025. Along with a ten-fold increase in the rate of collisions, the High Luminosity LHC (HL-LHC) is expected to reach unprecedented levels of radiation. In parallel, in the ATLAS experiment an all-silicon tracker capable of coping with the demands of the new collider will replace the current Inner Detector.

The future ATLAS Inner Tracker (ITk) will comprise a Strip Tracker and a Pixel Detector. The construction of both systems will make extensive use of advanced materials and lightweight technologies in order to meet the stringent material budget, thermal performance and stability requirements. However, the ambitious performance targets set for the ITk, the harsh HL-LHC environment and the severe space constraints will give rise to a series of new engineering challenges, the answer to

which calls for innovative approaches in the design of the support structures, the cooling strategy and the overall integration scheme.

This talk will review the mechanical design of the ATLAS ITk, focusing on the solutions developed for the support and thermal management of the silicon sensors and readout electronics. The ongoing prototyping activities for these elements will also be discussed.

Vertex detector subsystems / **67**

Microchannel cooling for the LHCb VELO pixel upgrade

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The LHCb Vertex Detector (VELO) is currently being upgraded to a lightweight, capable pixel detector of 40 MHz. The thermal management of the system will be provided by evaporative CO2 circulating in micro channels. This solution has been selected because of the excellent thermal efficiency, the absence of thermal expansion, as well as the ability of CO2 and the contribution to the material budget.

Although micro channel cooling is gaining considerable attention for applications related to microelectronics, it is still a novel technology for particle physics experiments, especially when combined with evaporative CO2 cooling. The LHCb design focusses on an efficient layout of the channels with a fluidic connector and its attachment. The distribution of the coolant is ensured by the use of restrictions implemented before the race.

The microchannel production is a complex process involving the production of quality control and the production of the process. The quality control includes a cyclic stress test in pressure and temperature, high pressure tests with helium, and surface evaluation. The microchannel production is now underway and will be described along with future R & D improvements that could be envisaged.

Future facilities/experiments / **62**

Monolithic fully-depleted CMOS sensors for frontier vertex and silicon detectors

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The exploitation of the physics reach at the next generation electron-positron colliders requires outstanding flavour tagging performance, impacting on the vertex detector characteristics:
- state-of-the-art granularity for resolutions at the few micron level shall be guaranteed while preserving a high event rate capability;
- minimum multiple scattering at the innermost radius calls for a material budget at the level of 0.15% X0 per layer;
- “compact” detectors requires advanced integration and packaging technologies, innovative cooling and assembly solutions.

Monolithic active pixel silicon detectors will expectedly play a major role. At the moment, no architecture nor technology exists fulfilling all of the requirements. However, several solutions are being

explored, capitalizing on the experience of the first large area, high performance vertex detectors under construction or commissioning.

The talk will discuss possible options on silicon sensors and associated electronics for future vertex detectors, with a view on the use of this technology also for large area trackers. As exemplary illustration, I will present the status and outlook of the INFN project on the design of fully-depleted CMOS monolithic sensors.

Sensor/ASICs technology / **41**

MuPix & ATLASpix: Architectures and Results

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High Voltage Monolithic Active Pixel Sensors (HVMAPS) are based on a commercial High Voltage CMOS process and collect charge by drift inside a reversely biased diode. HVMAPS represent a promising technology for future pixel tracking detectors.

Two recent developments are presented. The Mupix has a continuous readout and was developed for the Mu3e experiment whereas the ATLASpix has a triggered readout and was developed for ATLAS. Both variants have a fully monolithic design including state machines, clock circuits and serial drivers. Several prototypes and design variants were characterized in the lab and in testbeam campaigns to measure efficiencies, noise, time resolution and radiation tolerance.
Results from recent Mupix and ATLASpix prototypes are presented and prospects for future improvements are discussed.

Vertex detector subsystems / **23**

MuPix chips, mechanics and cooling systems of Mu3e experiment

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Mu3e is an upcoming experiment at Paul Scherrer Institut in the search for the strongly suppressed decay of μ->eee. It will use an ultra-lightweight silicon pixel detector using thinned HV-CMOS MAPS chips. Untriggered, zero-suppressed, always-on operation is needed for observing random decays of muons at rest with a decay rate of 10^8-10^9 decays per second. More than 1 m2 of instrumented surface will produce about 3 kW of heat (≤250 mW/cm2). Traditional cooling approaches are in conflict with the low-mass requirements, hence a gaseous helium flow cooling system will be implemented. This talk will give a report on the chip status, the mechanical design challenges with our solutions and the results of our comprehensive cooling studies performed recently.

Future facilities/experiments / **53**

New Developments for the ILC Vertex Detectors

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The International Linear Collider (ILC) is the next generation electron-positron high energy frontier machine. To perform the precision Higgs measurements and search for new physics, precise measurements of the vertex positions which are not achieved current experiments, are required. We will report on the new developments on the ILC vertex detectors covering sensor technologies and mechanical and cooling structures.

Timing detectors / **1**

Next-Generation Tracking System for Future Hadron Colliders

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The design of future high-energy and high-intensity hadronic machines, such as FCC-hh, relies on the ability of detectors to sustain harsh radiation environments while keeping excellent performances on tracking and tagging all the interaction products. In order to face the challenge, a vast R&D effort is required.

In this contribution, we propose a novel concept of tracking system, that combines the possibility to track particles up to fluences of the order of 5-10·10^{16} n_{eq}/cm^2 together with a precise time information, σ_t ~ 10 ps. For this purpose, Low-Gain Avalanche Diodes (LGAD) are the suited technology.

For the innermost, most irradiated portion of the detector, very thin sensors (20-40 μm) with moderate gain (~5-10) can provide the required tolerance to the radiation. For such detectors, the internal gain mechanism of LGAD allows to provide the same amount of charge released by a particle passing 100-200 μm of standard PiN diodes up to ϕ ~ 0.5·10^{16} n_{eq}/cm^2. Above those fluences, the thin doped layer responsible for the signal multiplication gets deactivated, but if operated at the proper bias voltage (~500 V) the signal multiplication happens inside the whole irradiated bulk volume.

Moreover, in the region of the tracker detector where the level of overall fluence keeps ≤ 0.5-1·10^{16} n_{eq}/cm^2, LGAD with a geometry optimised for timing measurement can be used to provide precise position and timing information at the same time. Considering the current timing performances of LGAD under irradiation and assuming a σ_t ~ 40 ps from sensor + ASIC, the usage of track-timing layers alternated to tracking only layers can provide an ultimate σ_t ~ 10 ps per single track.

Large detectors / **11**

Operational Experience and Performance with the ATLAS Pixel detector at the Large Hadron Collider

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The tracking performance of the ATLAS detector relies critically on its 4-layer Pixel Detector which has undergone significant hardware and readout upgrades to meet the challenges imposed by the higher collision energy, pileup and luminosity delivered by the Large Hadron Collider (LHC), with record breaking instantaneous luminosities of 2 x 10^34 cm-2 s-1 recently surpassed.
The key status and performance metrics of the ATLAS Pixel Detector are summarized, and the operational experience and requirements to ensure optimum data quality and data taking efficiency will be described, with special emphasis on radiation damage experience.

Vertex detector subsystems / **61**

Optical links for high energy physics experiments in the next decade

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Optical data links have become ubiquitous in modern High Energy Physics experiments. Since their first large scale use in LHC detectors, they have proven to be extremely robust, reliable and resistant to radiation and magnetic fields. Based on this positive experience, optical links operating at higher and higher data rates have been qualified for use in a broad range of detectors worldwide. For instance, current developments for HL-LHC target data rates of 10 Gb/s, radiation resistance levels as high as 1 MGy and 10^15 n/cm2, and a tolerance to magnetic fields up to 4 T.
Unfortunately, radiation tests of multiple types of active optoelectronic components (semiconductor lasers and photodiodes) clearly indicate that they will reach the limits of their radiation resistance at HL-LHC. A novel optical link technology must thus be developed to address the requirements of future detectors aiming at extreme radiation hardness.
This presentation will review the performance of the common optical link system being developed for HL-LHC experiments and will highlight its limitations. It will then explore the available options to achieve higher data rates and better radiation resistance in the future. Finally, it will expand on silicon photonics as one of the candidate technologies to reach extreme radiation resistance and high integration density, at the expense however of a much more complex optical system.

Workshop summary / **78**

Oral presentations summary talk

Large detectors / **21**

Performance of the Belle II Silicon Vertex Detector

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The Belle II experiment at the SuperKEKB collider of KEK (Japan) will accumulate 50 ab^{-1} of e^+e^- collision data at an unprecedented instantaneous luminosity of 8×10^{35} cm^{-2}s^{-1}, about 40 times larger than its predecessor. The Belle II vertex detector plays a crucial role in the rich Belle II physics program, especially for time-dependent measurements. It consists of two layers of DEPFET-based pixels and four layers of double sided silicon strip detectors (SVD). The vertex detector has recently completed its first physics run in spring 2019 and is scheduled to restart in October for the autumn run of SuperKEKB. In this talk, I will report results from the commissioning of the SVD and its performance measured with the first collision data set.

Workshop summary / **77**

Poster session summary talk

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Prototype module construction for the high luminosity upgrade of the CMS pixel detector

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With the planned upgrades of the LHC towards a high luminosity, the entire CMS silicon tracker will be replaced in order to cope with the resulting elevated pileup and radiation levels. To meet these requirements for the inner tracker, a new pixel readout chip was developed by the RD53 collaboration in 65nm CMOS technology, featuring a higher readout bandwidth and increased granularity and radiation tolerance. These chips are operated at high currents rendering the classical parallel powering of individual devices inefficient. A serial powering scheme has therefore been developed where the input current is shared by a chain of devices, reducing considerably the power loss in the detector and thus keeping the requirements for powering and cooling at acceptable levels.
Novel module concepts, implementing the new readout and powering schemes, were developed and multiple prototypes are currently under test. The development, construction and test results of prototype modules for the upgraded CMS pixel detector will be presented.

Sensor/ASICs technology / **33**

RD53 analog front-end processors for the ATLAS and CMS experiments at the High-Luminosity LHC

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This work discusses the design and the main results relevant to the characterization of analog front-end processors in view of their operation in the pixel detector readout chips of ATLAS and CMS

at the High-Luminosity LHC. The front-end channels presented in this paper are part of RD53A, a large scale demonstrator designed in a 65 nm CMOS technology by the RD53 collaboration. The collaboration is now developing the full-sized readout chips for the actual experiments. Some details on the improvements implemented in the analog front-ends will be provided in the conference paper.

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Radiation Hardness Studies of ALPIDE, the CMOS sensor for the ALICE ITS Upgrade

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The ALICE (A Large Ion Collider Experiment) experiment at CERN is undergoing a major upgrade of its Inner Tracking System (ITS) detector. The new ITS will have seven concentric cylindrical layers of monolithic active pixel sensors ALPIDEs, which are based on the 180 nm CMOS technology by TowerJazz. It is expected that during their operation, the sensors in the innermost layer will obtain a total ionization dose (TID) of 270 krad and 10^{12} 1 MeV n_{eq} cm^{-2} of non-ionizing energy loss (NIEL). The project proposal however expects that the sensors should sustain ten times higher radiation loads. Radiation hardness of ALPIDE sensors was studied using a 30 MeV proton beam provided by the U-120M cyclotron of the Nuclear Physics Institute of the Czech Academy of Sciences in Řež. The poster will present results from these radiation hardness studies and we will show that the ALPIDE sensor fulfils the technical design requirements in terms of radiation hardness.

Radiation effects / 46

Radiation induced performance degradation of p-type silicon devices by acceptor removal effects

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New sensor technologies are constantly under development to cope with the ever increasing requirements for high energy physics (HEP) detectors. For the High-Luminosity LHC (HL-LHC) and the Future Circular Collider (FCC-hh) higher radiation hardness, improved timing performance and lower cost large area detector technologies are essential, to name just some of the major challenges. Recent developments of radiation hard p-type silicon planar sensors, sensors with intrinsic gain for timing applications and monolithic sensors are examples for upcoming new detector technologies. A commonality of these new sensors is the use of boron doped p-type silicon, while present HEP silicon sensors are essentially based on n type silicon. Consequently, radiation effects in p-type silicon have been less studied in the detector community, but are now of high relevance. In this presentation, we review radiation effects in p-type silicon devices with focus on acceptor removal effects.

In p-type silicon doped with Boron exposure to radiation cause an apparent deactivation of the dopant. This so-called acceptor removal effect is for example evidenced by an initial decrease of depletion voltage in p-type sensors with rising particle fluence, while after exposure to higher fluences the Boron is de-activated and the device behavior is dominated by other radiation induced defects. Low Gain Avalanche Detectors (LGADs) are the baseline technology for future solid-state timing layers at the HL-LHC. Their good timing performance is based on the intrinsic amplification of the signal by impact ionization in a p-type layer, the gain layer. Radiation effects reduce the active

Boron concentration in the gain layer and lead to a reduction in field-strength and consequently loss of intrinsic signal amplification, thus limiting the radiation hardness of this technology. Monolithic detectors, especially High Voltage CMOS, is another technology affected by acceptor removal, as the bulk silicon used for the sensor is typically of p-type. We review the impact of radiation damage on the depleted volume as function of the initial Boron concentration and the corresponding change in signal charge and device performance.
The origin of the radiation induced de-activation of the Boron acceptor is found in the creation of defect levels that contain Boron, that is consequently no longer acting as shallow dopant. Defect spectroscopy techniques like TSC (Thermally Stimulated Currents) and DLTS (Deep Level Transient Spectroscopy) allow detecting these levels, help to understand the defect formation kinetics on the microscopic level and open the door to defect engineering approaches to mitigate the acceptor removal effect. Latest RD50 results in this research field are reviewed.

Radiation effects / **31**

Radiation-tolerant Silicon Detectors for the LHC Phase-II Upgrade and Beyond: Review of RD50 Activities

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The inner tracking layers of all LHC experiments were designed and developed to cope with the environment of the present Large Hadron Collider (LHC). At the LHC Phase-II Upgrade foreseen for 2026, the particle densities and radiation levels will increase by roughly an order of magnitude compared to the present LHC conditions, and the silicon-based inner tracking systems have to be able to withstand fluences of up to 2e16 neq/cm2.
Within the CERN RD50 Collaboration, a large R&D program has been underway for more than a decade across experimental boundaries to develop silicon sensors with sufficient radiation tolerance for HL-LHC tracker detectors. This challenge is approached simultaneously from different angles: Collaboration activities range from defect characterization and modeling to sensor development and the integration of sensors into full detector systems.
One of the main objectives of the RD50 collaboration is to gain a deeper understanding of the connection between the macroscopic sensor properties, such as radiation-induced increase of leakage current and trapping, and the microscopic properties at the defect level. With increasing fluence, radiation-induced phenomena on a sensor level become increasingly complex, and call for advanced techniques and strategies to identify the mechanisms behind the observed changes in material properties. Furthermore, at very high radiation levels the differences in radiation damage caused by different types of radiation are highlighted, which poses a challenge for the scaling of radiation damage.
Experimental results are complemented by simulation studies, e.g. to obtain predictions of the electric field distributions and trapping in the silicon sensors and to assist device structure optimization, using both open-source and commercial TCAD simulation tools.

This talk will present an overview of research activities within the RD50 Collaboration, with an emphasis on the characterization and current understanding of radiation-induced effects corresponding to HL-LHC fluences. We will comment on considerations for silicon detectors in future collider experiments, where tracker detectors may be exposed to fluences of up to 7e17 neq/cm2.
We will also discuss recent developments in novel silicon detector technologies and fabrication, for example 3D detectors and low-gain avalanche detectors, as far as they are not covered in dedicated presentations.

Tracking and vertexing / **34**

Real-time reconstruction of pixel vertex detectors with FPGAs

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The LHCb experiment is undergoing a major upgrade in view of Run-3, in which the complete detector will be read out, and events fully reconstructed, at the full LHC crossing rate (averaging 30 MHz). One of the key steps of event reconstruction is finding tracks in the new, high precision pixel vertex detector (VELOPIX). This step is the necessary starting point for most of the rest of the reconstruction, and requires a significant fraction (close to a half) of the total CPU time that will be availabe in the upgraded Event Filter Farm. We present the current status of a LHCb R&D project devoted to accelerating this computation by the use of an array of commercial state-of-the-art FPGA cards embedded in the DAQ system, performing pattern recognition in the vertex detector 'on the fly', while the detector is being readout at 30 MHz.

Sensor/ASICs technology / **48**

Recent depleted CMOS developments within the CERN-RD50 framework

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Depleted Monolithic Active Pixel Sensors (DMAPS) in commercial High Voltage-CMOS (HV-CMOS) processes are groundbreaking tracking detectors for particle physics experiments, as they offer a competitive and cost-effective solution over a large range of applications. In spite of the major improvements demonstrated by DMAPS during the last few years, these sensors require further research especially in terms of improving the time resolution and radiation tolerance to realise the full potential of the extremely challenging particle physics experiments planned for the near future. In this context, the CERN-RD50 collaboration has started to study depleted CMOS sensors as one of its main priorities.

This contribution presents the R&D programme within the CERN-RD50 collaboration to study depleted CMOS sensors. We will describe the 2 test prototypes developed so far, which are in the 150 nm HV-CMOS technology process from LFoundry and manufactured on high resistivity substrates. Following from work in the wider community, the first prototype (RD50-MPW1) integrates 2 fully monolithic matrices of depleted CMOS pixels and test structures for edge Transient Current Technique (eTCT) characterisation. One of the matrices has 50 μm x 50 μm pixels with FE-I3 style readout electronics embedded inside the sensing area of the pixels, while the other matrix has 75 μm x 75 μm pixels with a 16-bit counter for photon counting applications. The second prototype (RD50-MPW2) implements a small matrix of depleted CMOS pixels with analog readout electronics to minimise the sensor readout time, several other readout circuits and test structures. All the designs of RD50-MPW2 incorporate new methodologies to reduce the large leakage currents, and therefore increase the radiation tolerance, measured with RD50-MPW1. These methodologies comprise blocking the generation of certain filling layers added by the foundry during the post-processing stage and adding a series of guard rings around the chip. We will also describe the design work towards a new pixel

flavour, named sampling pixel and recently submitted for fabrication with LFoundry as a proof-of-concept, which in simulations improves the time resolution of depleted CMOS sensors to approximately 2 ns. This design and others will be included in the large area submission RD50-ENGRUN1 planned by the collaboration.

The details that will be covered in this presentation include device simulations with TCAD to optimise the leakage current of DMAPS, ASIC design aspects of the pixel flavours that have been fabricated so far, the development of a common and flexible data acquisition system based on the Caribou generic board and used in the experimental evaluation of the prototypes, and the main performance results achieved already.

Radiation effects / **69**

Recent progress in CVD diamond detector R&D

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Progress in experimental particle physics continues to depend crucially upon the ability to carry out experiments in a high radiation environment. The RD42 Collaboration at CERN is investigating Chemical Vapor Deposition (CVD) diamond as a material for tracking detectors operating in such conditions. CVD diamond detectors have been used routinely and successfully in beam conditions/beam loss monitors as the innermost detectors in the highest radiation areas of Large Hadron Collider (LHC) experiments.
This talk will present an overview of the latest developments from RD42, including the most recent radiation tolerance measurements performed on the highest quality single-crystal (scCVD) and polycrystalline Chemical Vapor Deposition (pCVD) diamond material with 800 MeV and 24 GeV protons up to a fluence of about 2 x 10^16 protons/cm^2.
Over the last two years the RD42 collaboration has furthermore constructed a series of 3D pixel detectors using pCVD diamond as the active material and laser fabricated electrodes in the bulk, with 3D cell sizes of 50 um x 50 um and 3D electrode diameters of 2.6 um achieved. These devices were studied in test beams using the latest pixel readout electronics developed by ATLAS and CMS. The talk will present recent results obtained with these devices.

Timing detectors / **7**

Recent results of the TIMESPOT project on sensors and electronics developments for future vertex detectors

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The TIMESPOT project is a R&D project entirely funded by INFN – Italy. It is active since the end of 2017 and will operate for 3 years. The project aims at the construction of a mini-tracker demonstrator implementing both high space and time resolutions at the single pixel level. The pixels have a pitch of 55x55 μm^2. Specified r.m.s. time resolution is equal or better than 50 ps.
Sensors are based both on 3D silicon and diamond technologies, whose layout and fabrication process have been suitably optimized for best time resolution. Read-out pixel electronics is developed in 28-nm CMOS technology. The single pixel circuit contains one charge sensitive amplifier, one discriminator and one TDC per pixel.
The first batch of 3D silicon sensors, containing several test structures based on different geometries

of the electrodes, has been delivered last June and is currently under characterization tests. Among the different structures being tested and compared, a high density trench-type layout has been realized, being particularly promising about timing performance.
I-V curves have been already extracted showing a general good behaviour of the sensors. Dynamic tests using a pulsed laser beam are on-going to evaluate the sensor performce in terms of charge collection efficiency and timing.
A first prototype of 3D column-type diamond sensor with optimized timing performance has been also realized and tested with encouraging results.
The first prototype of the 28-nm CMOS ASIC has been delivered in Spring 2019 and is being tested. One of the important results is the feasibility of integrating a high performance TDC (about 20 ps r.m.s. time resolution) inside a total pixel circuit area of 55x55 μm^2..
In the present paper our results on sensor and readout electronics tests will be illustrated. They represent an important step forward in the development of pixels with timing operating at extremely high interaction rates.

Excursion to Dubrovnik / **75**

Return to Lopud

Vertex detector subsystems / **36**

Serial Powering for the Tracker Phase-2 Upgrade

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The upgrade of the Large Hadron Collider for the High-Luminosity (HL-LHC) phase, will introduce extreme operating conditions for the CMS Inner Tracker, including hit rates of 3.2 GHz/cm2 and a trigger rate of 750 kHz. The radiation levels will be reaching the unprecedented levels of 1.25 Grad of Total Ionizing Dose (TID) and a hadron fluence of 2.3×10^16 neq cm−2 for 10 years of operation. In addition, there are very tight physical constraints on the available space for the services as well as stringent material requirements posed in order to maintain good tracking performance. Therefore, a new and highly efficient, low mass Inner Tracker detector is being designed and will be installed in CMS to fully exploit the physics potential of the upgraded machine.

The Inner Tracker detector will be made of 3900 hybrid modules i.e. silicon sensors bump-bonded to pixel readout chips (two or four). Both thin planar and 3D silicon sensors are being considered with a pixel aspect ratio of 25x100 um2 or 50x50 um2. The pixel readout chip demands a deep sub-micron CMOS technology and an efficient architecture, where groups of pixel channels will share digital resources for buffering, control and data formatting. A large demonstrator pixel readout chip, the RD53A, has been designed by the RD53 collaboration in 65 nm CMOS technology addressing all the above-mentioned challenges. The use of this modern high density low power CMOS technology with low supply voltage (1.2 V), demands significant current levels of about 2 A per chip, resulting in a total of 40 kW needed to power the final pixel readout chips, the design of which will be submitted in spring 2020.

A serial power distribution scheme is the only viable solution to supply the HL-LHC pixel detectors with the required current levels, within acceptable material budget and power cable losses. In serial powering, a constant supply current is provided to a chain of modules (up to twelve) powered in series, while the chips on a module (two or four) are connected in parallel. To support this scheme, on-chip shunt-regulators are needed to generate locally the required voltages for the pixel chip. The RD53A chip has two integrated, radiation hard, and highly specialized and optimized Shunt-Low Dropout (Shunt-LDO) regulators, one per power domain (analog and digital).

The presentation will describe laboratory tests and results that demonstrate a reliable and efficient operation of this novel serial powering scheme. An overview of its implementation for the future CMS Inner Tracker and respective developments will be given. System tests performed on serial power chains of prototype RD53A quad modules, which host four RD53A chips on a high-density interface (HDI), will be presented. In addition, results from tests of failure analysis in chains of RD53A chips will be shown including reliability studies of the Shunt-LDO regulator. Finally, new Shunt-LDO features and improvements towards the final design of the CMS pixel chip will be discussed and remaining open points for the optimization of serial powering in CMS will be addressed.

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Series Production and Test of Hybrid Modules for the ALICE ITS Upgrade

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ALICE is one of the four experiments at the LHC located at CERN. As part of the upgrade of the detector, the current Inner Tracking System (ITS) will be replaced by an all silicon detector constructed from pixel sensors with a pitch of 29 × 27 μm^2 using CMOS Monolithic Active Pixel Sensors (MAPs) technology. The goal of this upgrade is to enable precise measurements of low momenta particles by significantly improving the impact parameter resolution, tracking efficiency and readout capacity. The detector consists of 7 concentric layers split into two barrels, an inner barrel and an outer barrel. To construct a layer in the detector several sensors are arranged and glued to an FPC and electrically connected through wirebonds to create a hybrid module. These modules are then joined together to make the staves and then finally the barrels that vary in size depending on the layer. The module production was carried out at five assembly sites and has now finished. In total over 2500 modules were produced with a yield of 85% for detector grade modules. Each module underwent wire pull tests to assess the quality of the bonds, extensive electrical tests to evaluate the functionality of the module and classify it based on the results. Metrology was also carried out on selected modules to better understand the mechanical properties and the quality of the assembly during the construction phase. This poster will present the assembly procedure of the modules, give details and results of the tests carried out and a summary of the production as a whole.

Future facilities/experiments / **9**

Silicon Vertex & Tracking Detectors for the Compact Linear Collider

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CLIC is a proposed linear e+e- collider with center-of-mass energies of up to 3TeV. Its main objectives are precise top quark, Higgs boson and Beyond Standard Model physics. In addition to spatial resolutions of a few micrometers and a very low material budget, the vertex and tracking detectors also require timing capabilities with a precision of a few nanoseconds to allow suppression of beam-induced background particles.

Different technologies using hybrid silicon detectors are explored for the vertex detectors, such as dedicated 65nm readout ASICs, small-pitch sensors as well as bonding using anisotropic conductive films. Monolithic sensors are the current choice for the tracking detector, and a prototype using

a 180nm high-resistivity CMOS process has been designed and produced, and is currently under evaluation.
Different designs using a silicon-on-insulator process are under investigation for both vertex and tracking detector.

All prototypes are tested in laboratory and beam tests, and newly developed simulation tools combining Geant4 and TCAD are used to assess and optimize their performance. This contribution gives an overview of the R&D program for the CLIC vertex and tracking detectors, highlighting new results from the prototypes.

Non-HEP applications / 50

Silicon tracking detectors in space-borne experiments

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Silicon tracking detectors are playing a crucial role in space-borne astroparticle experiments for the measurement of both charged cosmic rays and gamma rays.
The technology used for accelerator based experiments has been proven to work properly in space with high reliability and is used in several running and planned experiments.
I will review the current experiments equipped with silicon microstrips detector and will give an overview on the future mission that plan to use microstrips or pixel semiconductor detectors.

Non-HEP applications / 38

Status of the CCDs sensors for DAMIC/DAMIC-M

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Recent advances in CCD technology due to the increase in the purity of the silicon have allowed the fabrication of thicker devices, achieving a record thickness of 675 microns with an area of 6cm x 6cm, for a CCD mass of 5.8 g. This opens up a new experimental frontier in searching for coherent scattering of dark matter or neutrinos from silicon nuclei that produce ionisation energies of only 10s of electron Volts.
Furthermore, these CCDs also present high spatial resolution and an excellent energy response in very effective background identification techniques. This has been the idea of the DAMIC detector located at SNOLAB, taking data since 2017. The charge resolution with such a low electronic noise (approx. 2 e-) allows an unprecedentedly low energy threshold of a few tens of eV (40eV), dominated by the noise of the readout amplifier. The extremely low leakage current is the lowest dark current ever measured in a silicon detector, <10-21 A/cm2 at an operating temperature of 105 K [38], exquisite spatial resolution and 3D reconstruction. A truly unique capability of DAMIC is that background can be identified and rejected as spatially correlated events occurring at different times. Hence, DAMIC has the ability to distinguish radiogenic backgrounds such as alphas, betas, muons, etc. This imaging capability of the CCDs allows to observe ¨in situ¨ disintegration chains like 238U, 232Th, 32Si, etc. These characteristics make the DAMIC CCDs a well-suited detector to identify and suppress radioactive backgrounds and search for Dark matter candidates.
The collaborations is planning to increase to 1kg of CCD cameras in the next three years in the Laboratoire Souterrain de Modane (CNRS / Université Grenoble Alpes). The DAMIC-M CCDs will be 6k x 6k pixel sensors with a skipper-CCD, a breakthrough technology with unprecedented sensitivity

for ultralow-energy particle detection, with repetitive, nondestructive readout of a a thick, fully depleted charge-coupled device. DAMIC-M will achieve a noise level of less than 0.1 e rms/pixel. Such a low noise readout and a dark current below 10-21 A/cm2 will enable a threshold of 2 or 3 electrons (corresponding to DM energy transfers as low as ≈ 3 eV given the silicon band gap energy). DAMIC-M will feature the most massive CCDs ever built. With this unprecedented sensitivity, DAMIC-M will take a leap forward of several orders of magnitude in the exploration of the dark matter particle hypothesis,DAMIC-M, will pioneer the low-mass DM searches with unprecedented sensitivity to DM-electron scattering and hidden-photon DM, by improving by orders of magnitude the sensitivity to the ionisation signals from the scattering of dark matter particles with valence electrons.

Simulation / **44**

TCAD advanced radiation damage modelling in silicon detectors

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In this work we present the development of a comprehensive (surface and bulk) TCAD radiation damage effects model which enables a predictive insight into the electrical behavior of novel solid-state detectors up to the particle fluences expected at the end of HL-LHC.
To better understand in a comprehensive framework the complex and articulated phenomena related to the radiation damage mechanisms TCAD simulations have been carried out and compared with measurements performed on several test structures and sensors. In particular, surface radiation damage effects have been deeply investigated on both p-type and n-type substrate test structures exposed to X-ray irradiation at doses in the range 0.05-100 Mrad(SiO2). By analyzing the properties of the SiO2 layer and of the Si-SiO2 interface as a function of the dose physically meaningful parameters such as the integrated interface trap density and the oxide charge, peculiar to different vendors/technology options have been extrapolated from measurements aiming at the TCAD model validation. The
complete bulk and surface radiation damage model findings have been then compared with available measurements in terms of charge collection efficiency up to 2×10 16 1 MeV equivalent n/cm2. The predictive capabilities of the combined surface and bulk new University of Perugia TCAD model can be therefore exploited for the design and optimization of the new generation of silicon detectors to be used in future HEP experiments.

Simulation / **58**

TCAD and recent defect studies

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This talk will expone recent simulation techniques for analyzing acceptor removal, new defects model (in particular the pentatrap Hamburg model and the new Perugia model) and how to take into account effects related to temperature and the signal processing from the electronics front end. Acceptor removal in LGAD, for example, is now a problem under study and its simulation needs to

define ad hoc device models, to consider the appropriate trap emulation and also to take into account, for timing purposes, the front end signal processing part.

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Test Beam Characterization of Prototype Modules for the ATLAS Inner Tracker Strip Detector

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After more than ten years of operations, starting from 2024 the LHC will be upgraded to the High-Luminosity LHC (HL-LHC). The HL-LHC will deliver a total integrated luminosity of up to 4000fb-1 in about ten years, with a peak luminosity five times higher than that which was reached before the current LHC shutdown. To cope with the higher radiation levels and pile up, the ATLAS experiment will replace the current tracking system with an all silicon detector, the Inner Tracker (ITk), consisting of inner pixel layers and outer strip layers.

The ITk Strip detector will operate in a much harsher environment than the current strip detector, the Semiconductor Tracker. For this reason, ATLAS has undertaken an intense R&D program to develop new radiation-hard silicon sensors and front-end chips. As part of this program, several test beams have been performed to characterize the performance of the prototype modules. A strip module is the basic building unit of the ITk Strip detector and is composed of an n+-in-p silicon strip sensor, the hybrids, which host the front-end chips, and a power board. The hybrids and the power board are glued directly to the silicon sensor.

In this contribution, test beam measurements obtained with several prototype modules are presented. Results of modules with a prototype version of the front end chip (ABC130) and the production version (ABCStar) are discussed. A few modules have been irradiated to approximately their end-of-lifetime fluence, and their performance is compared to the requirements for the ATLAS experiment. The measurements were performed at the DESY and CERN test beam facilities, with the use of EUDET-type pixel telescopes as reference systems. The main focus of the characterization lies on the performance of the sensors and front-end electronics, with results on efficiency, charge collection, noise occupancy and tracking performance.

Vertex detector subsystems / 56

The ALICE ITS Upgrade Readout and Power System

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For the CERN LHC Run 3, the ALICE experiment completely redesigned the Inner Tracking System, now consisting of seven cylindrical layers instrumented with 24120 Monolithic Active Pixel Sensors (MAPS), covering a total surface area of 10 m2. The readout and powering systems are composed of 192 identical Readout Units (RUs) and 142 Power Boards (PBs), respectively, and have complete control over all sensor operations, including power management, triggering, data readout and slow control. In the novel ITS the MAPS sensors directly drive the differential high-speed links connecting them to the Readout Units, making it mandatory to place the readout system as close as possible to the detector to ensure reliable connection up to the design bitrate of 1.2 Gb/s. The power system is similarly located as close as possible to the detector in order to minimize the power loss due to the cables, and actually shares the same crates with the readout system within the magnet yoke. The ITS readout system is connected to the counting room and to the Central Trigger Processor network through 960 Versatile Link optical channels, which allow sustaining a total data rate in excess of 1 Tb/s upstream. This ensures the necessary operational margins to cope with interaction rates of 100 kHz. As the entire system relyes on the optical links for both data acquisition and detector control,a CAN-bus network ensures that there is a backup control path should the optical links fail. The Power Boards also implement several hard-wired automatic threshold switches to selectively cut-off power to sensors in case of anomalous supply conditions.

Due to their installation location, the Readout Units and the Power Boards will both operate at about five meters from the interaction point along the beam axis, and at a radial distance of about one meter. The expected TID at this location, for the entire detector life cycle, is about 10 kRad (safety factor of 10), while the expected flux of particles with sufficient energy (>20 MeV) to induce Single-Event Effects (SEEs) is of the order of 103 cm-2 s-1. Despite having to operate in such hostile radiation environment, the Readout Unit uses a commercial SRAM FPGA as main logic core, as well as commercial DC-DC converters for the power supply. All components were extensively tested for TID, while specific design solutions were adopted against SEE, which actually represent the major concern for the operational reliability of the system.

This contribution describes the design of the system, focusing on the key requirements and how they have been addressed, and discuss the overall performance achieved. Solutions adopted to ensure the system radiation hardness and reliability, for both the hardware and firmware part, as well as the lessons learnt during the system design, testing and integration will be highlighted.

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The ATLAS Forward Proton Time-of-Flight Detector System

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The Time-of-Flight (ToF) detectors of the ATLAS Forward Proton (AFP) system are designed to measure the primary vertex z-position of the pp -> pXp processes by comparing the arrival times measured in the ToF of the two intact protons in the final state.
We present the results obtained from a performance study of the AFP ToF detector operation in 2017. A time resolutions of individual channels ranging between 20 ps and 40 ps are extracted, even though the AFP ToF efficiency is below 10%. The overall time resolution of each ToF detector is found to be 20(26) +- 4(5) ps for side A(C). This represents a superb time resolution for a detector operating at few millimeters from the LHC beams.
Events from ATLAS physics runs at moderate pile-up taken at the end of 2017 are selected with signals in ToF stations at both sides of ATLAS. The difference of the primary vertex z-position measured

by ATLAS and the value obtained by the AFP ToFs is studied. The distribution of the time difference constitutes of a background component from combinatorics due to non-negligible pile-up, and significantly narrower signal component from events where protons from the same interaction are detected in ToF. The fits performed to the distribution of the reconstructed time difference yield the vertex position resolution of about 5 mm +- 1 mm, which is in agreement with the expectation based on single-ToF channel resolution.

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The ATLAS Hardware Track Trigger design towards first prototypes

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In the High Luminosity LHC, planned to start with Run4 in 2026, the ATLAS experiment will be equipped with the Hardware Track Trigger (HTT) system, a dedicated hardware system able to reconstruct tracks in the silicon detectors with short latency. This HTT will be composed of about 700 ATCA boards, based on new technologies available on the market, like high speed links and powerful FPGAs, as well as custom-designed Associative Memories ASIC (AM), which are an evolution of those used extensively in previous experiments and in the ATLAS Fast Tracker (FTK).

The HTT is designed to cope with the expected extreme high luminosity in the so called L0-only scenario, where HTT will operate at the L0 rate (1 MHz). It will provide good quality tracks to the software High-Level-Trigger (HLT), operating as coprocessor, reducing the HLT farm size by a factor of 10, by lightening the load of the software tracking.

All ATLAS upgrade projects are designed also for an evolved, so-called "L0/L1" architecture, where part of HTT is used in a low-latency mode (L1Track), providing tracks in regions of ATLAS at a rate of up to 4MHz, with a latency of a few micro-seconds. This second phase poses very stringent requirements on the latency budget and to the dataflow rates.

All the requirements and the specifications of this system have been assessed. The design of all the components has being reviewed and validated with preliminary simulation studies. After these validations are completed, the development of the first prototypes will start. In this paper we describe the status of the design review, showing challenges and assessed specifications, towards the preparation of the first slice tests with real prototypes.

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The ATLAS ITk Strip Detector System for the Phase-II LHC Upgrade

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The ATLAS experiment at the Large Hadron Collider is currently preparing for a major upgrade of the Inner Tracking for the Phase-II LHC operation (known as HL-LHC), scheduled to start in 2026. In order to achieve the integrated luminosity of 4000 fb-1, the instantaneous luminosity is expected to reach unprecedented values, resulting in about 200 proton-proton interactions in a typical bunch

crossing. The radiation damage at the full integrated luminosity implies integrated hadron fluencies over 2x10^16 neq/cm2 requiring a completed replacement of the existing Inner Detector. An all-silicon Inner Tracker (ITk) is under development with a pixel detector surrounded by a strip detector, aiming to provide increased tracking coverage up to |η|=4.

The current prototyping, targeting an ITk Strip Detector system consisting of four barrel layers in the centre and forward regions composed of six disks at each end, is described in the ATLAS Inner Tracker Strip Detector Technical Design Report (TDR). With the recent final approval of the ITk strip TDR by the CERN Research Board, the prototyping phase is coming to an end and the pre-production readiness phase has started at the institutes involved.

In this contribution we present the design of the ITk Strip Detector. We will give an extended summary of the R&D results achieved, including a wide set of measurements with detectors for several vendors, and irradiated with a range of fluencies and reaching up to to HL-LHC doses, demonstrating the excellent radiation hardness achieved. In addition, we will outline the current status of prototyping on various detector components, with a particular emphasis on the radiation-hard sensors, ASICs and front-end electronics under development. We will also discuss the status of preparations and the plans for the forth-coming pre-production and production phase.

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The LHCb Vertex Locator Upgrade

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The LHCb experiment at the LHC is designed to capture decays of b- and c-hadrons for the study of CP violation and rare decays. It has already had a transformative impact in the field of flavour physics as well as making many general purpose physics measurements in the forward region. At the end of Run-II, many of the LHCb measurements will remain statistically dominated. For this reason the experiment is being upgraded to run at higher luminosity after 2020. The trigger scheme, which currently has a 1 MHz lowest level hardware rate, will be transformed to a strategy whereby the entire experiment is read out at 40 MHz to a flexible software trigger. The increased luminosity and trigger efficiency anticipated at the upgrade will allow significant improvements in measurements across the flavour sector and beyond. In order to allow the triggerless readout the front end electronics of all subdetectors will be changed, and many subdetectors will be upgraded to cope with the increased occupancy and radiation levels anticipated at the upgrade.
The Vertex Locator (VELO) surrounding the interaction region, whose role is to reconstruct and trigger on the primary and secondary vertices of the events, is an example of a subdetector which will be completely changed. The current strip detector will be replaced by a hybrid pixel detector read out with the VeloPix ASIC. The detector operates just 5 mm away from the collision region, and will give optimum track reconstruction efficiency and projected precision at the vertex region.
The upgraded VELO is composed of 52 modules placed along the beam axis. The 26 modules in each half can be retracted during LHC filling and only close to the nominal position after stable beams have been declared. Each module is equipped with 4 silicon hybrid pixel tiles, each read out with by 3 VeloPix ASICs. The pixels have a pitch of 55 μm × 55 μm and the sensors are produced in 200 μm thick p-in-n type silicon. The sensors must withstand an integrated fluence of up to 8×10151~MeV neq/cm2, a roughly equivalent dose of 400 MRad, and it is anticipated that the bias voltage must be raised to 1000V by the end of lifetime of the detector. The highest occupancy ASICs will have pixel hit rates of 800 Mhits/s and produce an output data rate of over 15 Gbits/s, with a total rate of 1.6 Tbits/s anticipated for the whole detector.
The VELO upgrade modules are composed of the detector assemblies and electronics hybrid circuits mounted onto a cooling substrate, which is composed of thin silicon plates with embedded microchannels that allow the circulation of liquid CO2. This technique was selected due to the excellent thermal efficiency, the absence of thermal expansion mismatch with silicon ASIC's and sensors, radiation hardness of CO2, and very low and uniform contribution to the material budget. The front-end hybrids host the VeloPix ASICs and a GBTx ASIC for control and communication. The signals are routed to the electronics mounted outside the vacuum tank via 56~cm copper data tapes running at

5 Gb/s and custom vacuum feedthrough boards.
The secondary vacuum in which the modules are located is separated from the beam vacuum by a thin custom made foil. This foil is manufactured through a novel milling process and possibly thinned further by chemical etching.
The upgraded VELO is currently under construction and module pre-production is underway. The performance of the ASICs, bump bonded sensors and double sided electrical module will be described, along with the first results from the prototype modules in terms of electrical, mechanical and thermal performance, along with the status of the mechanical construction and preparation for assembly.

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The MAPS-based ITS Upgrade for ALICE

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The Inner Tracking System (ITS) Upgrade for the ALICE Experiment at LHC is the first large-area ($\sim$10 m^2) silicon vertex detector based on the CMOS Monolithic Active Pixel Sensor (MAPS) technology, which combines sensitive volume and front-end readout logic in the same piece of silicon. This technology allows a reduced material budget (target value of 0.3% on the innermost layers) thanks to the thin sensors (50-100~μm) and limited need of cooling, in combination with light-material interconnection circuits and support structures. The small pixel pitch ($\sim$30μm), the location of the layers (7 cylindrical layers with radii ranging from 2.3 cm to 39.3 cm from the beam interaction line), and the limited material budget will provide the ALICE experiment with extremely precise tracking resolution. The high-rate readout capabilities will also enable ALICE to collect a large data sample at the 50 kHz Pb-Pb collision rate expected in the LHC Run 3.

The new ITS, now assembled at the surface, is currently undergoing an exhaustive pre-commissioning phase with standalone calibration and cosmic ray data-taking, which will be completed by April 2020 before the installation in the ALICE detector. Experience gained from the construction and the pre-commissioning phase, and plans for the installation and preparation for the data-taking in ALICE will be presented in this talk. The role played by the new ITS within the development path of the MAPS technology for future applications will also be briefly discussed.

Sensor/ASICs technology / **16**

The Timepix4 chip and its design approach

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The Timepix4 chip is the new hybrid pixel detector ASIC designed at CERN in the frame of the Medipix4 collaboration. This new chip will consist of an array of 512x448 pixels with 55 um square pixels. The chip is highly configurable in order to cover a large range of applications and it can be programmed to work in particle tracking mode or in frame based mode. In particle tracking mode the chip works in a data driven readout mode where the chip sends out a 64-bit data packet containing pixel coordinate, time over threshold and time of arrival immediately after the hit is processed by the pixel. The maximum hit rate in particle tracking mode is 360 Mhits/cm2/s with a time tagging bin size of 195 ps. In frame based mode the pixel works in photon counting mode with a maximum count rate of 800 Ghits/cm2/s. The chip includes 16 10 Gbps serializers in order to cope with the maximum particle hit rate in data-driven. The aim of this publication is to present the chip as an example of the usage of modern ASIC design tools and how the designers approach the design of such complex chip.

Large detectors / **66**

The Upstream Tracker for the LHCb Upgrade

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The LHCb experiment is a forward spectrometer at the Large Hadron Collider designed to study the decays of beauty and charm hadrons. During the data taking phase recently concluded, it produced a vast array of data, in flavour physics and in additional physics topics that take advantage of the forward acceptance of the LHCb experiment. In the current LHC's second long shutdown, a major upgrade of the LHCb detector is being installed and commissioned. The upgraded detector will take data at higher luminosity and will implement a flexible software trigger that requires all the detector components to push out their information at 40 MHz. The Upstream Tracker is a new silicon strip detector placed upstream of the LHCb bending magnet. It is composed of four planes of silicon microstrip detectors mounted on both sides of vertical structures called staves, providing mechanical support and CO_2 evaporative cooling. Four different silicon sensor designs are used to handle the varying occupancy over the detector acceptance. The innermost sensors are shaped to optimize the acceptance near the beam pipe, reaching an inner radius 3.5 cm away from the beam axis. A novel embedded pitch adapter design allows direct wire bonding of the sensor strips to front end electronics input channels. A dedicated front-end ASIC, the SALT chip, provides pulse shaping with fast baseline restoration, digitization via 6-bit ADCs, and digital signal processing providing pedestal and common-mode noise subtraction as well as zero-suppression. Near detector electronics organizes the data transmission to the remote data acquisition system and regulated low-voltage power distribution. In this contribution, the performance of the individual detector components is reviewed, with particular emphasis to studies of the sensor-SALT hybrid modules, in test bench studies of modules and instrumented staves. Moreover system studies performed on pre-series staves will be discussed.

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The operational experience, challenges and performance of the ATLAS Semiconductor Tracker during LHC Run-2

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The Large Hadron Collider (LHC) recently completed its Run-2 operation period (2015-2018) which delivered an integrated luminosity of 156 fb-1 at the centre-of-mass *pp* collision energy of 13~TeV. This marked 10 years of successful operation by the ATLAS Semiconductor Tracker (SCT), which operated during Run-2 with instantaneous luminosity and pileup conditions that were far in excess of what the SCT was originally designed to meet. The first significant effects of radiation damage in the SCT were also observed during Run-2. This talk will summarise the operational experience, challenges and performance of the SCT during Run-2, with a focus on the impact and mitigation of radiation damage effects.

Vertex detector subsystems / **45**

Upgrade of the ALICE ITS in LS3

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ALICE is planning to replace its inner-most three tracking layers with a fully cylindrical, bent silicon tracker during LHC Long Shutdown 3 (LS3, targeting 2024-25). The new detector is to reach an unprecedented low material budget of below 0.05% X0 per layer, combined with an intrinsic spatial resolution of around 2 μm in z- and rφ-directions. Its main building part is an ultra-thin (20-40 μm), wafer-scale (300 mm) CMOS Monolithic Active Pixel Sensor, that will be developed in 65 nm technology for this purpose. The sensor dimensions reach up to 280 by 94 mm, and, owing to the flexible nature of silicon chips at these thicknesses, is bent into half-cylinders of radii of 18, 24, and 30 mm, respectively, to form the new detector barrels.

This contribution addresses the detector R&D roadmap as well as projected improvements in performance and related physics yields. The combination of reduced material budget, closer proximity to the interaction point, and higher intrinsic resolution translate into a significant advancement in the measurement of short-lived particles and low-mass di-electrons, which are amongst the main physics goals of ALICE.

Future facilities/experiments / **55**

Vertex and Tracking Detectors for the Circular Electron Positron Collider (CEPC)

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The Circular Electron Positron Collider (CEPC) has been proposed as a Higgs factory to measure the properties of the Higgs boson with high precision and to enable the possibility to explore new physics. To meet the stringent physics requirements, it is necessary to design and construct both vertex and tracking detectors with the state-of-the-art silicon detector technologies. Initial R&D has been focused on CMOS pixel sensors to achieve both high position resolution and low power consumption. They are desirable for the vertex detector, which will sit closest to the interaction point and play a decisive role in precise determination of the primary and secondary vertices that are crucial for heavy flavor tagging. Recently, efforts have been also made to explore the possibility to design the large area silicon tracker with pixel sensors developed with high voltage CMOS technology, which promises both high position resolution and timing resolution. A short stave populated with the latest development of ATLASPix has been proposed for the demonstrator and sensor design tailored toward the CEPC tracker requirements are being pursued.