RD53 analog front-end processors for the ATLAS and CMS experiments at the High-Luminosity LHC

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Outline

- RD53 Collaboration – Challenges & Goals

- The RD53A demonstrator chip

    - Specifications

    - Floorplan

- RD53A analog front-ends

    - Design

    - Test results

- From RD53A to RD53B

- Conclusions

RD53 – An overview

- Collaboration among **ATLAS** & **CMS** communities aiming at the development of large scale pixel chips for LHC phase-2 upgrades

- **65 nm CMOS** is the common technology platform

- **RD53 Goals**

  - Detailed understanding of **radiation effects** in 65nm → guidelines for radiation hardness

  - Design of a **shared rad-hard IPs library**

  - Design and characterization of **full sized pixel array chip**

RD53A
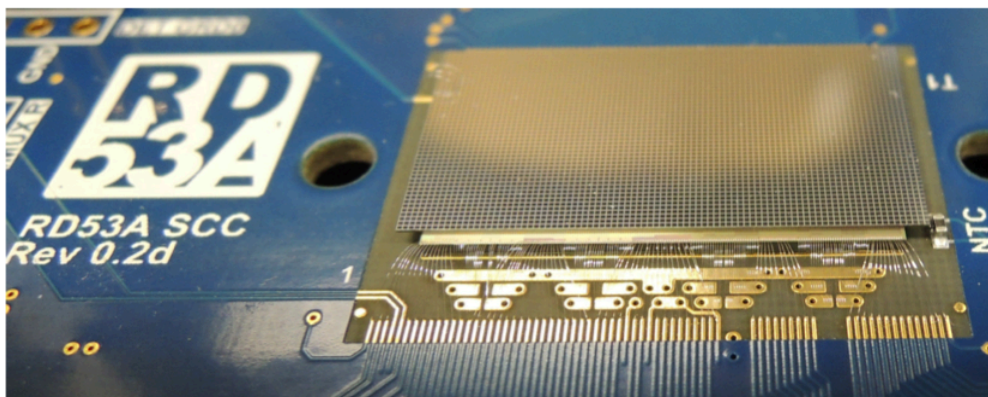
- The efforts of the RD53 collaboration led to the submission of the **RD53A chip**

- 20x11.5 mm^2 chip featuring a matrix of **400x192 pixels** (50x50 μm^2 each)

- It contains design variations for testing purpose (3 analog front-ends, 2 digital readout architectures)

- **Submitted** in August 2017, **comprehensive testing activity** carried out in 2018 and 2019

RD53 timeline

2013 — Building blocks: Analog FEs, IPs
Digital Architecture
Verification environment
Complex Chip Integration
Radiation characterization of the CMOS 65 nm

2015 — Small demonstrators (64x64 pixel matrix)
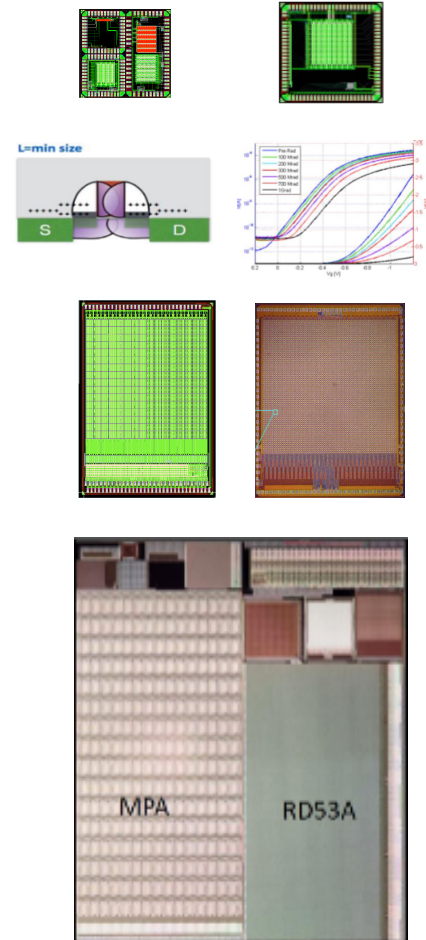FE65P2
CHIPIX65-FE0

2017 — RD53A large scale prototype
400x192 pixel matrix

2019 — RD53B
~400x400 pixel matrix

ATLAS
pixel chip

CMS
pixel chip

Two submissions with different matrix size: **ATLAS** chip first (Nov. 2019), then **CMS** chip (Apr. 2020)

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RD53A main specifications

From the Spec. document   http://cds.cern.ch/record/2113263

- **Hit rate:** up to 3 GHz/cm^2 (75 kHz pixel hit rate)
- **Detector capacitance**: < 100 fF (200 fF for the edge pixels)
- **Detector leakage**: 10 nA (20 nA for the edge pixels)
- **Trigger rate**: max 1 MHz
- **Trigger latency**: 12.5 us
- **Low threshold**: 600 e- $\rightarrow$ severe requirements on noise and dispersion
- **In-time overdrive**: < 600e-
- **Noise occupancy**: < 10^{-6} (in a 25ns interval)
- **Hit loss @ max hit rate**: 1%
- **Radiation tolerance**: 500 Mrad @ -15° C

Top test pad

- Row of test pads for debugging purposes

- Will be removed in the production chip

Pixel matrix

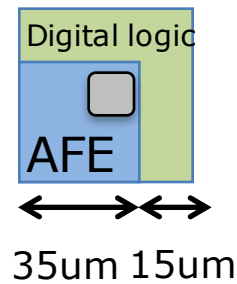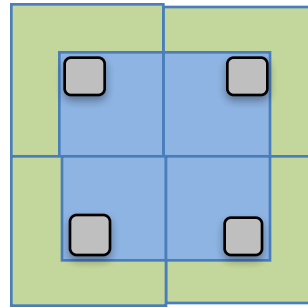- 192 x 400 = 76 800 pixels

Chip Bottom

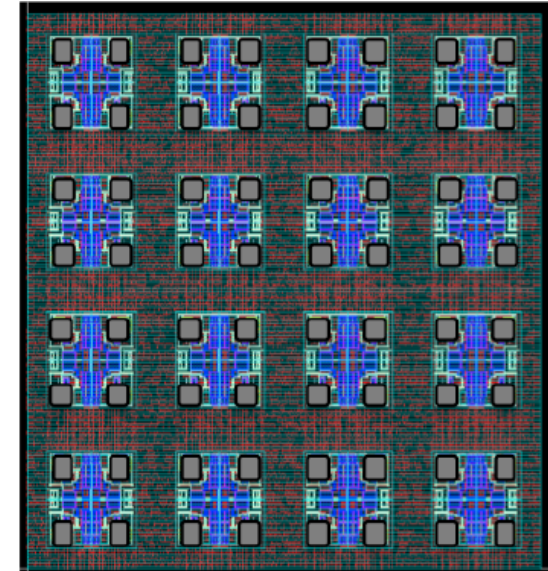- all global analog and digital circuitry needed to bias, configure, monitor the chip and for signal readout
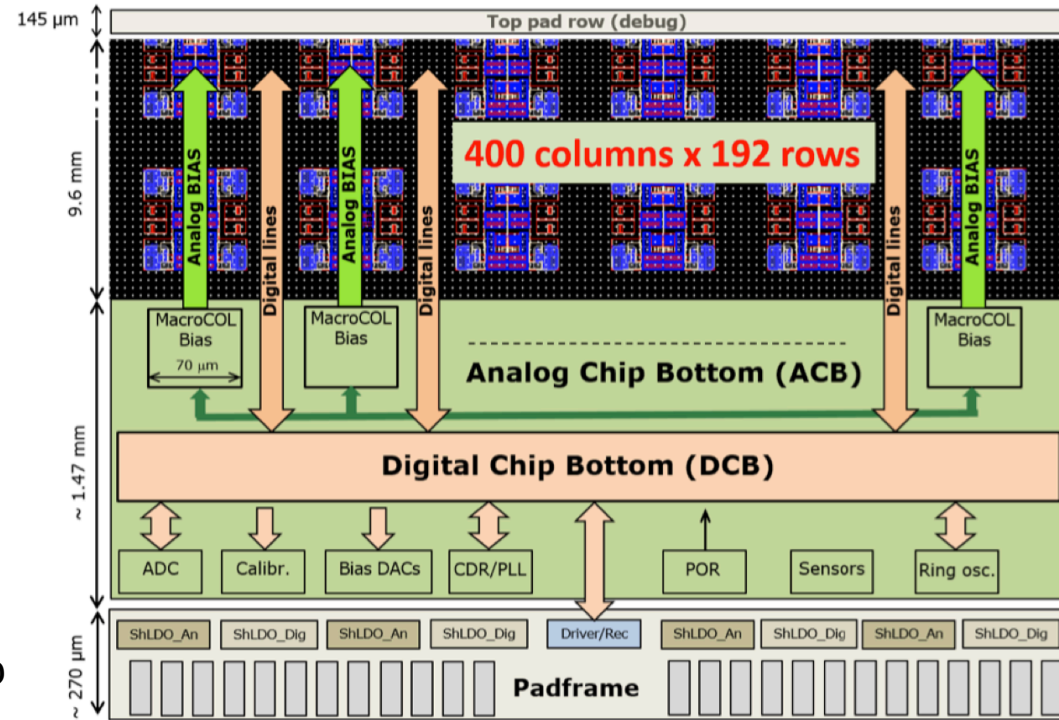
RD53A pixel floorplan

Pixel

35um 15um

Digital logic

AFE

Quad

Core

- **Isolation strategy**: two different DNWs for analog and digital
- DNW-isolated analog 'islands':
  - Occasional PFETs using body NW for sub isolation
  - DNW shorted to V_{DDA}
- DNW-isolated digital 'sea':
  - DNW biased at V_{DDD}
- **Global substrate** not used by supply or device bodies

Serial Powering

- **Serial powering** is the **baseline powering scheme** for CMS and ATLAS HL-LHC pixel detectors
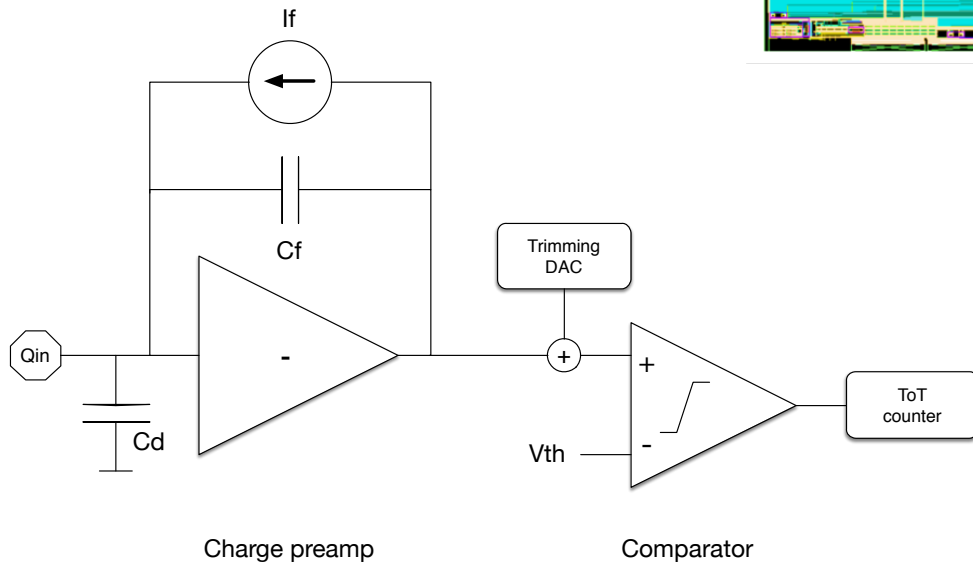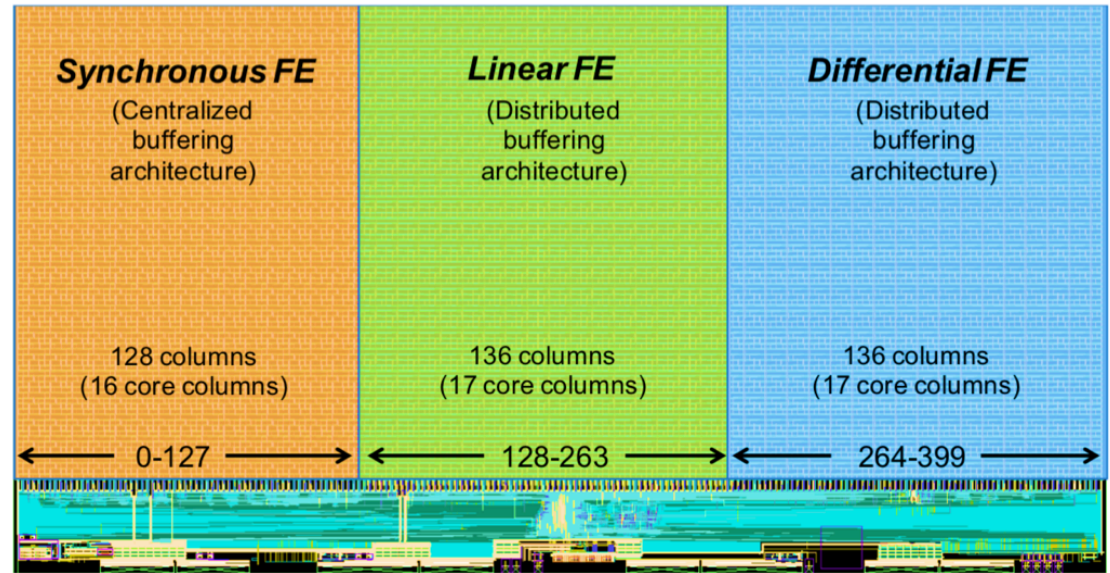
  → D. Koukola talk "Serial Powering for the Tracker Phase-2 Upgrade"

- **RD53A** is designed to operate with serial powering → constant current to power chip modules in series

  - Based on ShuntLDO

  - Dimensioned for production chip

- **Three operation modes:**

  - ShuntLDO: constant input current Iin → local regulated VDD

  - LDO (Shunt is OFF): external un-regulated voltage → local regulated VDD

  - External regulated VDD (Shunt-LDO bypassed)
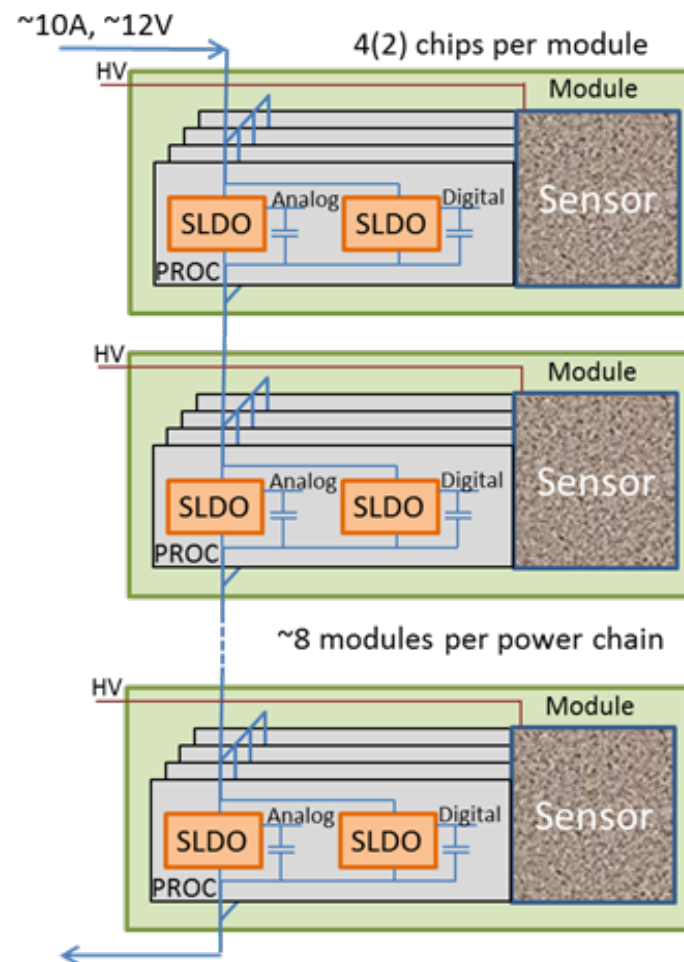
RD53A Analog front-ends

- **3 different** analog FEs integrated in **RD53A**
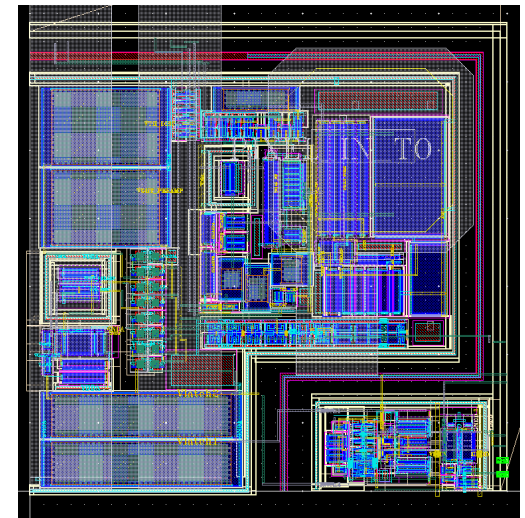
  - Synchronous

  - Linear

  - Differential

Synchronous FE
(Centralized buffering architecture)

128 columns
(16 core columns)

0-127

Linear FE
(Distributed buffering architecture)

136 columns
(17 core columns)

128-263

Differential FE
(Distributed buffering architecture)

136 columns
(17 core columns)

264-399

If

Cf

Qin

Cd

Trimming DAC

Vth

ToT counter

Charge preamp

Comparator

Comprehensive **characterization** of the FEs and **FE reviews** in view of the integration of final chips
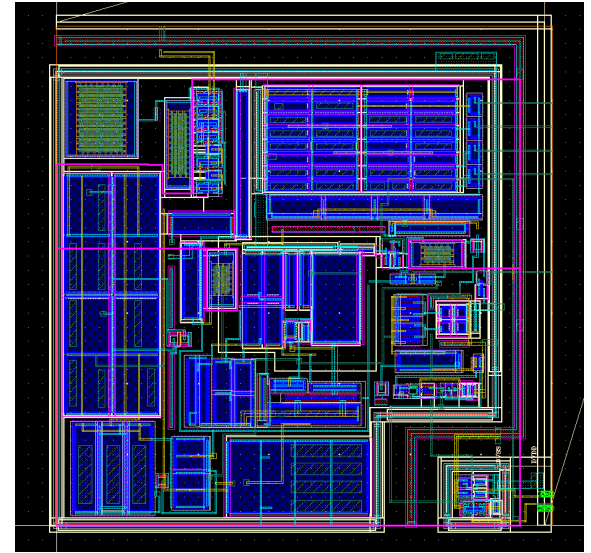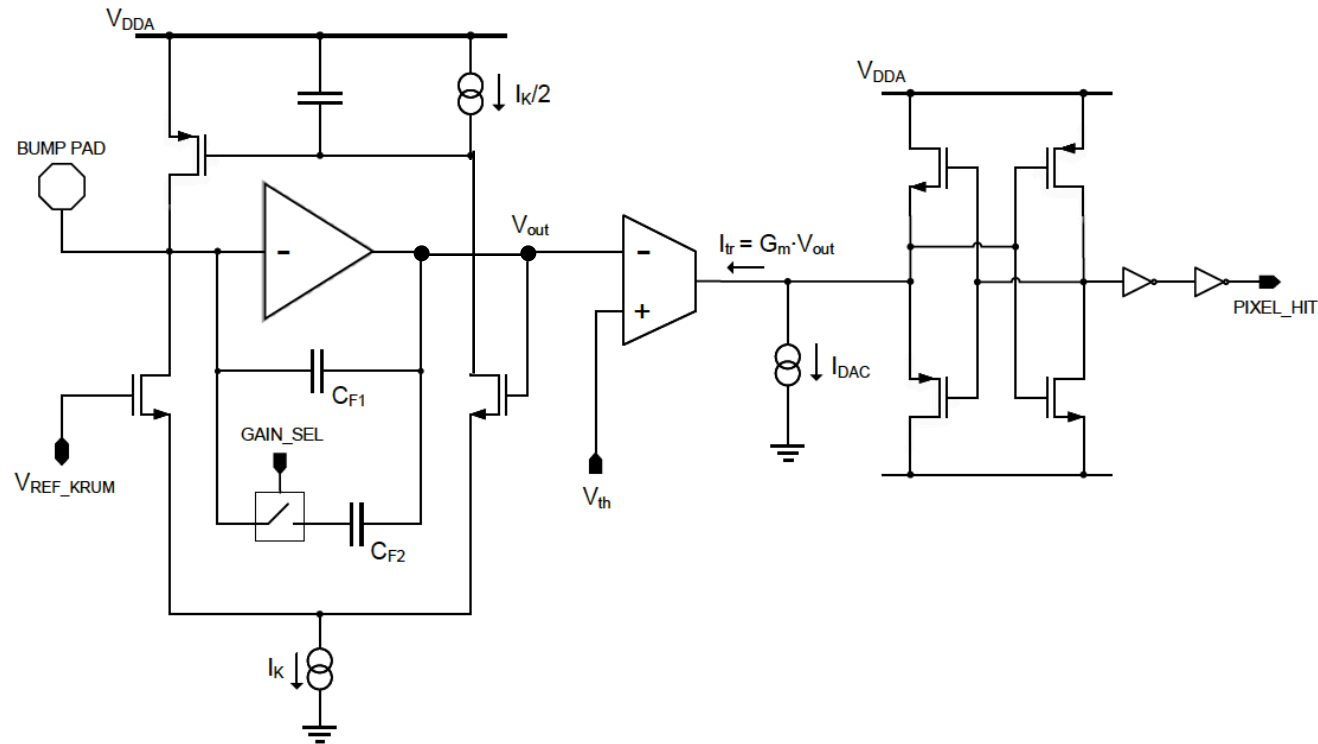
Synchronous Analog Front-end
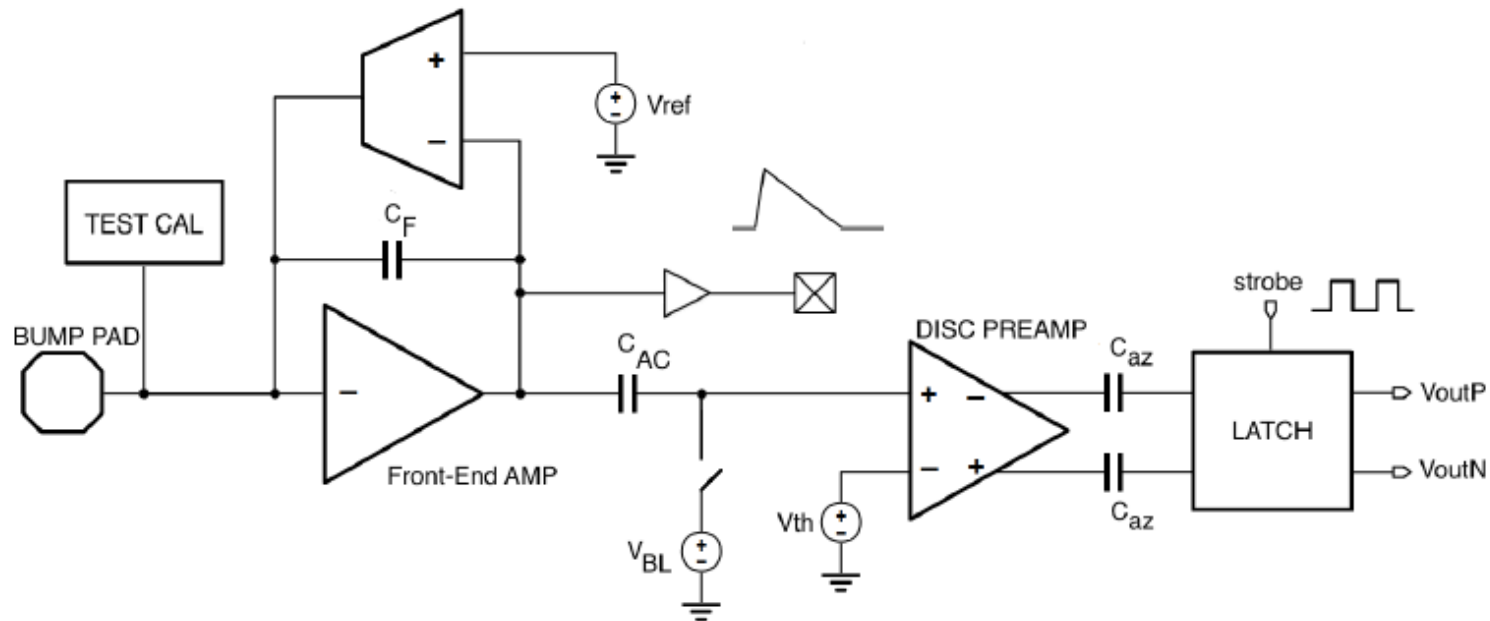
- **One stage CSA** with **Krummenacher** feedback for linear ToT charge encoding

- **Synchronous discriminator**, AC coupled to CSA, including offset compensated differential amplifier and latch

- Threshold trimming by means of autozeroing (no local trimming DAC)

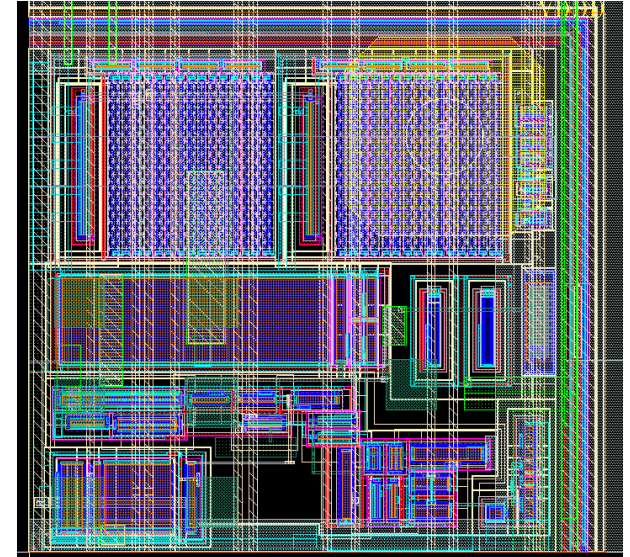- **Fast ToT counting** with latch turned into a local oscillator (100-900 MHz)
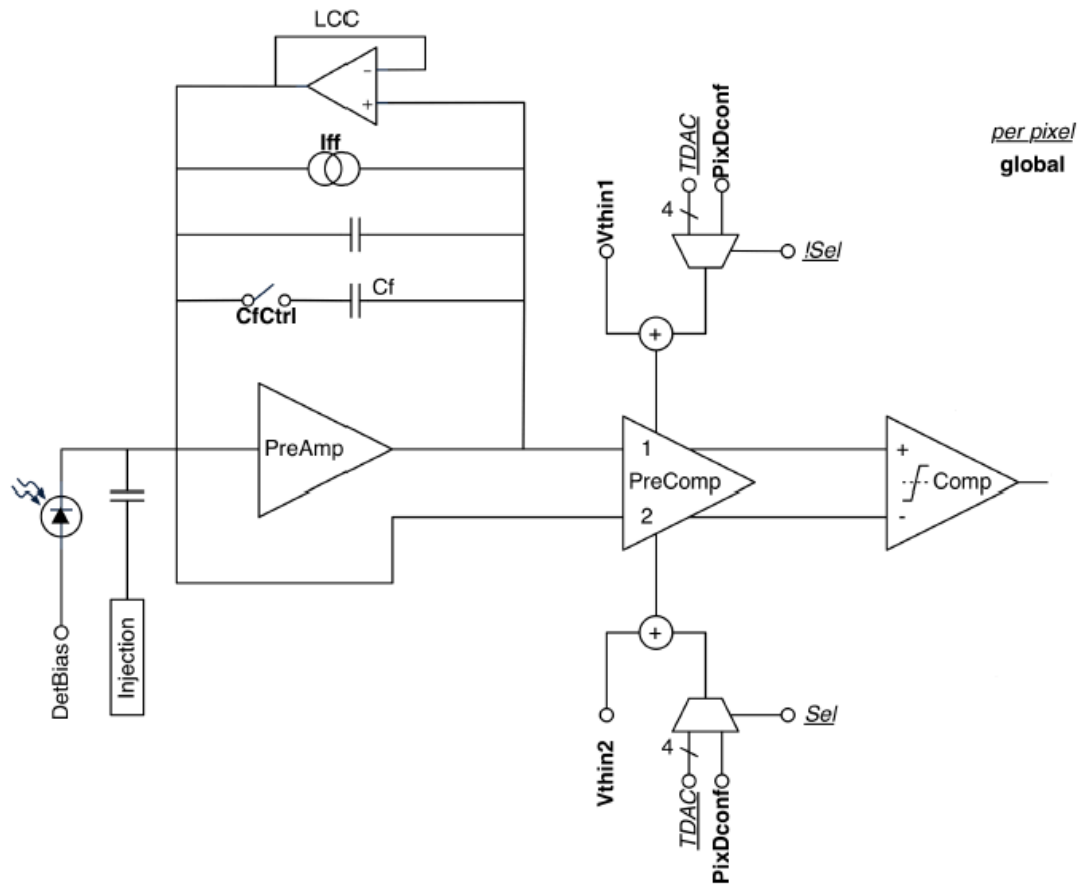
Linear Analog Front-end

- **One stage Krummenacher feedback** to comply with the expected large increase in the detector leakage current

- High speed, low power asynchronous **current comparator**

- **4 bit local DAC for threshold tuning**

Differential Analog Front-end

- **Continuous reset integrator** first stage with **DC-coupled pre-comparator stage**
- Two-stage open loop, **fully differential input comparator**
- **Leakage current compensation** a la FEI4
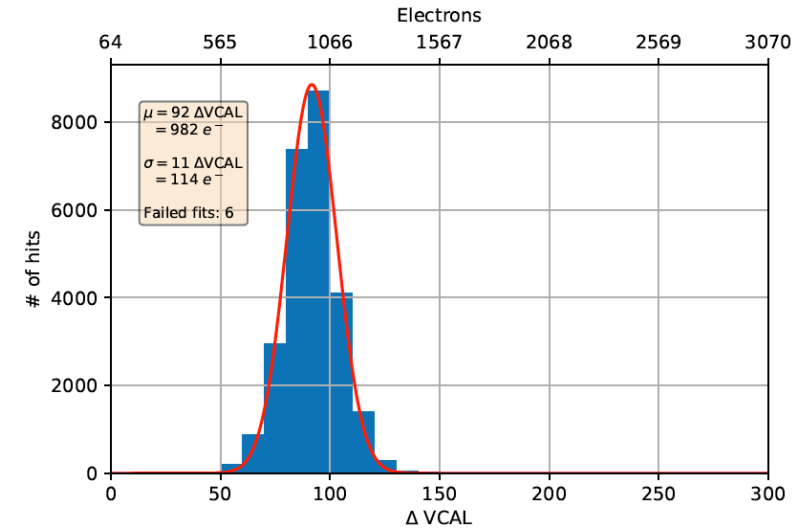- **Threshold adjusting** with global 8bit DAC and two per pixel 4bit DACs

Threshold scans

- Measures probability of discriminator to fire vs input charge

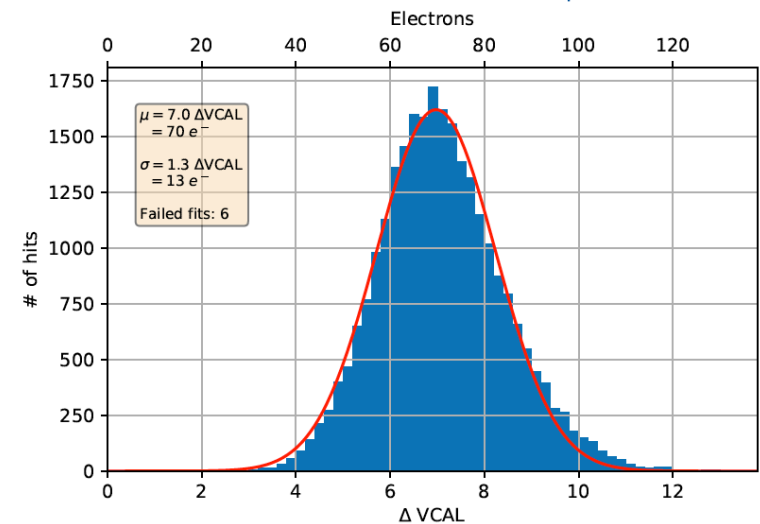- Fitting S-Curve provides measurement of threshold and noise
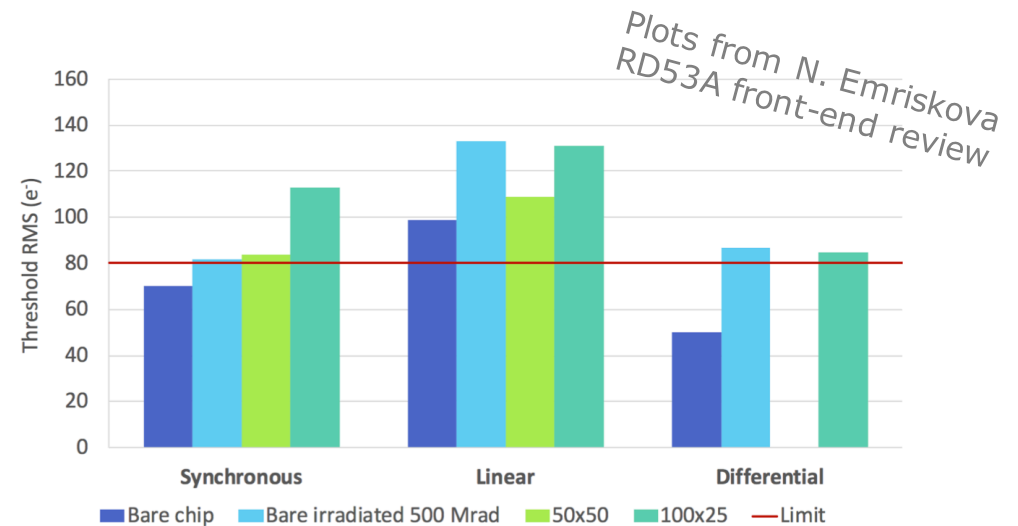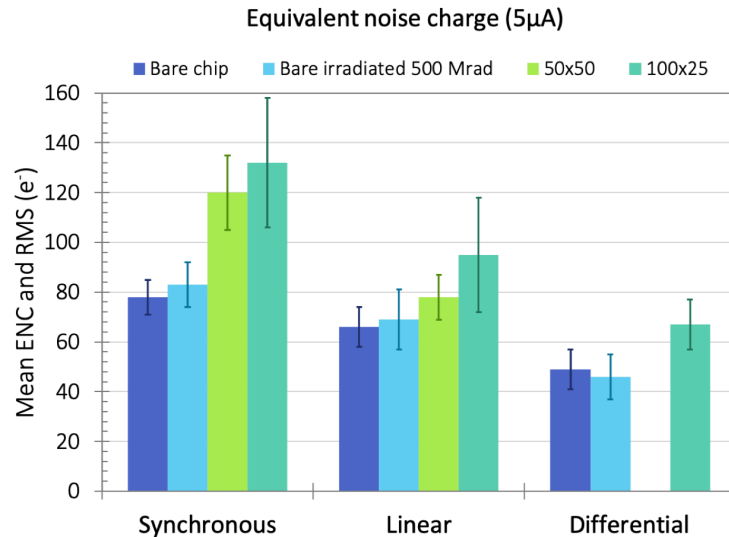

S-curves for 26063 pixel(s)
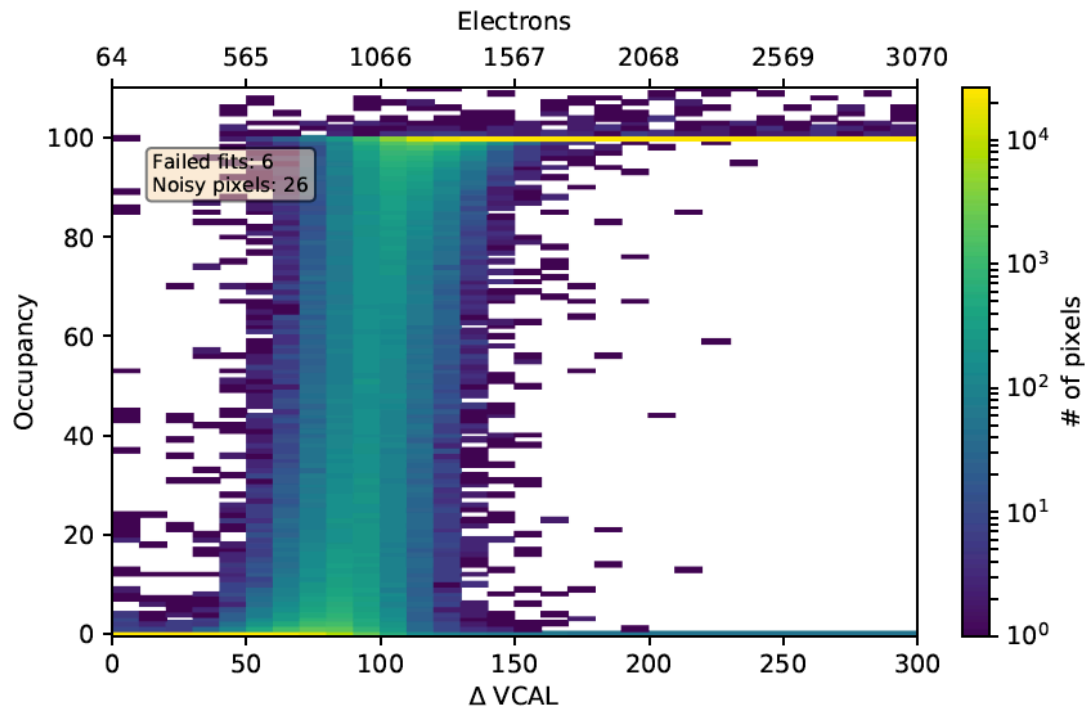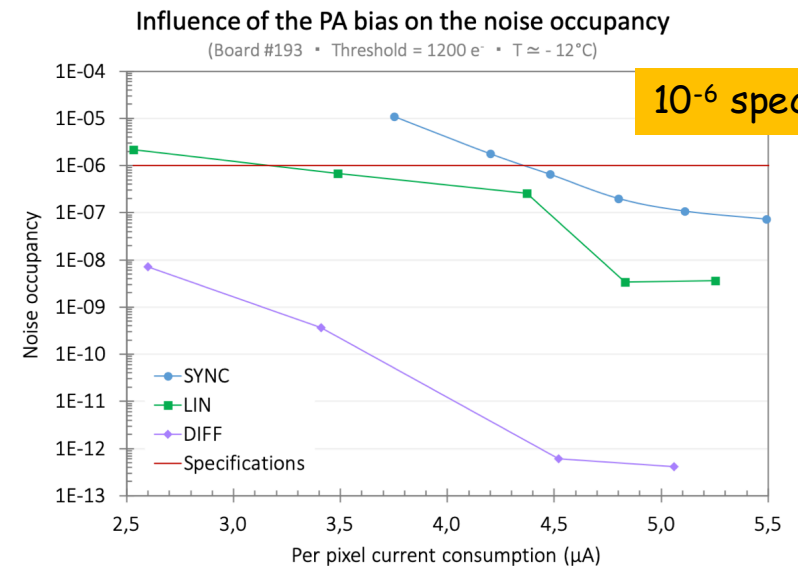

Threshold distribution for enabled pixels

$\mu = 92\ \Delta\text{VCAL}$
$= 982\ e^-$

$\sigma = 11\ \Delta\text{VCAL}$
$= 114\ e^-$

Failed fits: 6

Noise distribution for enabled pixels

$\mu = 7.0\ \Delta\text{VCAL}$
$= 70\ e^-$

$\sigma = 1.3\ \Delta\text{VCAL}$
$= 13\ e^-$

Failed fits: 6

Noise and threshold dispersion

Equivalent noise charge (5µA)

Legend: ■ Bare chip ■ Bare irradiated 500 Mrad ■ 50x50 ■ 100x25

Mean ENC and RMS (e^-) vs Synchronous, Linear, Differential

Threshold RMS (e^-) vs Synchronous, Linear, Differential

Legend: ■ Bare chip ■ Bare irradiated 500 Mrad ■ 50x50 ■ 100x25 — Limit

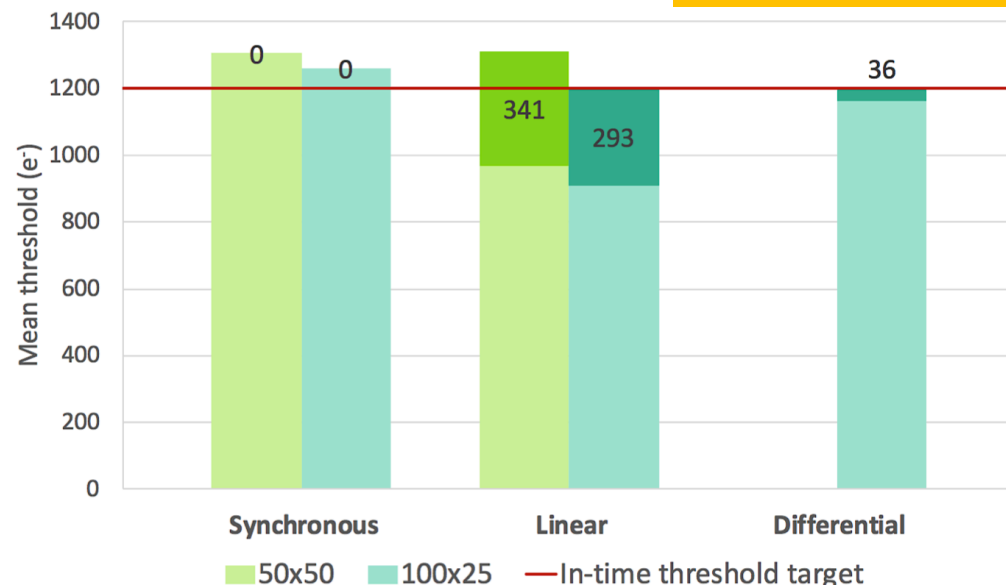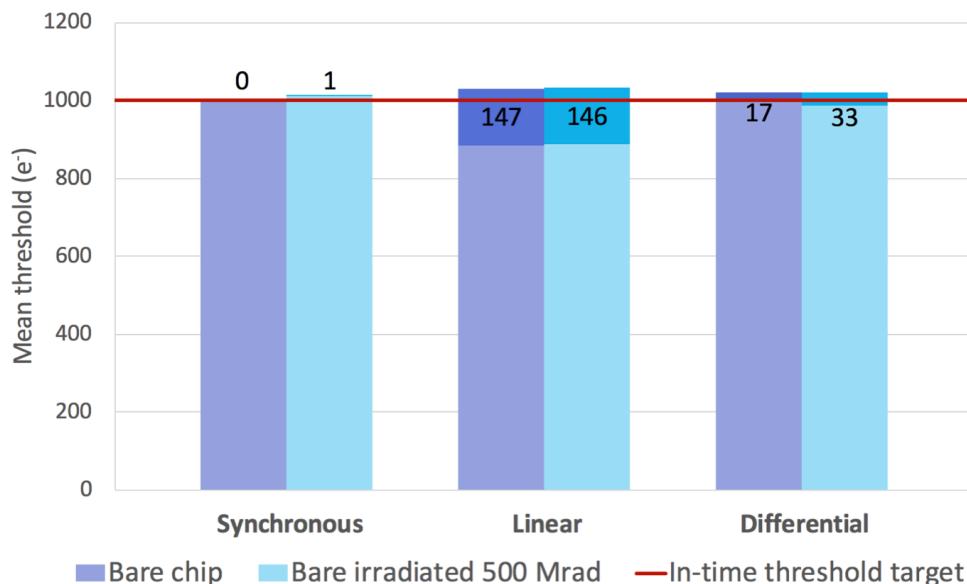*Plots from N. Emriskova RD53A front-end review*

- **Equivalent noise charge** and **threshold RMS** @ 5 uA for bare chips and assemblies:
  - 50x50 planar sensor
  - 100x25 planar sensor

- **Threshold RMS** obtained directly from extrapolated data, NOT from Gaussian fit of threshold distributions → outliers pixels might have an impact

- Both parameters have an impact on **noise occupancy** (increasing pixel current consumption also has a beneficial impact thanks to reduced ENC)

- Excellent noise occupancy performance for DIFF

Influence of the PA bias on the noise occupancy
(Board #193 · Threshold = 1200 e⁻ · T ≃ - 12°C)

10^{-6} spec

Noise occupancy vs Per pixel current consumption (µA)

Legend: SYNC, LIN, DIFF, Specifications

In-time threshold and overdrive

- **Regular threshold**: the signal charge at which the discriminator has 50% probability to fire

- 25ns BX bunches @ LHC → **in-time threshold**: the minimum signal that is detected in the right BX

- **Overdrive**: in time threshold – regular threshold

Overdrive < 600e- (RD53A spec)

Plots from N. Emriskova
RD53A front-end review

- Bare chips tuned to an in-time threshold of 1000 e- and assemblies to 1200 e-

Analog FE characterization after irradiation

- Irradiation with X-rays @c old, RD53A powered and tested/readout continuously

- Very good results - chip works, all three AFEs operated with **low thresholds**

- **Noise** for different current settings (for 0, 200, 300, 500 Mrad)

A. Dimitrievska,
RD53A talk, VCI 2019
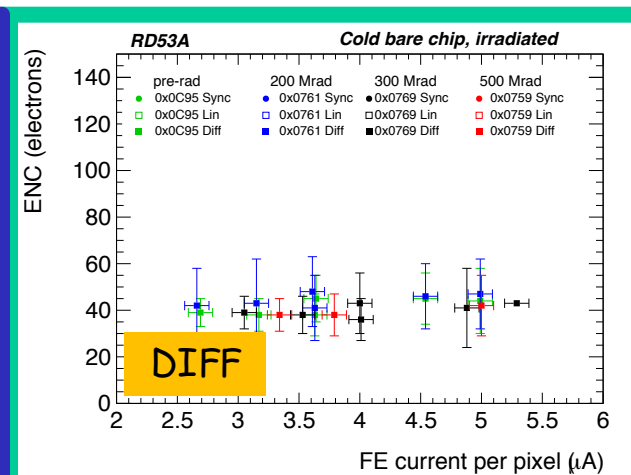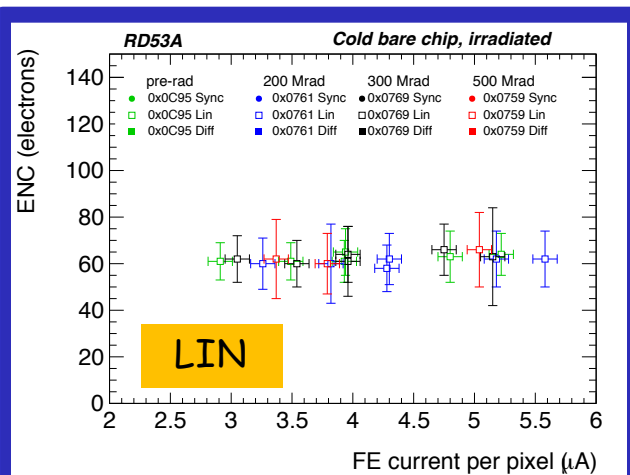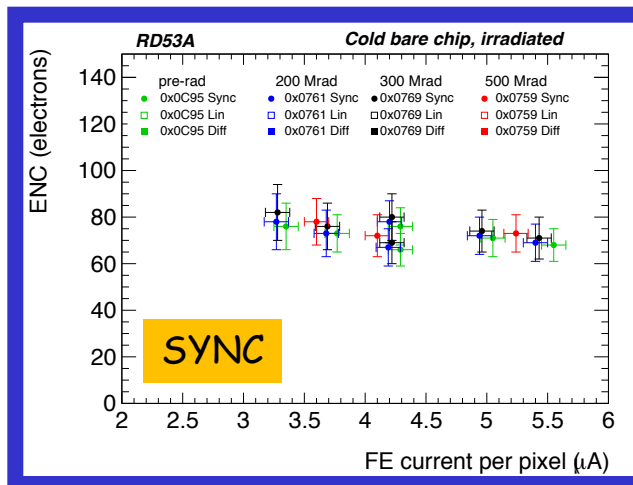
- **Threshold** distribution after 1 Grad irradiation of a bare chip
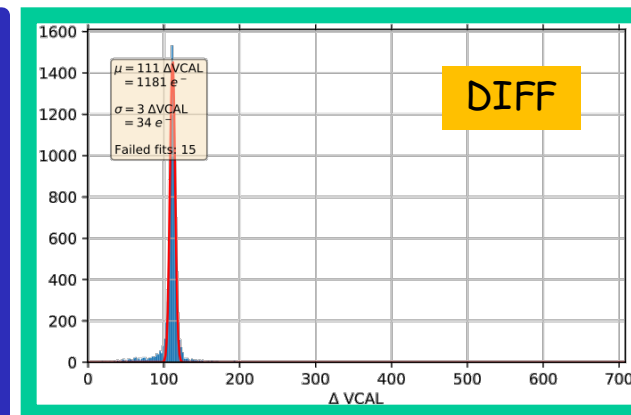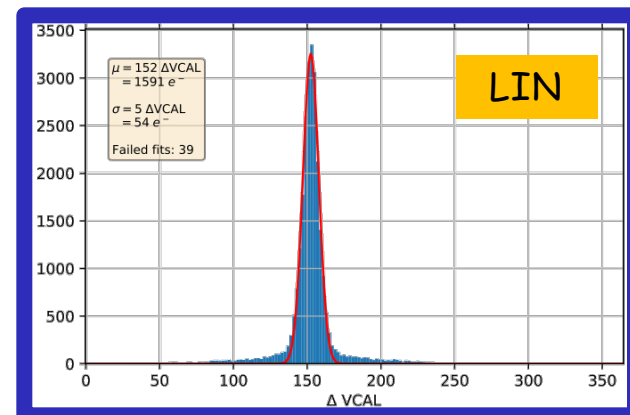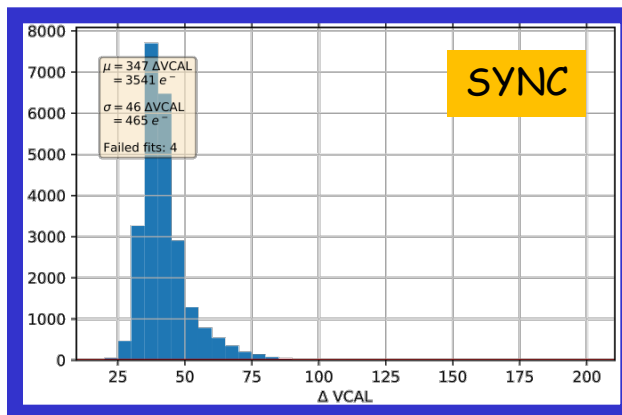
NOTE: sigma from Gaussian fit, not RMS from data

Towards RD53B

- The **success of RD53A** is the baseline for the design of the pixel readout chips of CMS and ATLAS at the HL-LHC

- **RD53B** is the common design framework for the design of the final production pixel chips for ATLAS and CMS

- ATLAS and CMS chips to be submitted in November 2019 and April 2020 as implementation of the RD53B design

- All **RD53A** elements with **bug fixes** and, where needed, **technical improvements**

- **Additional features** to be implemented (list not exhaustive)

  - Bias of edge and top "long" pixels
  - 6-to-4 bit dual slope ToT mapping
  - 80 MHz ToT counting
  - ATLAS 2-level trigger support

  - Power saving ~20%
  - Improved design for testability
  - TMR for pixel configuration
 - Optimal data formatting and compression

RD53B analog front-ends

- **RD53B: which analog front-end?**

- After a very detailed review process, a choice was made by the experiments for the analog FE:

    - ATLAS → **Differential**

    - CMS → **Linear**

- **Differential FE:**

    - Excellent **noise occupancy** performance

    - **Low power** (more critical for ATLAS)

- **Linear FE:**

    - Recommended by the review committee as the **lowest risk option**

    - Classical FE **architecture**

    - Able to cope with large **detector leakage** currents (more critical for CMS)

- ➡ **Improvements on FEs** according to reviewers comments and to experiments requirements

# Linear FE: overdrive improvement

- Weak point for the Linear FE: **large overdrive**

- Partial re-design of the comparator stage led to improvement in front-end speed
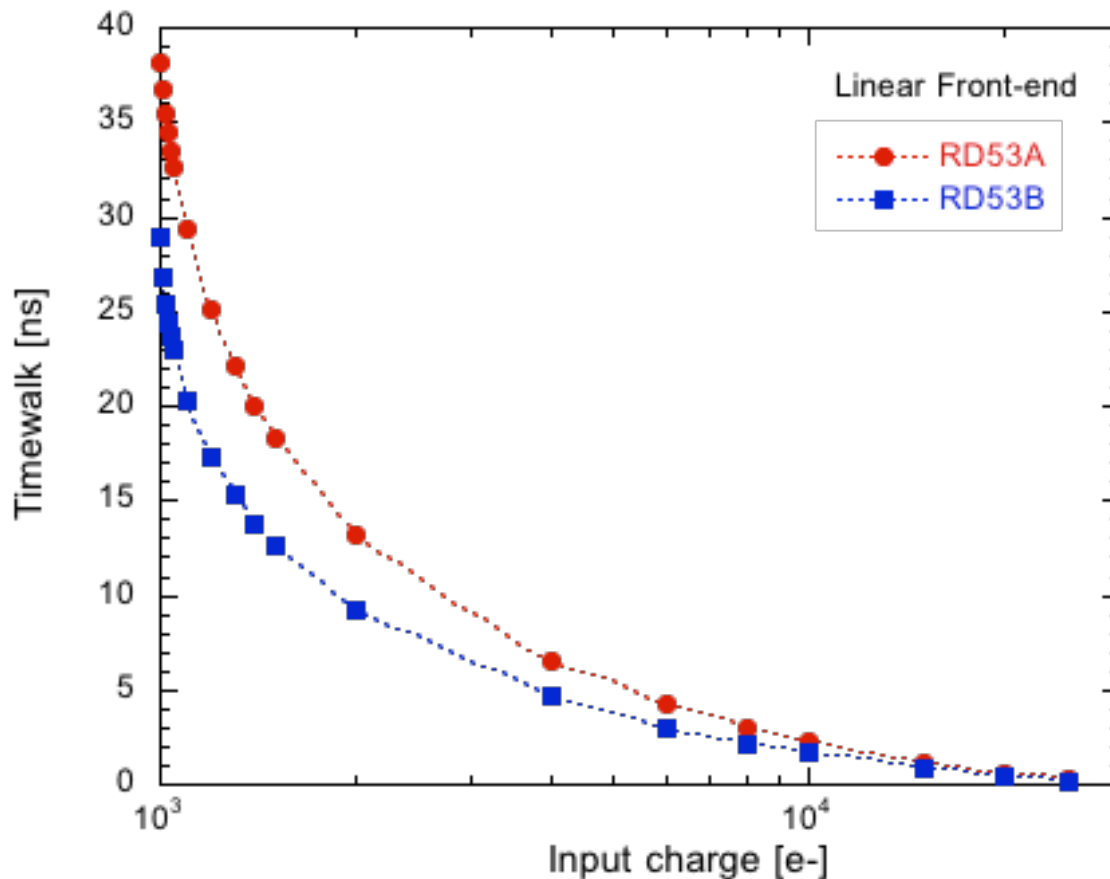
Significant **improvement in time-walk** (reduced overdrive) at the cost of a marginal increase in static current consumption
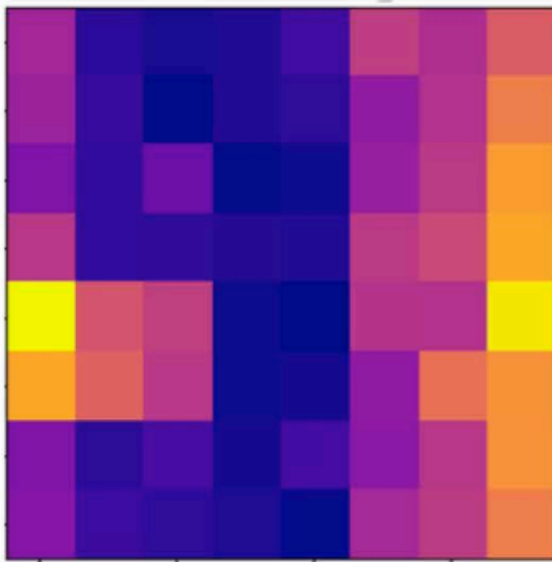
Linear FE: Trimming DAC

- Saturation effect in the LIN trimming DAC at cold (affecting TDAC dynamic range) → fixed in RD53B

  → Effects of outliers pixels should be limited for RD53B version

- Added a **5th trimming bit** to reduce threshold dispersion
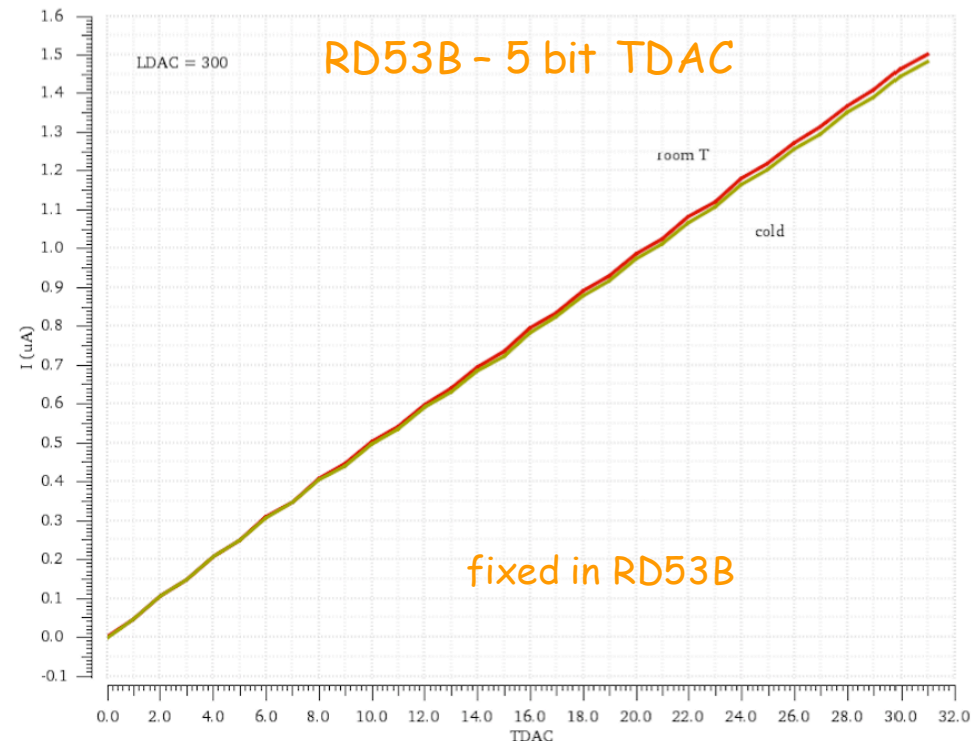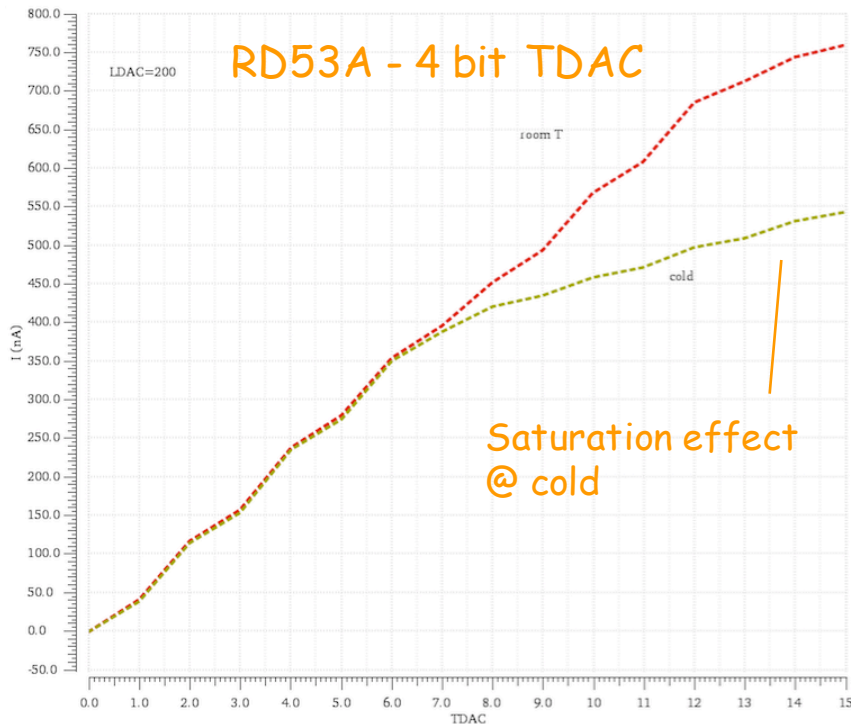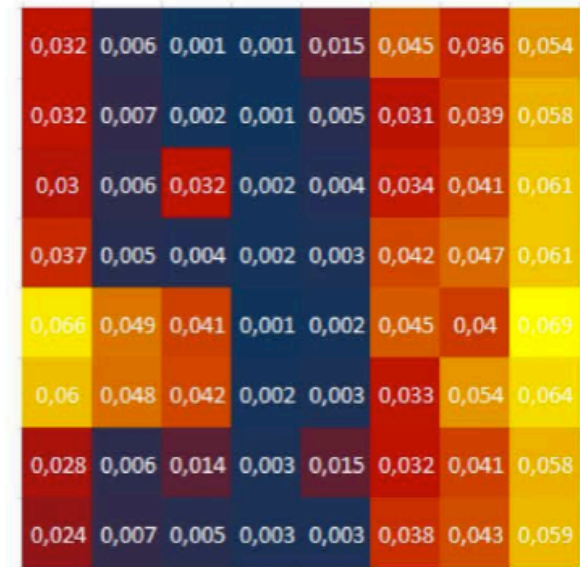
Differential front-end: comparator output routing

- Large **ToT dispersion** in initial testing of RD53A DIFF

- Missing P&R constraint on the FE hit output → Varying load capacitance on comparator output → systematic variation of delay and ToT

- Discriminator output **capacitive routing** load map matches measured ToT map of an 8x8 Core


Average TOT

0,032	0,006	0,001	0,001	0,015	0,045	0,036	0,054
0,032	0,007	0,002	0,001	0,005	0,031	0,039	0,058
0,03	0,006	0,032	0,002	0,004	0,034	0,041	0,061
0,037	0,005	0,004	0,002	0,003	0,042	0,047	0,061
0,066	0,049	0,041	0,001	0,002	0,045	0,04	0,069
0,06	0,048	0,042	0,002	0,003	0,033	0,054	0,064
0,028	0,006	0,014	0,003	0,015	0,032	0,041	0,058
0,024	0,007	0,005	0,003	0,003	0,038	0,043	0,059

Extracted *outdis* net load [pF]

- **Fixed in RD53B**: pre-placed and pre-routed buffers at the analog-digital interface

Differential front-end: hit timing

- Pixel by pixel variation of hit signal edges
- RD53A DIFF Comparator falling edge has very low slew rate resulting in large dispersion of the hit leading edge


Plots from A.Dimitrievska
FDR of the ATLAS pixel readout chip
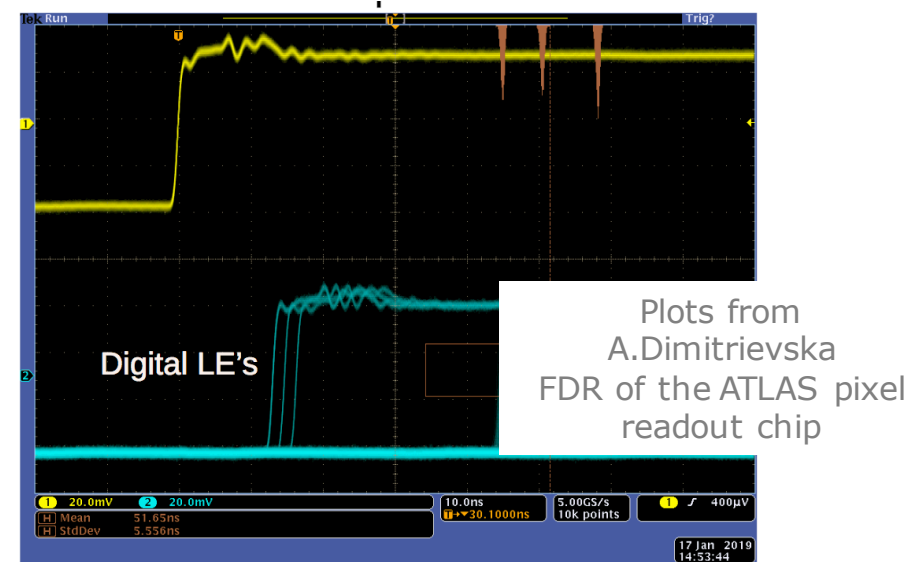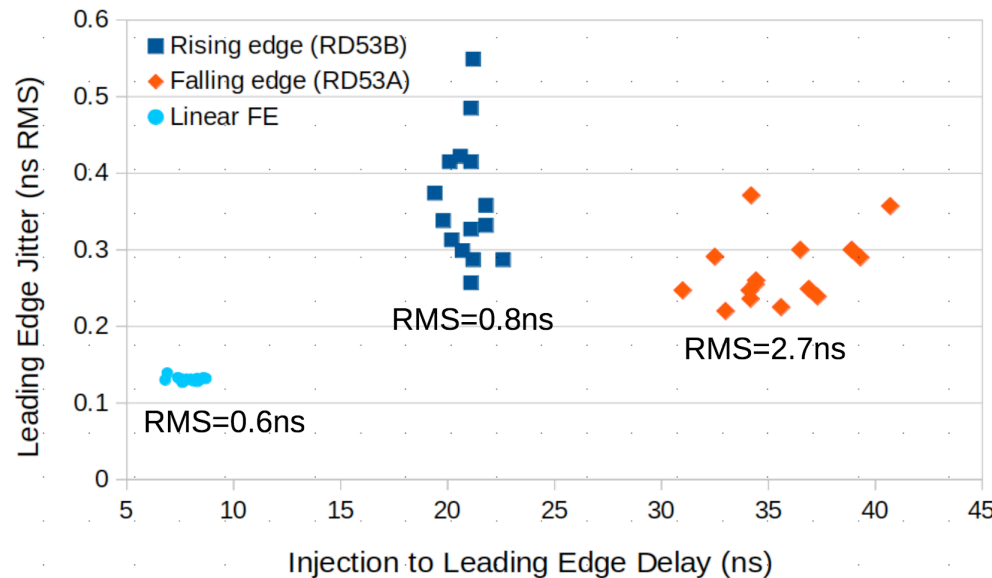
Inverting comparator polarity makes timing dispersion comparable to LIN front-end

Conclusions

- **RD53A** chips have been **thoroughly characterized** during the last two years, with striking good results (also after irradiation)

- After a detailed review process the **Differential** (ATLAS) and the **Linear** (CMS) front-end have been chosen for the implementation of the final production chips

- Final ATLAS/CMS chips will be designed in a common design framework called **RD53B**

- Improvements and few **fixes** to RD53A have been found and are being implemented in RD53B

- ATLAS and CMS chips are planned to be **submitted in November 2019 and April 2020** as implementation of the RD53B design

Backup

SYNC front-end: preamplifier response
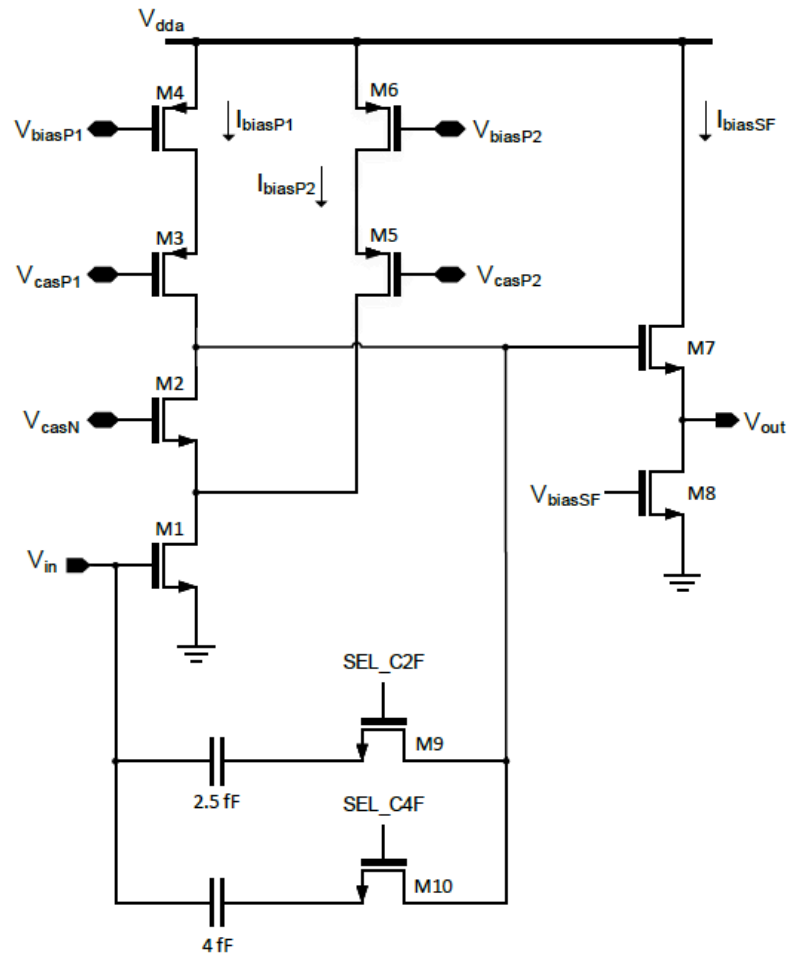
Preamplifier output (TOP PAD frame)
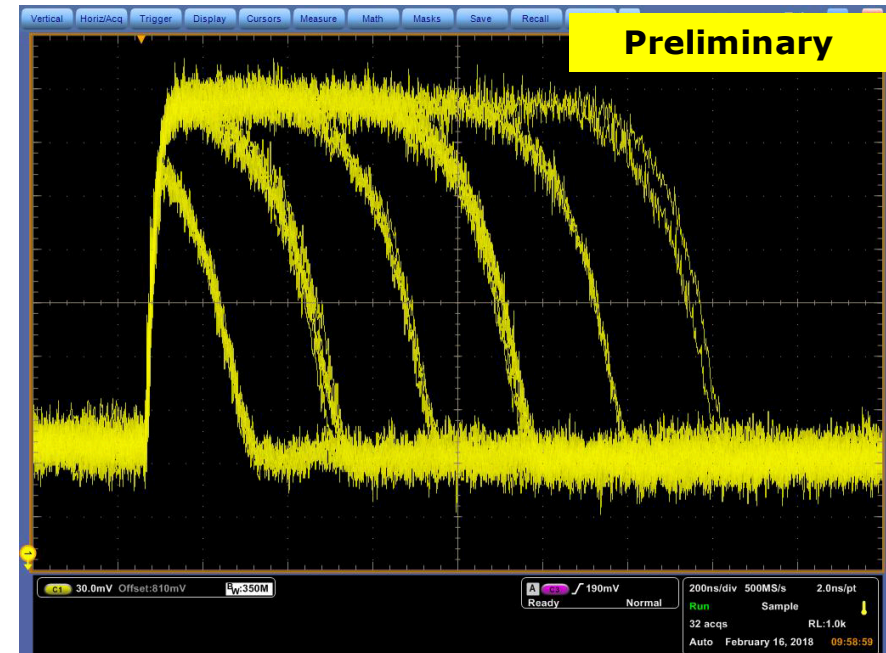
- Telescopic cascode with current splitting and source follower
- Two switches controlling the feedback capacitance value
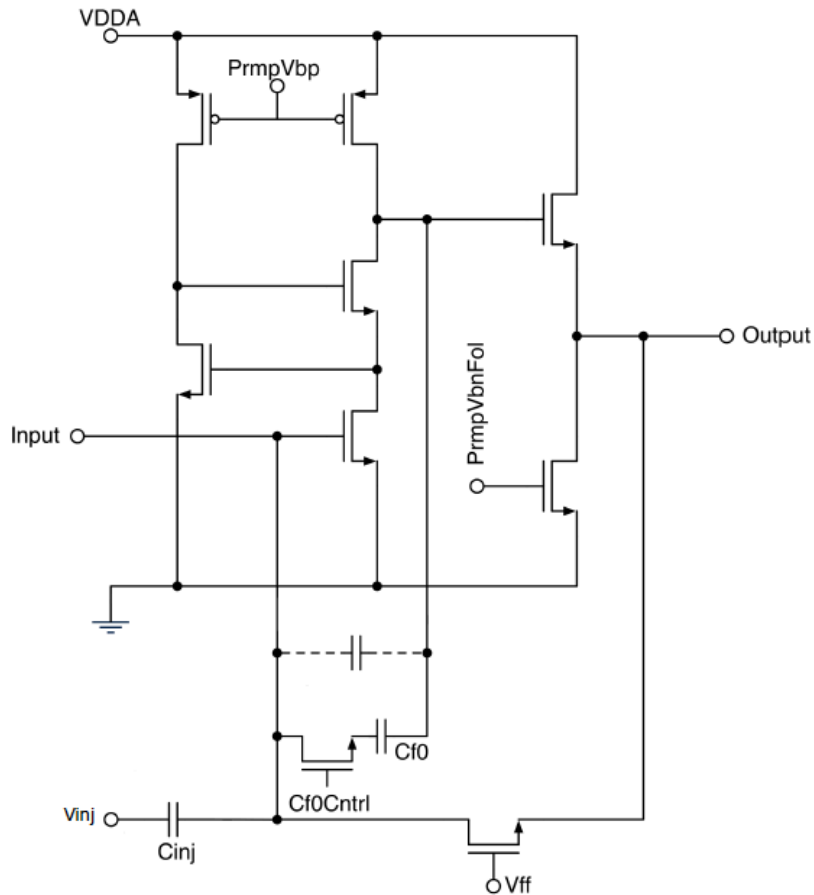
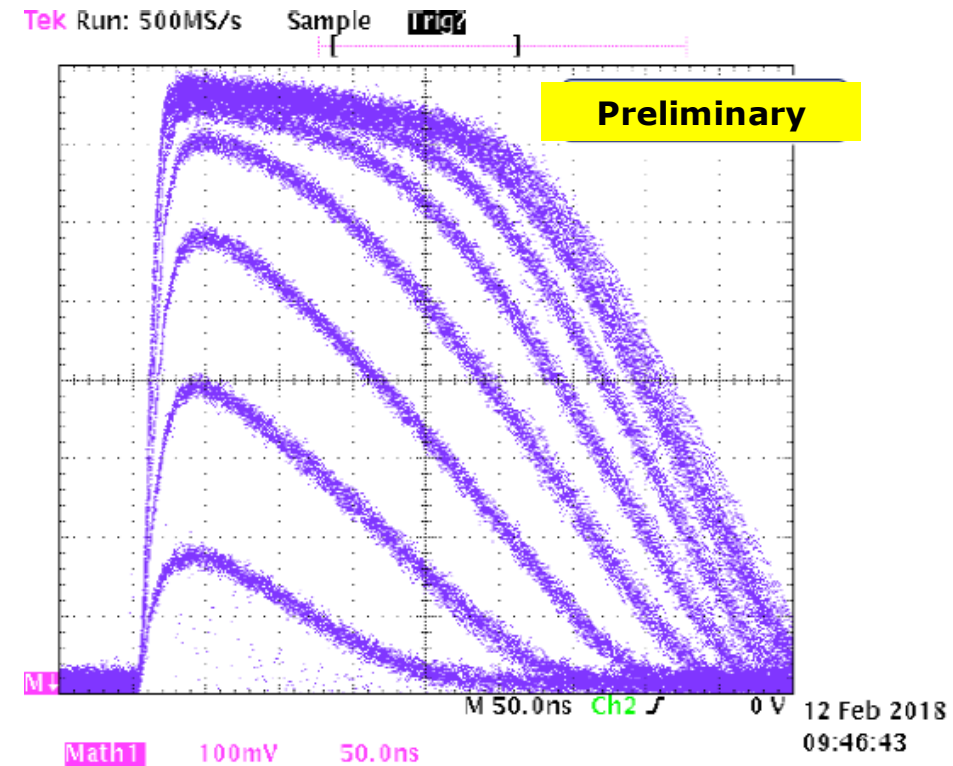# LIN front-end: preamplifier response
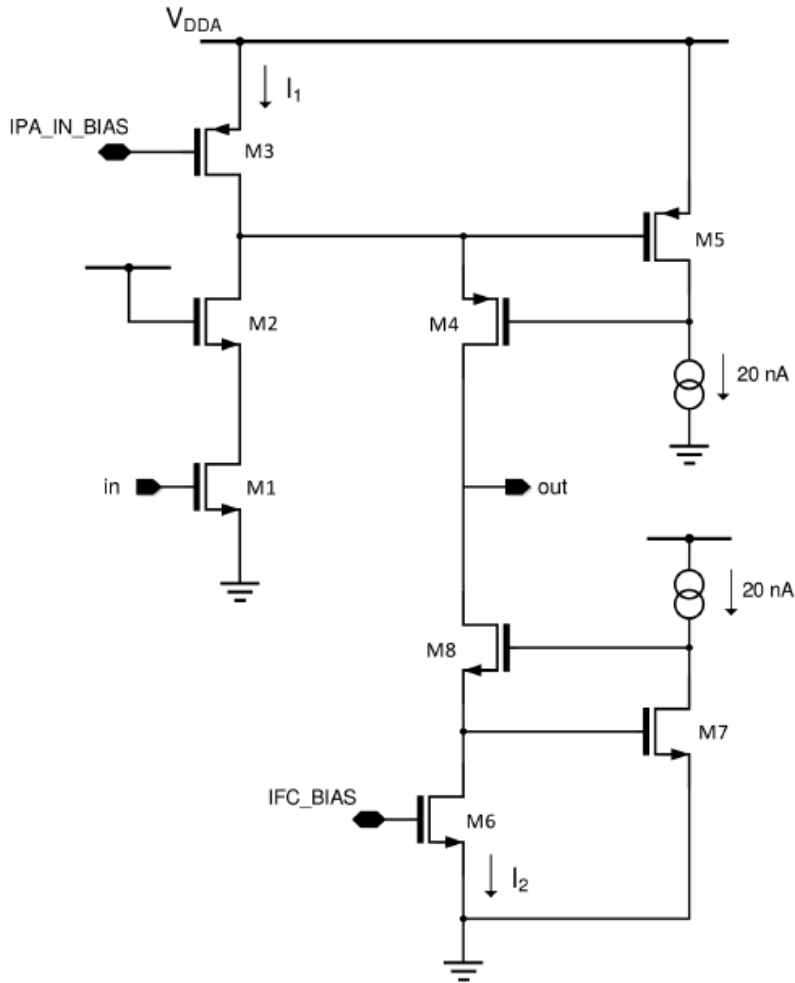
Preamplifier output (TOP PAD frame)
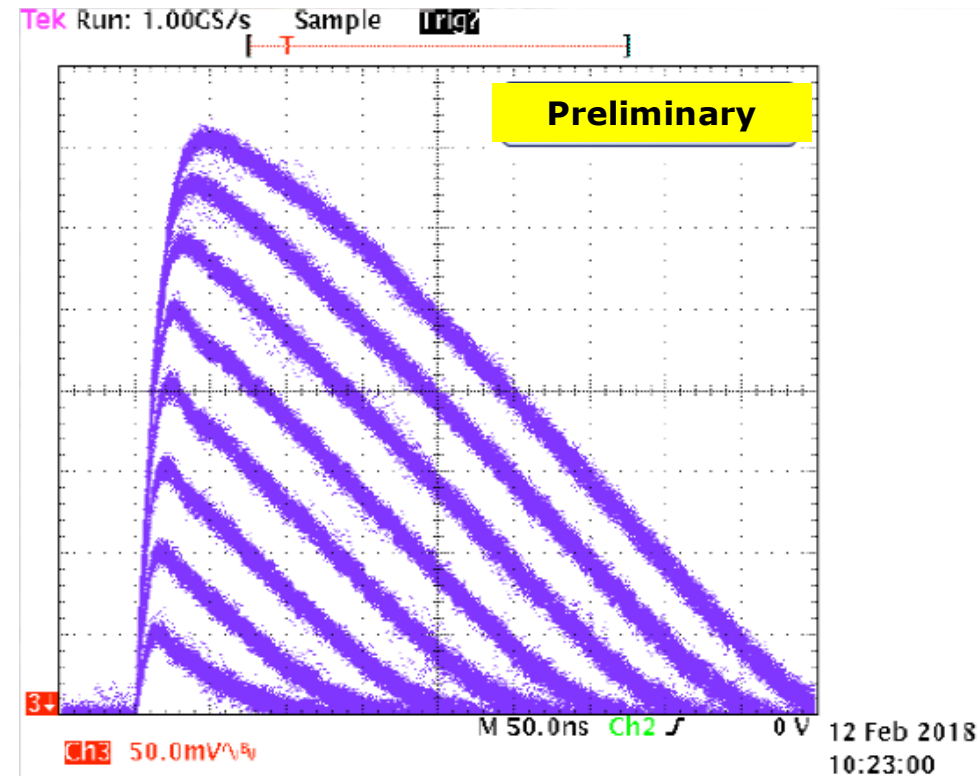
- Gain stage based on a **folded cascode** configuration (~3 uA absorbed current) with a regulated cascode load

DIFF front-end: preamplifier response

Preamplifier output (TOP PAD frame)

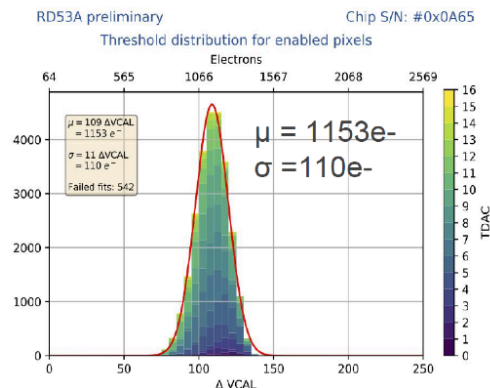- Straight regulated cascode architecture with NMOS input transistor in weak inversion

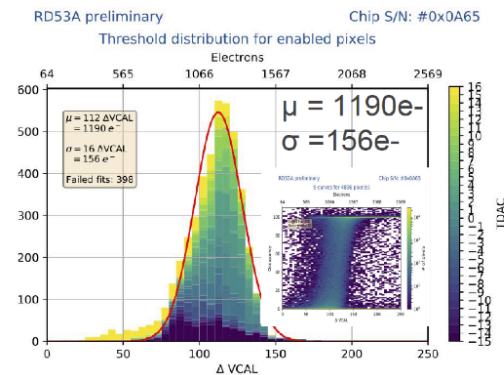# AFE vs Leakage current

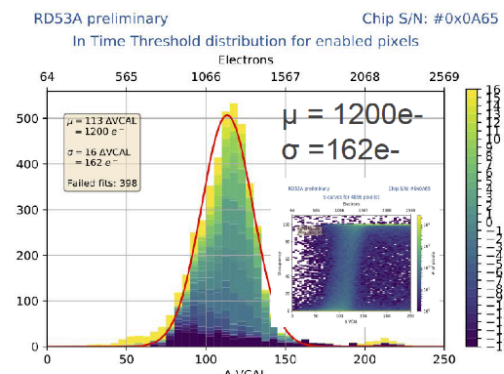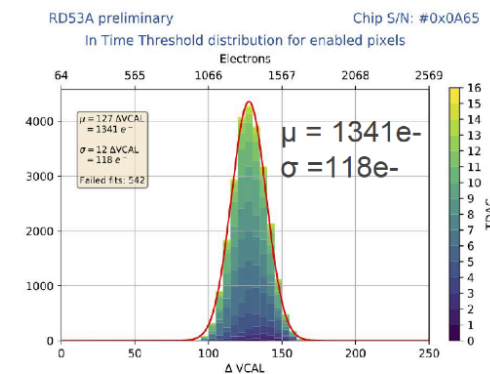## Threshold Dispersion 10nA / per pixel
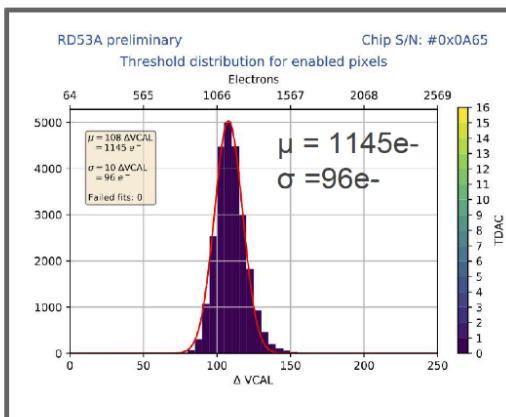
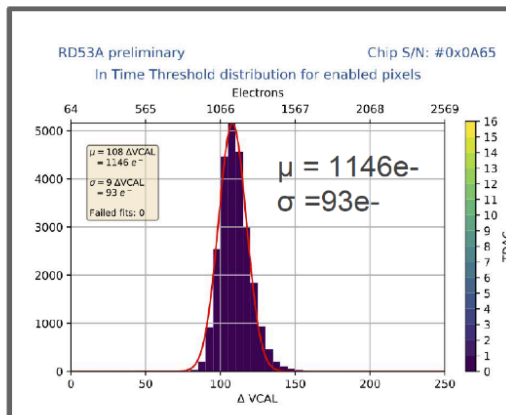| SYNC FE	LIN FE	DIFF FE

Vth= 135, IBIAS_KRUM_SYNC=50   Vth= 367, KRUM_CURR_LIN=26   Vth1=113, Vth2=0, VFF= 64, LCC=400, PreCompDiff=512

Plots from M.I. Lezki
RD53A front-end review

Measurements with Modules:

- Test beam done by RD53 to understand chip more than the sensors
  - Preliminary studies show similar results for the three FEs

- Now several test-beam have been done (AIDA-2020, ATLAS, CMS) by the sensor community to study planar and 3D silicon sensors. From October also irradiated modules have started to be studied.
  - Low thresholds (~800e- to 1200e-) are normally achieved
  - Lot of results are coming
  - Important learning curve for everybody in the sensor and RD53 community : tuning of FE is important and has to be optimised depending on the detector and its conditions


L.Demaria - Results from RD53A and perspectives -

TREDI 2019 - Trento 25 Feb 2019
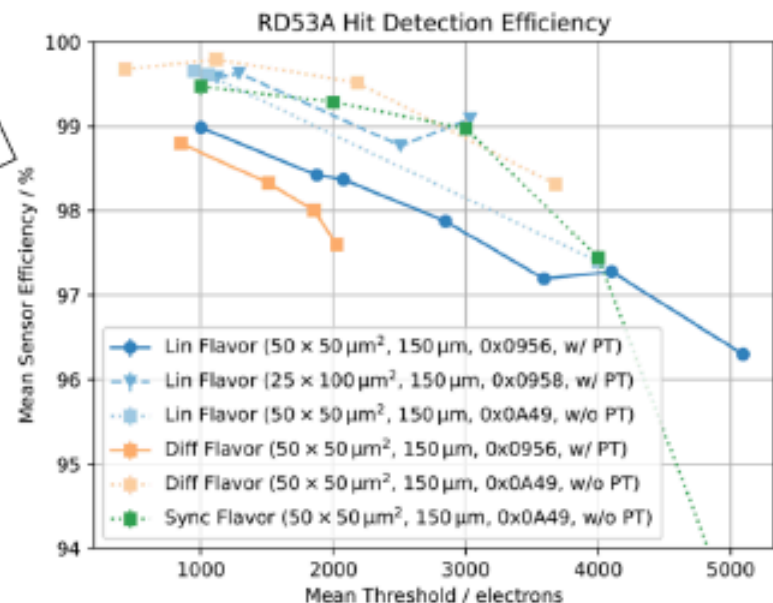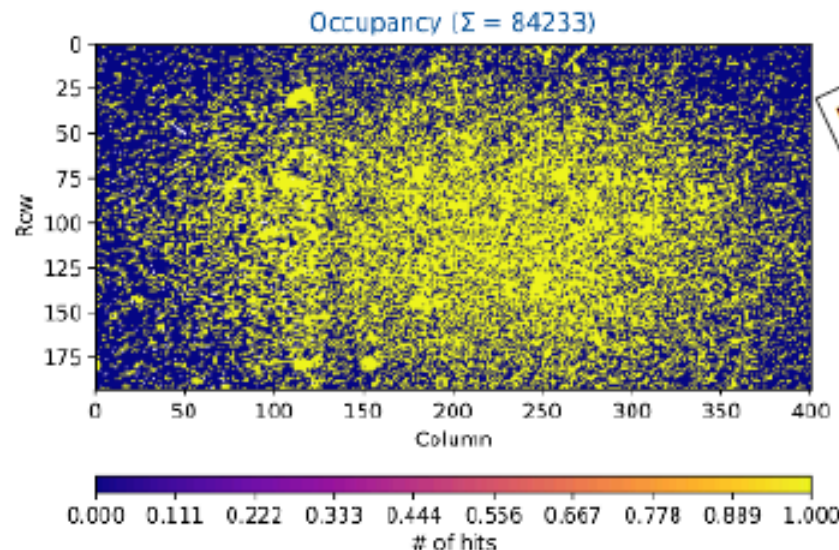
Calibration circuit (in-pixel)

- Local generation of the analog test pulse starting from 2 defined DC voltages CAL_HI and CAL_MI distributed to all pixels and a 3rd level (local GND)

- Two operation modes which allow to generate two consecutive signals of the same polarity or to inject different charges in neighboring pixels at the same time
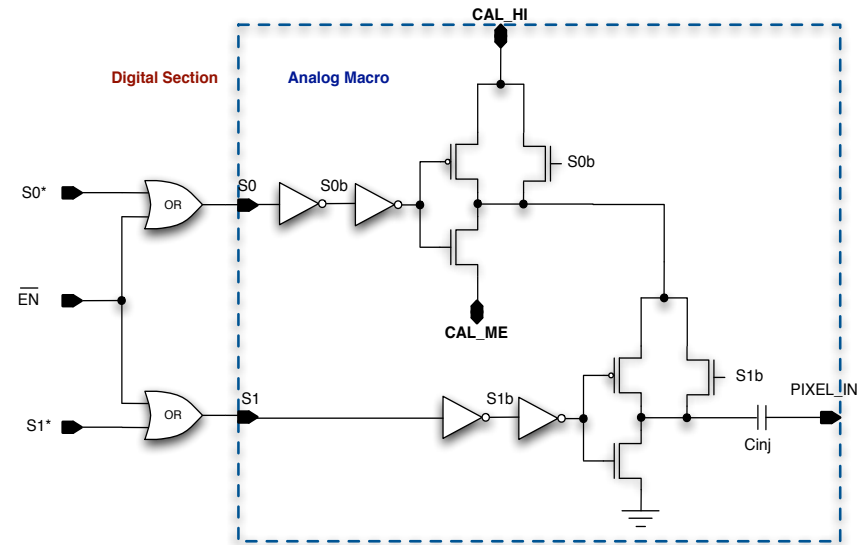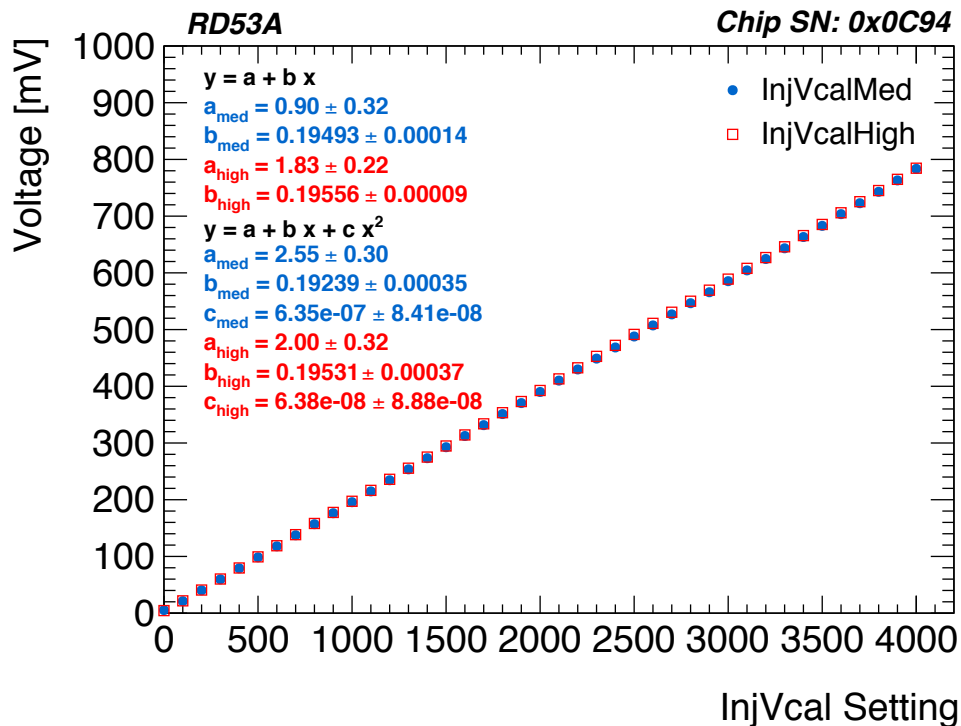
- **Injection DACs fully functional**

- Assuming 8.5fF in-pixel injection cap –> 10.08 e-/DAC

  - Close to simulation results (~11 e-/DAC)

- All biasing DACs (can be monitored using internal 12-bit ADC and are accessible on a dedicated pad) work fine