[CHIPS]

The Timepix4 chip and its design approach

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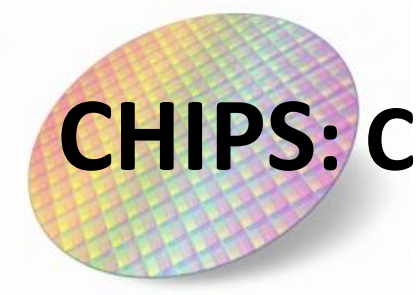
15th October 2019

Support Services in the future



CHIPS: CERN-HEP IC design Platform & Services

- Strengthening Foundry Services and Technical Support in CERN EP-ESE-ME
- Meeting the challenges of present and future CMOS designs in the HEP community and at CERN
- Announced to the HEP community at the MUG meeting at TWEPP 2019
- *Slides from M.Campbell and K.Kloukinas*

ASIC design support for HEP

- CERN evaluates and qualifies silicon technology processes
- Provide support to HEP community for selected technologies
  - Technology Support
    - Develop ASIC design platforms for common use
    - Develop specific macro blocks of general use
    - Organize distribution and maintenance
    - Provide technology support to designers
  - Foundry Access Services
    - Establish Commercial Contracts with silicon vendors
    - Develop productive working relationships
    - Establish NDAs that allows for collaborative work
    - Organize & coordinate silicon fabrication

ASICs for HL-LHC Upgrades

- List of ASICs for the upgrade programmes

ALICE (and NA62)
SAMPA, ALPIDE, FEERIC, Non-LHC, TDCpix (NA62)
LHCb
VELO – VeloPix, Upstream Tracker – SALT, RICH – CLARO, SciFi – PACIFIC, CALO – ICECAL, MUON - nSYNC
ATLAS
ITK Pixel, Monolithic Pixel, ITK strips, Lar Calorimeter, HGTD, Muon NSW, Muon MDT, Muon TGC, Muon RPC, Trigger-DAQ
CMS
GEM VFAT3, OT CBC, OT CIC, OT MPA, OT SSA, EB CATIA, EB LITE-DTU, IT ROC, EC Si ROC (HGCROC, H2GCROC), EC TCON, ECON, DCON, EC LDO, BTL TOFHIR, BTL ALDO2, ETL ETROC, CMS CFO
CERN common ASICs
lpGBT, LDQ10, lpGBTIA, GBTX, GBT-SCA, GBLD, GBTIA, FEAST2, bPOL12V, bPOL2V5, linPOL12V, RD53

ASIC design Challenges

- 67 ASICs are being developed
  - Most of them comply with development schedules
  - Many were delayed or required multiple prototyping iterations
  - Few are problematic and might have serious repercussions on the physics programs of the experiments

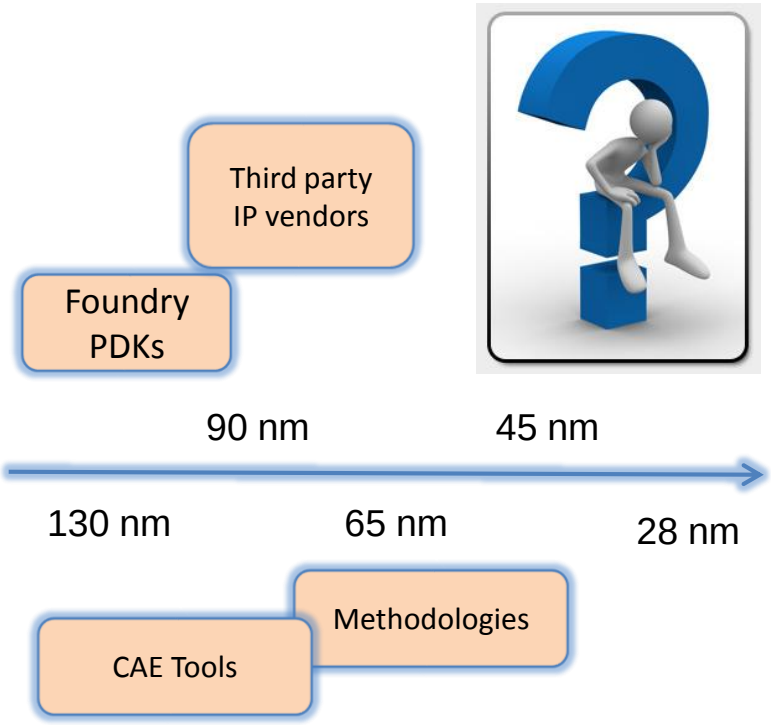
- The CERN SPC[1] highlighted at its December 2018 meeting (among other things) the challenges associated with ASIC developments in the HEP community and *asked for a coherent plan for dealing with these problems*

- What primarily emerged, is that the complexity of the CMOS processes being used is high and will increase in the future and along with that the complexity of our designs

[1]SPC: Scientific Policy Committee
an advisory body to CERN council
https://council.web.cern.ch/en/content/welcome-scientific-policy-committee

Present and Future Challenges

- Technology Challenges
  - Complex deep-submicron technologies
  - Powerful and Flexible CAE Tools
    but complicated to use
- Design Challenges
  - Designs of increased complexity (SOC)
  - Mixed Signal designs & IP reuse
  - Vendor IP libraries prepared for digital flows
  - Radiation Tolerance
- Productivity Requirements
  - Large, fragmented, multinational design teams
  - Designers with different levels of expertise
  - Work on common design projects
  - Relative low production:
    - Expensive prototyping technologies
    - Importance of 1st silicon success !



Complex Design Manufacturing Rules

DRC deck file line count:

250nm: 5,300 lines
130nm: 13,500 lines
90nm: 38,400 lines
65nm: 89,300 lines

Facing the Challenges

- The ***Digital on Top design implementation*** and ***System Level Verification methodologies*** must be adopted systematically to avoid expensive and time-consuming errors even if this implies a significant increase in design time and resources

- The layout of analog blocks for ***radiation hardness*** (and Single Event Upset resilience) becomes increasingly challenging and deep expertise is required

- The ***monolithic integration*** of sensor and electronics in a single substrate holds great potential for low material budget tracking detectors. However, the added ***complexity of shielding the sensor*** from the active readout electronics requires deep modelling expertise

- As the design ***community remains geographically scattered and smaller groups*** may struggle to cope with the new design flows CERN could strengthen training and support

CHIPS Action Plan

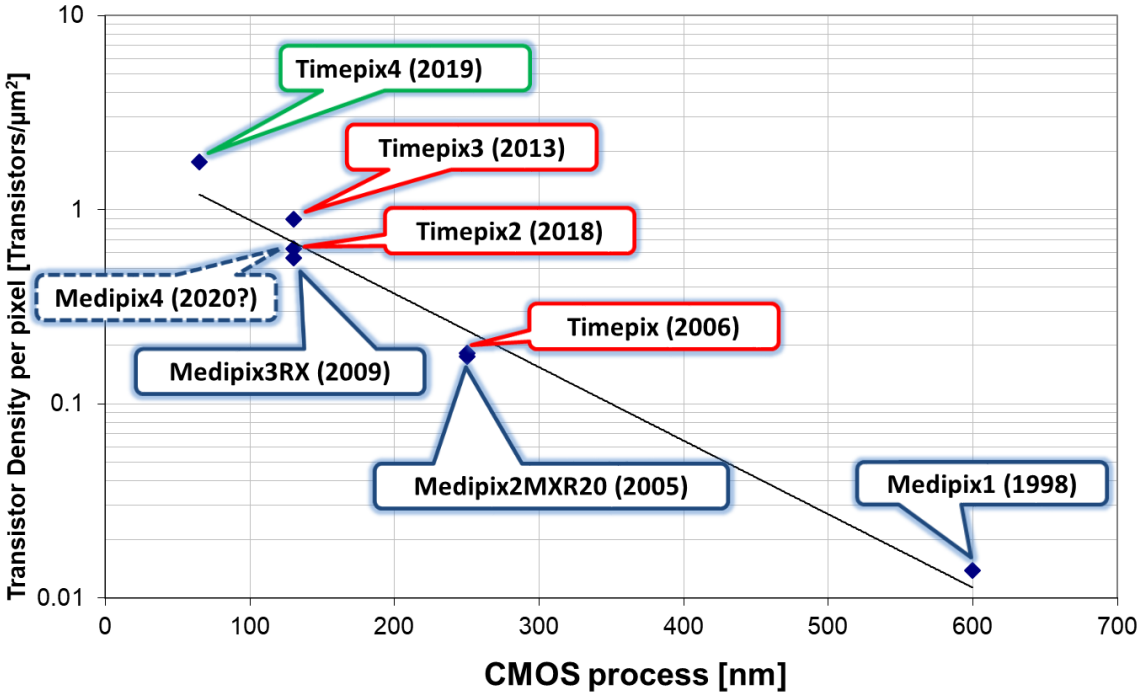
1) **Involve a broader spectrum of experienced practitioners in design support:**
   - At present a small core team in EP-ESE-ME provides support. It is proposed to redistribute the technical support tasks more uniformly across the experienced designers in EP-ESE-ME. For each step in the design flow one or two specialists will be identified and these will be tasked with supporting outside groups. Such support can only be provided by experienced practitioners
2) **Subcontract specialised tasks:**
   - Reinforce contracts with companies able to give punctual help with particular issues related to the tools and design flow. These facilities should be available both to CERN engineers and to members of the community. As with all such external contracts there should be one person responsible (of course with a back-up) to act as intermediary between the company and the designers
3) **Train and coach:**
   - Continue to organize formal training sessions to expose designers to the latest tools and, in particular, to educate them in the use of the common design platform.
   - Furthermore, host designers from the HEP community at CERN in each case for some months per year. Some ‘hot desks’ could be allocated for such activities

CHIPS Implementation Workplan

- The CHIPS implementation work plan is currently being drafted and will become available towards the end of 2019
- The workplan will cover a five year period: 2020-2024
- The ramping up of the new service and the level of support is a function of the additional resources that will be made available
  - First positions will start in January 2020

TIMEPIX4

Medipix4 Collaboration (from 2016)



- CEA, Paris, France
- CERN, Geneva, Switzerland,
- DESY-Hamburg, Germany
- Diamond Light Source, Oxfordshire, England, UK
- IEAP, Czech Technical University, Prague, Czech Republic
- JINR, Dubna, Russian Federation
- NIKHEF, Amsterdam, The Netherlands
- University of California, Berkeley, USA
- University of Houston, USA
- University of Maastricht, The Netherlands
- University of Canterbury, New Zealand
- University of Oxford, England, UK
- University of Geneva, Switzerland
- IFAE, Barcelona, Spain
- University of Glasgow, UK

Timepix4: A 4-side tillable large single threshold particle tracking detector chip with improved energy and time resolution and with high-rate imaging capabilities

15 members

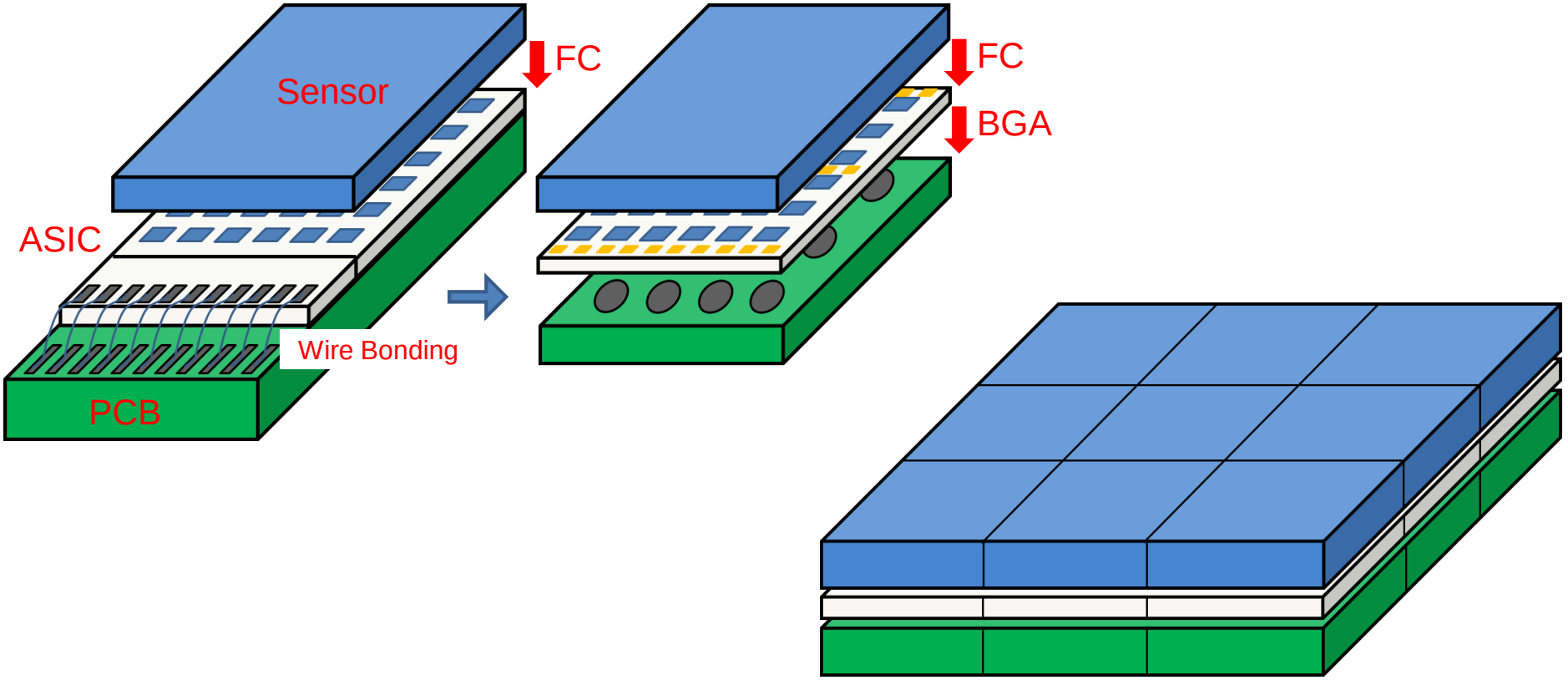
Timepix3 → Timepix4

			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448	**3.5x**
Sensitive area			1.98 cm^2	6.94 cm^2	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	**33%**
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**	**8x**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s	**5x**
TOT energy resolution			< 2KeV	< **1Kev**	**2x**
Time binning resolution			1.56ns	**195ps**	**8x**
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)**	
Target global minimum threshold			<500 e^-	<500 e^-	

Timepix4 Design Strategy

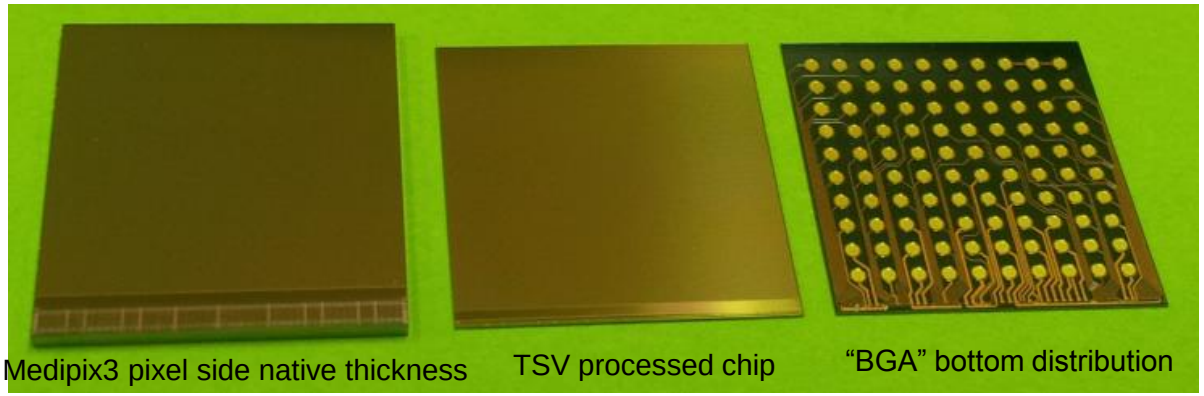
- Design specifications closed 2 years ago
- Top level chip floorplan realized at a very early stage
- Use the digital on top flow
  - All analog blocks designed as “islands” inside digital flow
    - Required careful physical and functional characterization before integration
  - Digital logic is used as “glue” between analog blocks
- Use of UVM as system level functional verification
  - Allows full chip top level simulations → Impossible using analog simulators
- Extensive use of repositories (GitLab, ClioSoft) allowed versioning and save file sharing between the design team
- Total design time of ~3 years with 8 engineers → ~12.5 FTE

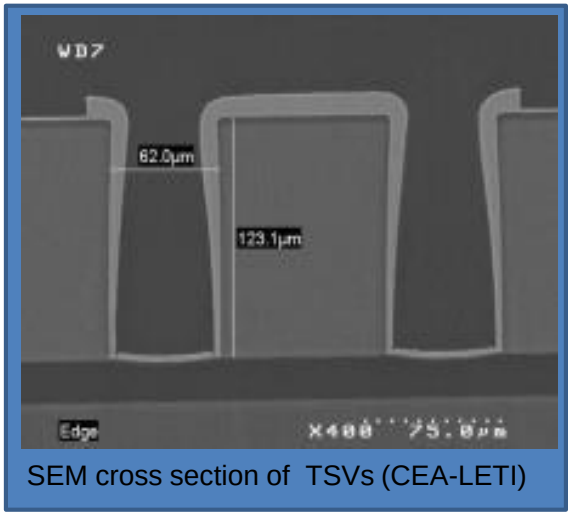
4-side buttable pixel arrangement



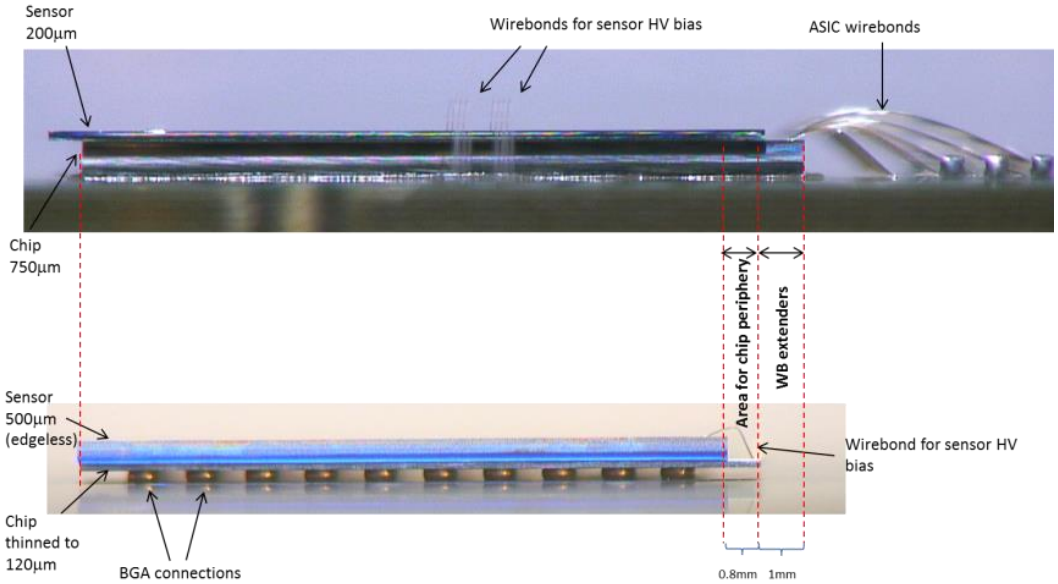
- Target to build **large area detectors** by combining smaller modules
- The through-silicon vias (TSVs) is the key technology for this paradigm shift

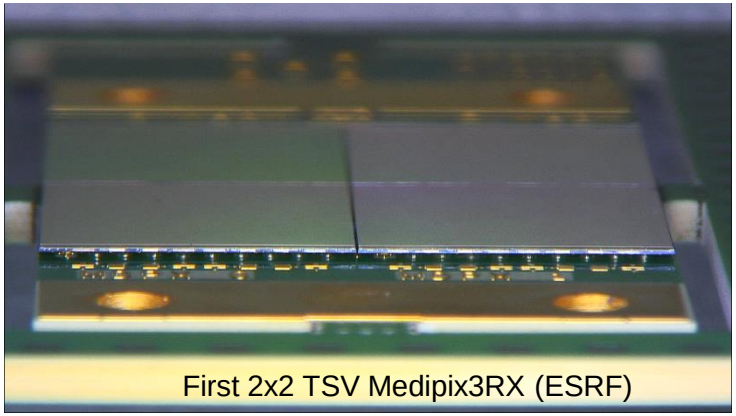
TSV Process





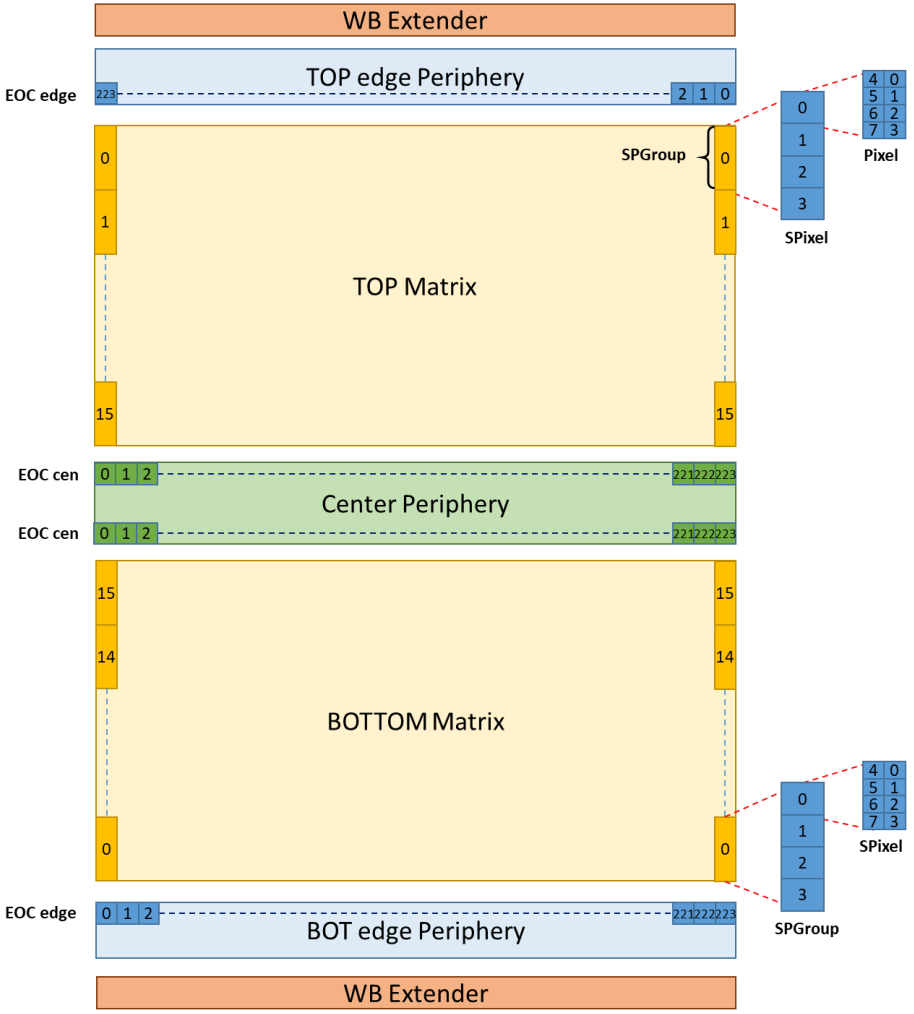
SEM cross section of TSVs (CEA-LETI)




First 2x2 TSV Medipix3RX (ESRF)

Timepix4 floorplan arrangement

- 512 x 448 of 55 x 55 µm pixels
- 3 “hidden” peripheries with TSV (Through-Silicon-Vias):
  - TOP, BOTTOM Edge: Data Readout (8x 10 Gbps Serializers)
  - CENTER: SC, Analog Blocks (DACs, ADC, Band-Gaps…)
- On-chip bump to pixel redistribution layer (RDL)
- Chip size:
  - With WB (wirebonds extenders): 29.96 mm x 24.7 mm
  - Without WB : 28.22 mm x 24.7 mm → **>99.5%** active area
- Control architecture allows to operated Timepix4 from any of the 3 peripheries:
  - i2C protocol
  - Custom Slow Control protocol
  - Interface to DAQ:
    - Through 3xTSVs
    - Through 2xWB
- Fast readout requires at least 1 serial link enabled in each edge periphery:
  - Serial links are highly configurable 40MBps → 10GBps



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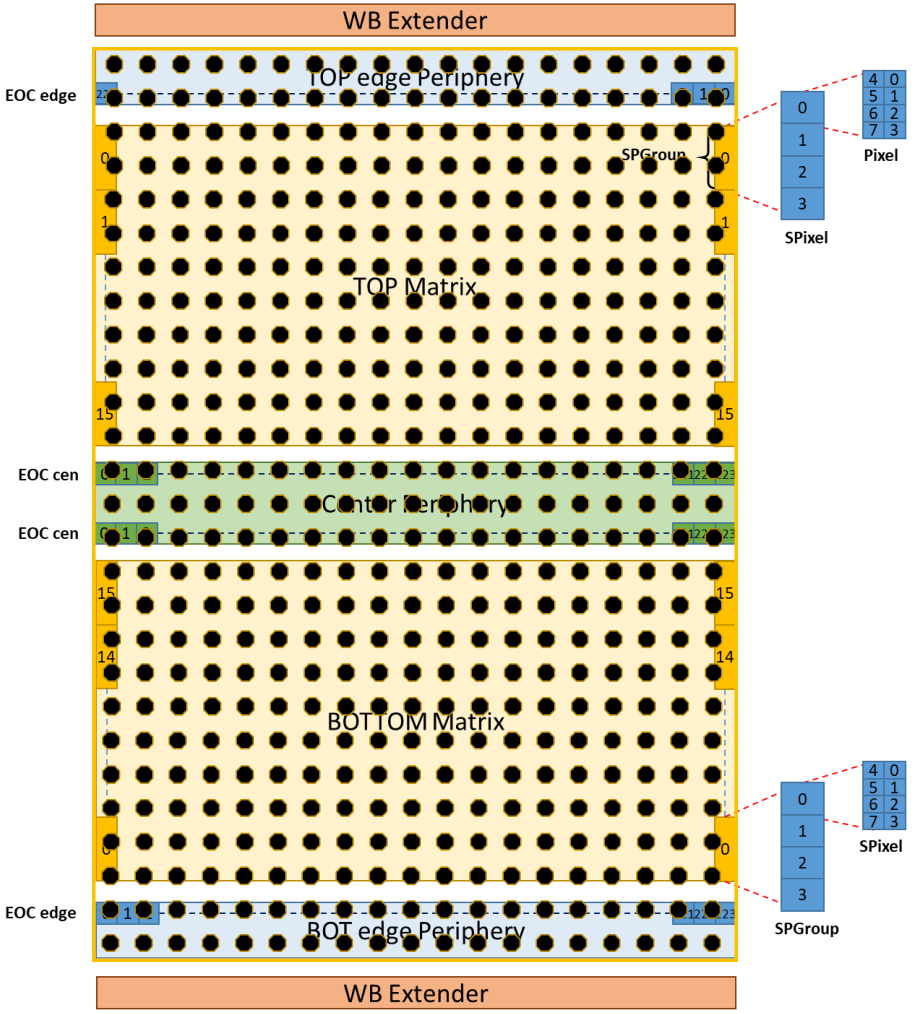
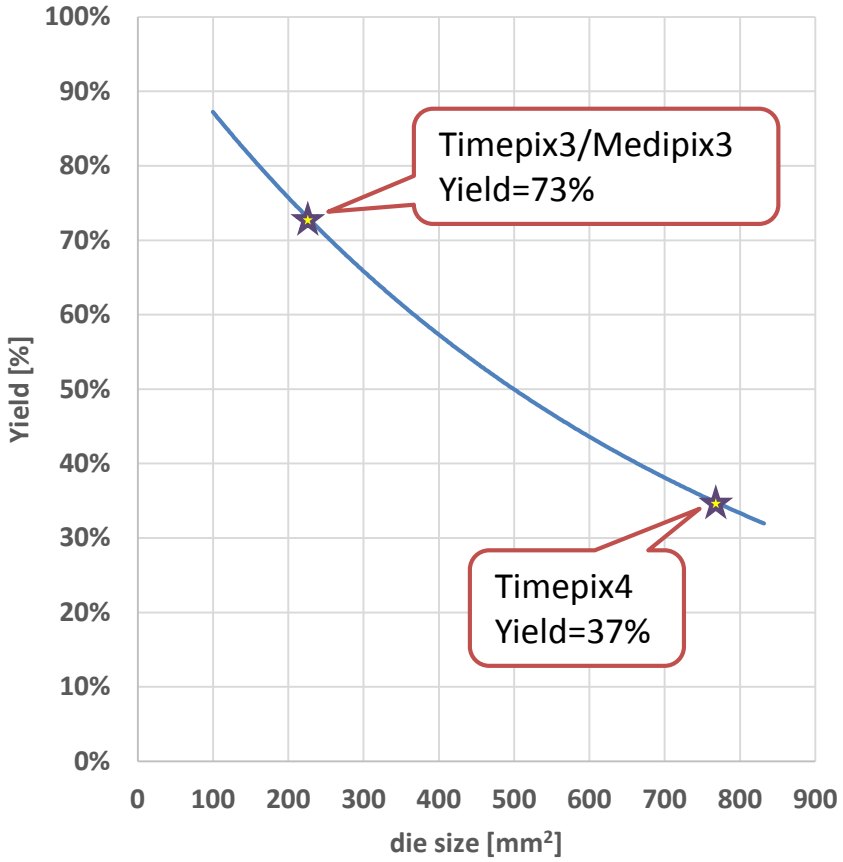
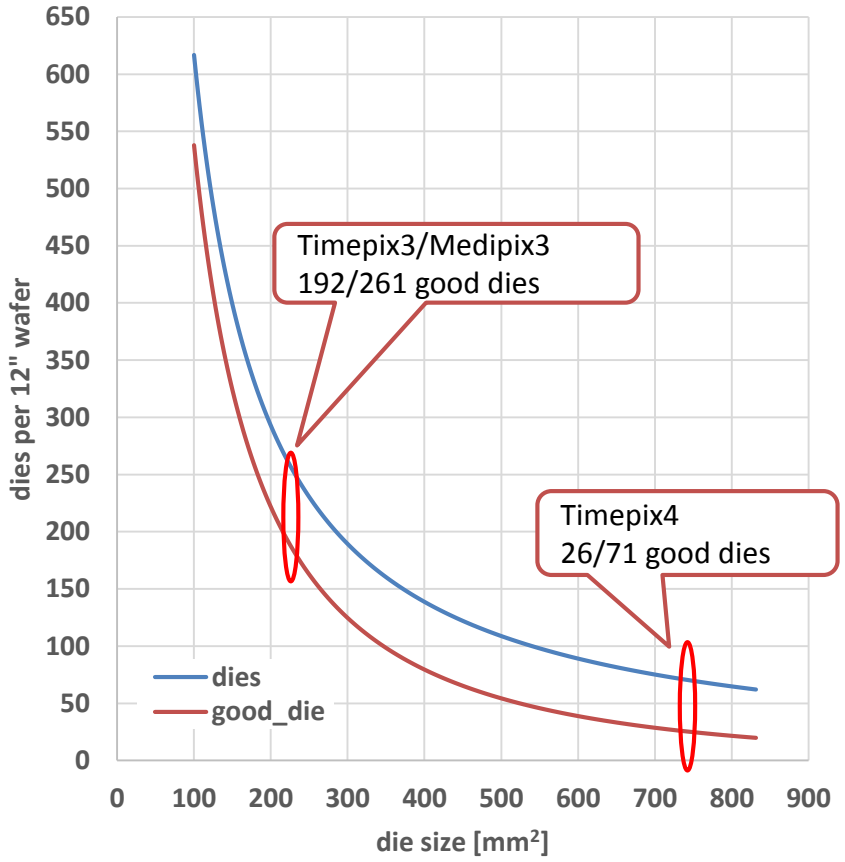


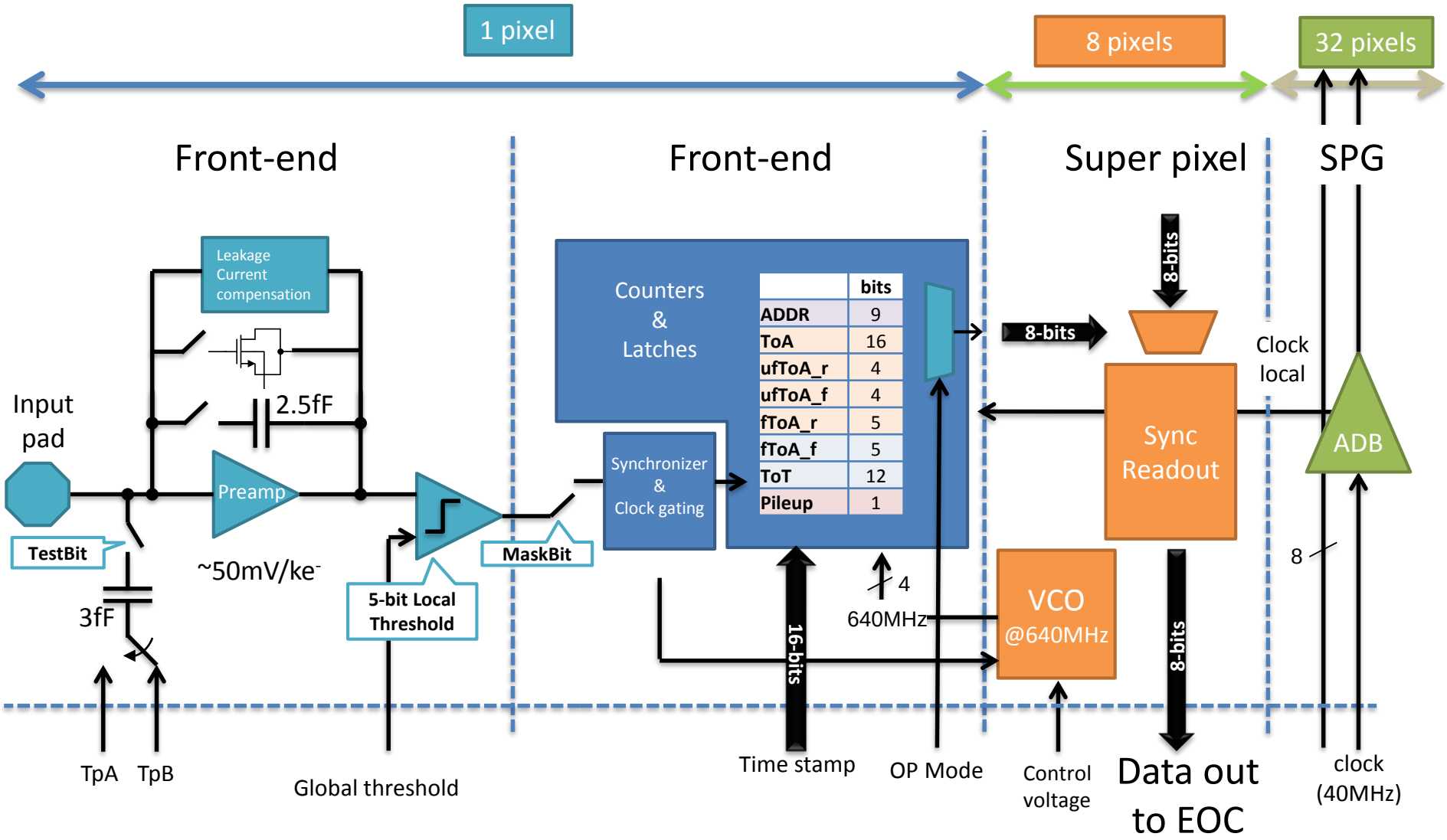
Expected Timepix4 Yield



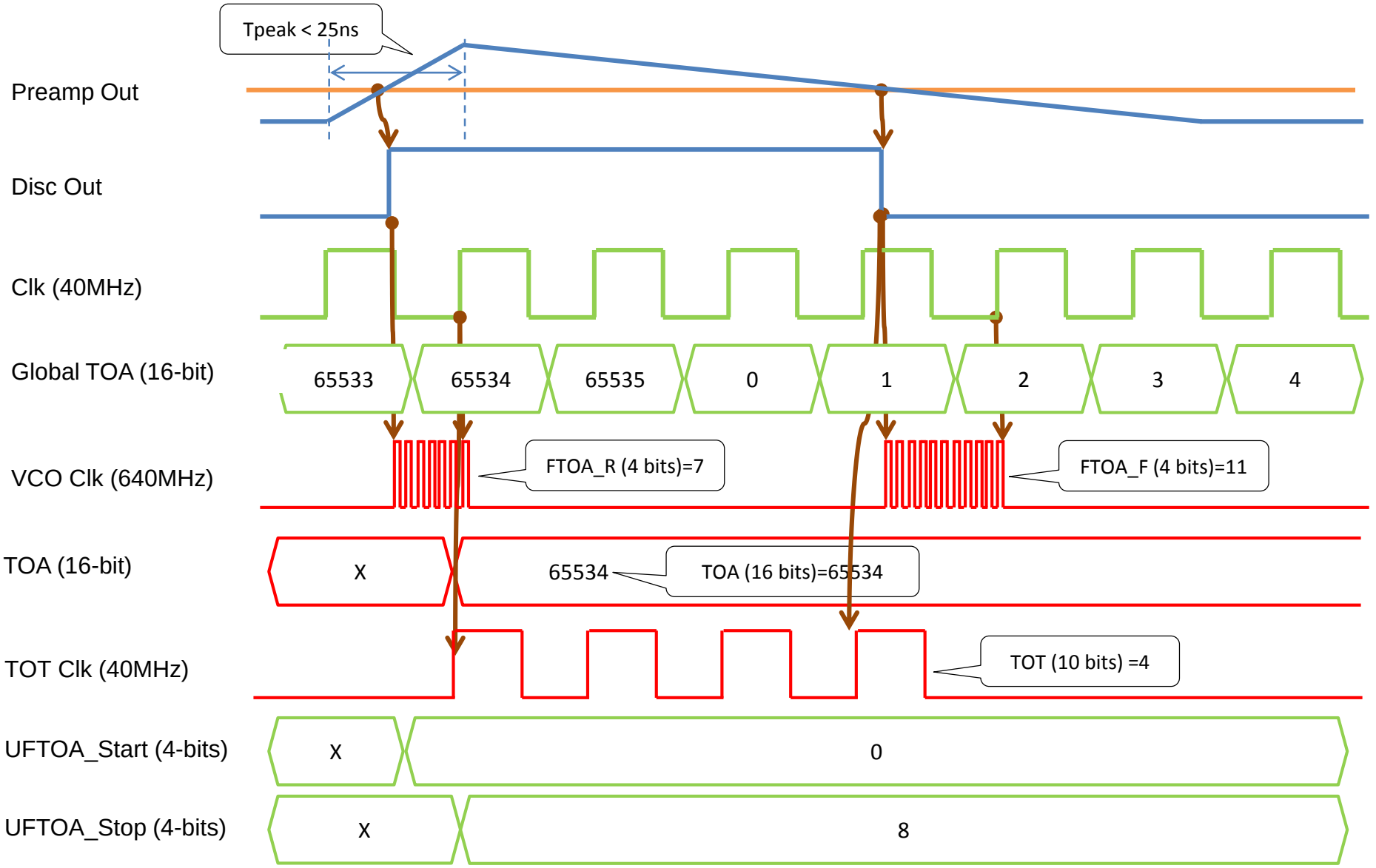


*Based in the foundry yield model for perfect dies

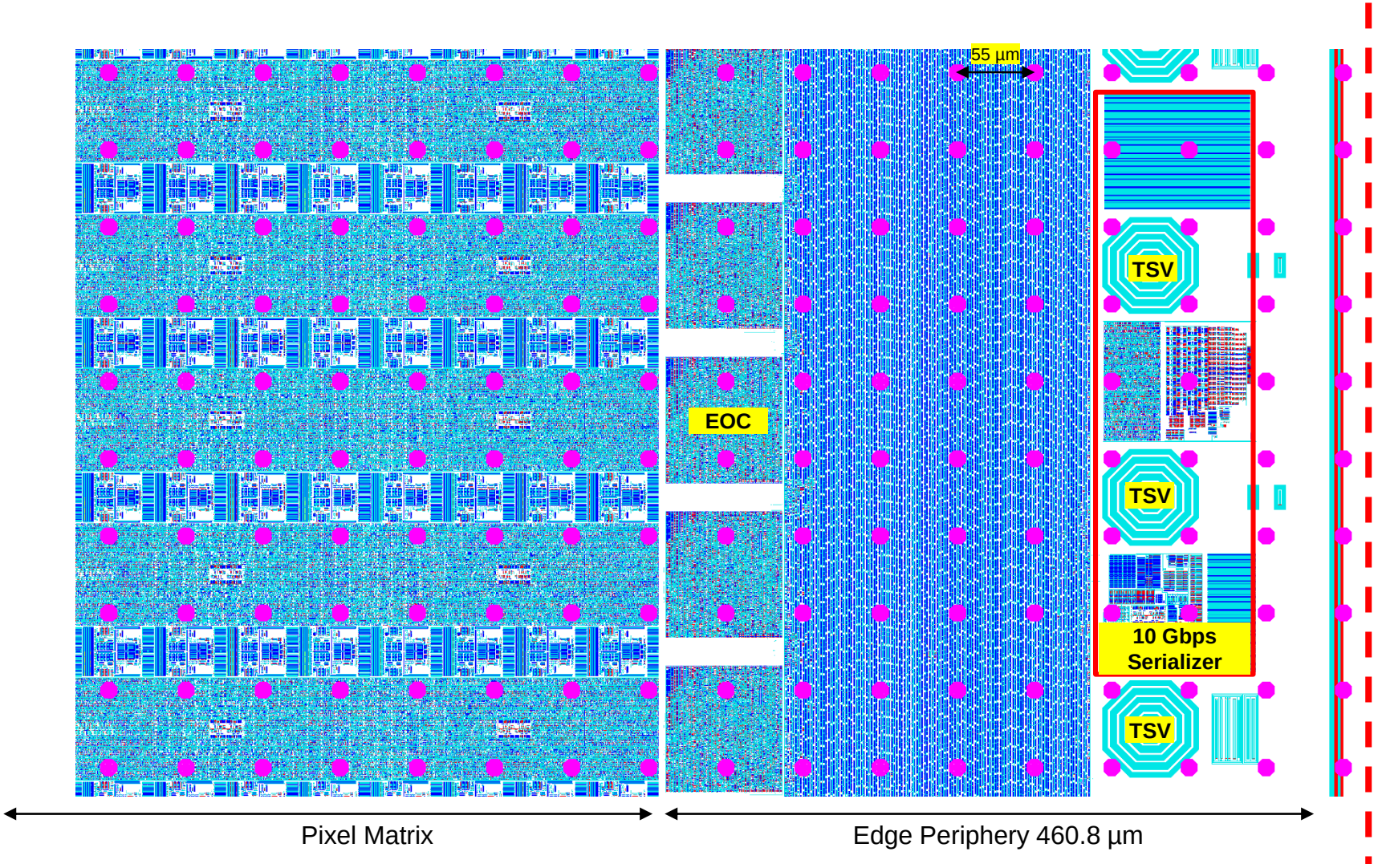
Timepix4 Pixel Schematic



Pixel Operation in TOA & TOT [DD]

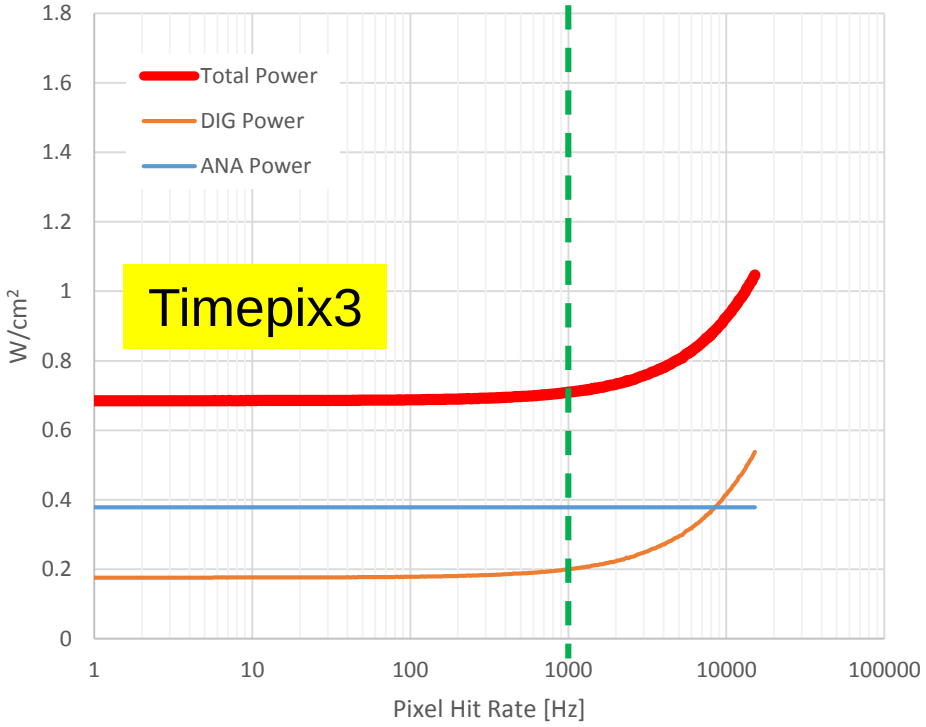


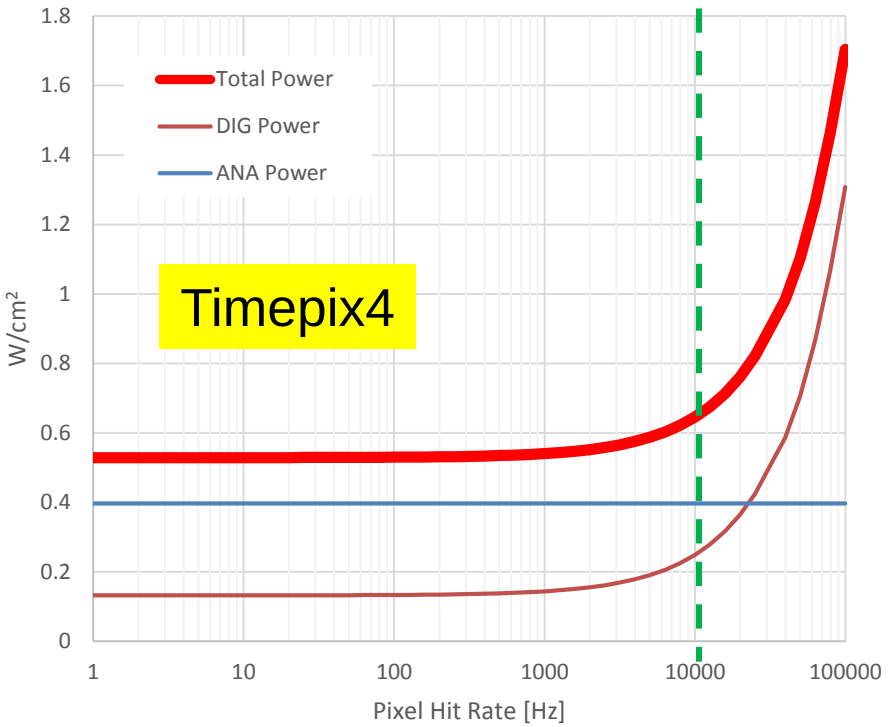
“Hidden” Edge Periphery



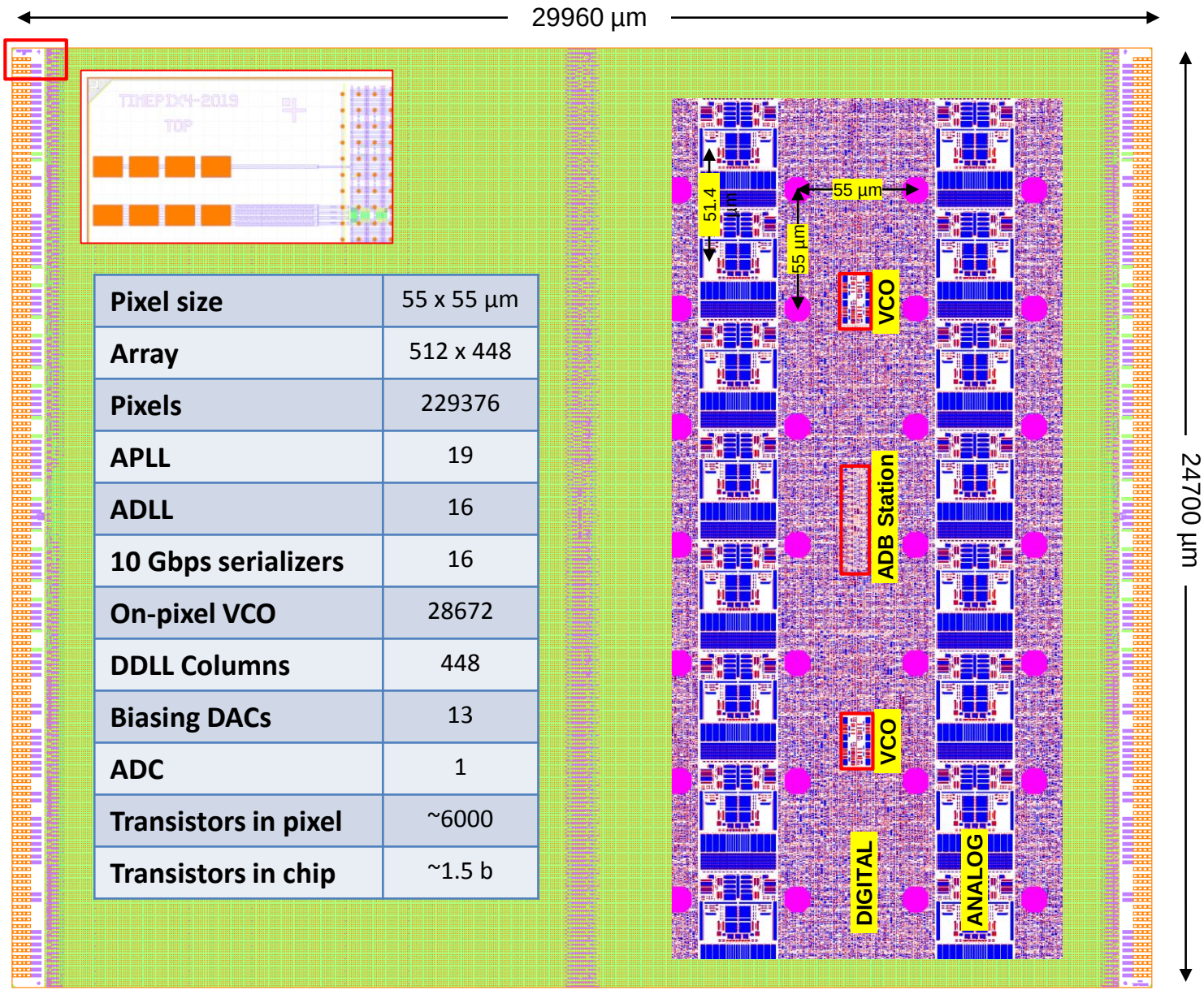
Digital (dynamic) Power Consumption [data-driven]

- Simulated power consumption density to be ~20 % less of Timepix3:
  - Digital power consumption 25% less
    - Improved pixel matrix clock distribution (DDLL)
    - 130nm → 65nm
  - Analog consumption is ~5% more
    - Minimize jitter → < 50ps
    - Compensate increase in input capacitance





Timepix4 (2019)



Pixel size	55 x 55 µm
Array	512 x 448
Pixels	229376
APLL	19
ADLL	16
10 Gbps serializers	16
On-pixel VCO	28672
DDLL Columns	448
Biasing DACs	13
ADC	1
Transistors in pixel	~6000
Transistors in chip	~1.5 b

Summary

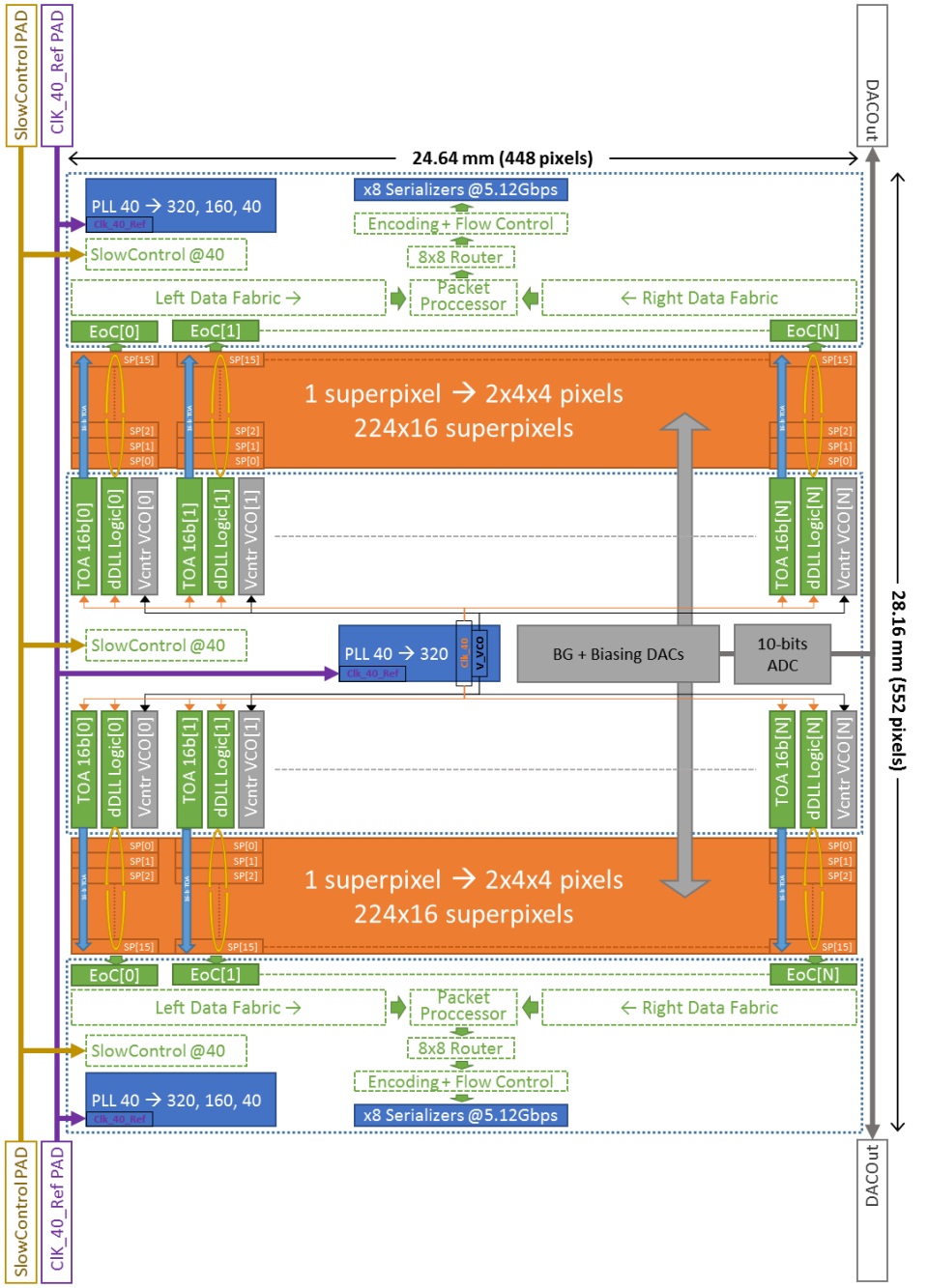
- CHIPS initiative aims to:
  - Strengthen Foundry Services and Technical Support in CERN EP-ESE-ME
  - Meet the challenges of present and future CMOS designs in the HEP community and at CERN

- Timepix4 (2019) is the new particle tracker hybrid pixel detector from the Medipix4 collaboration
  - >229 Kpixels of 55x55 µm
  - No dead area
  - 195 ps time binning → 56 ps_{rms} time resolution

SPARE

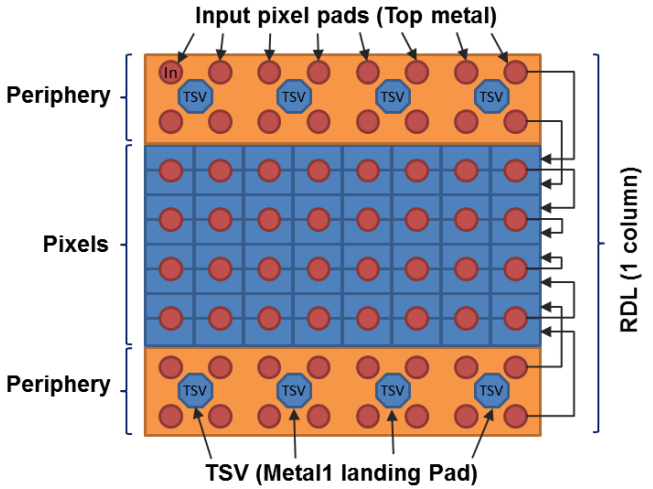
Timepix4 Floorplan

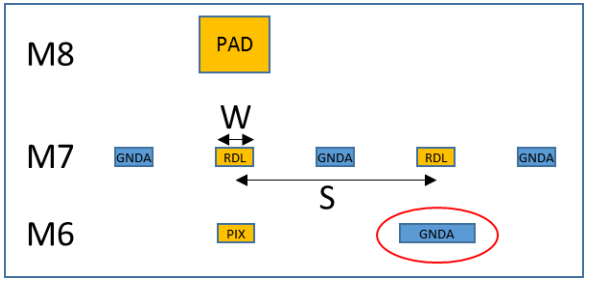
- Chip size 28.16mm x 24.64 mm (no Wirebonds)
- 512 x 448 → 229376 pixels
- Pixel size 55µm x 55µm
- Analog Periphery (920 µm):
  - BandGap + Temperature sensor
  - Biasing DACs
  - Monitoring ADC
  - PLL for time reference
  - Analog supply
  - Digital supply
- 2 x Digital Periphery (460 µm):
  - 8 x 10.28 Gbps serializers (configurable)
  - PLL(s)
  - Analog supply
  - Digital supply
- 2 x Pixel matrix (13.28 mm x 24.64mm):
  - 256 x 448 pixels 55 µm x 51.4 µm
  - 5.68% smaller than 55 µm x 55 µm
  - RDL to compensate up to 460.8 µm

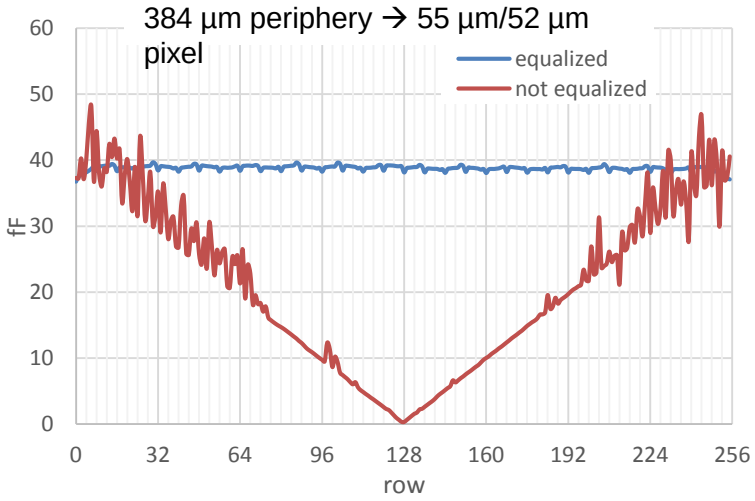


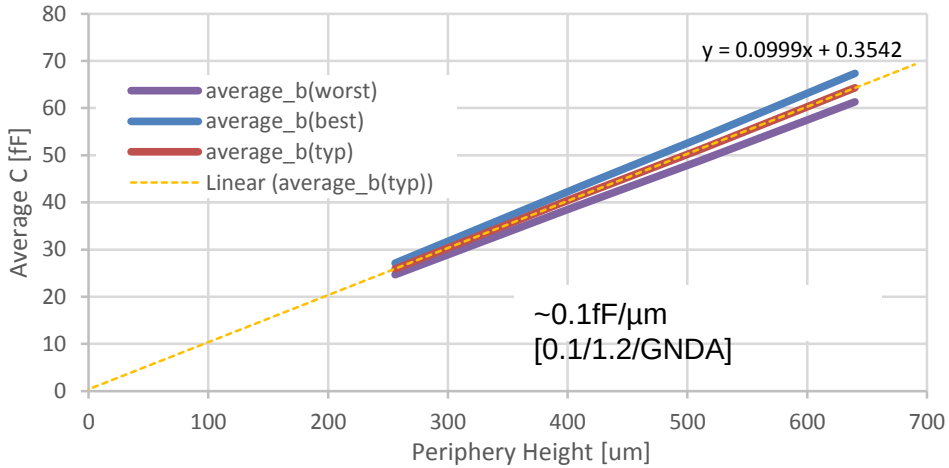
On-chip pad to pixel RDL

- Use of 10 metal option (1p9m + RDL):
  - Equalized Cin for all pixels → ~46 fF increase in Cin for a 460 µm periphery
  - Shielding of RDL layers to minimize/eliminate cross-coupling
- RDL routing over analog pixel circuitry and periphery → M7 used as shield



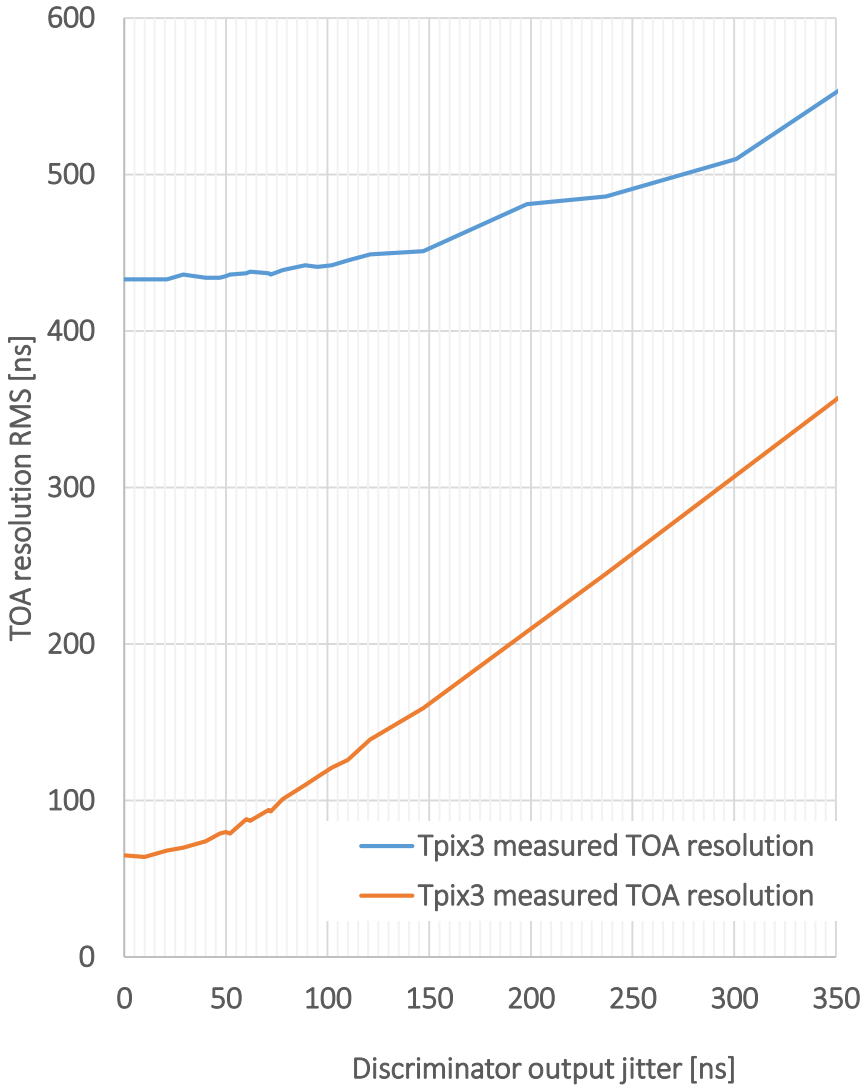






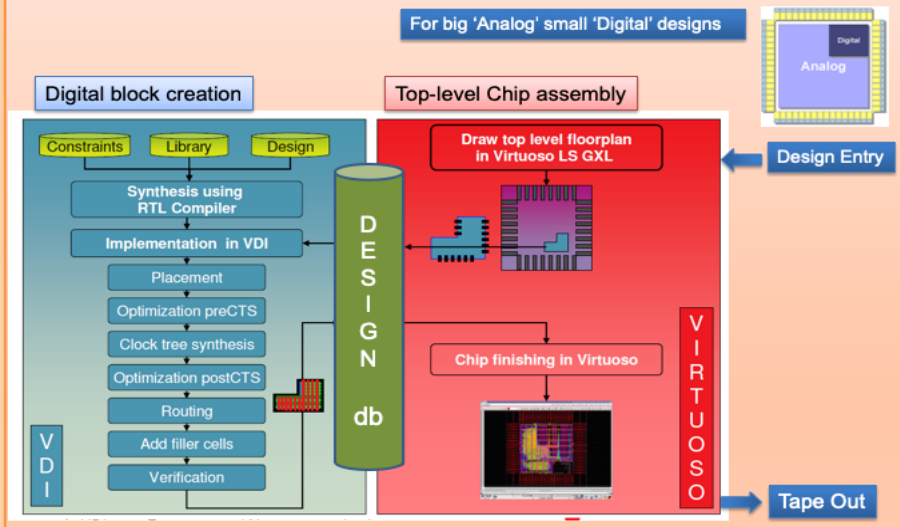
On-pixel < 200ps time resolution

- FE + discriminator jitter < 50 ps_{rms}
- Column dDLL to distribute the 40 MHz
  - Controlled skew on the stop signal (<100ps)
  - Minimizes noise from pixel matrix clock distribution
- Share an on-pixel 640 MHz VCO among 8-pixels:
  - Oscillation frequency locked (Vcntrl) with periphery PLL for PVT control
  - 1.56 ns resolution (as in Timepix3)
  - 195 ps obtained latching the internal VCO phases



Analog vs. Digital on Top flows

Analog On Top workflow

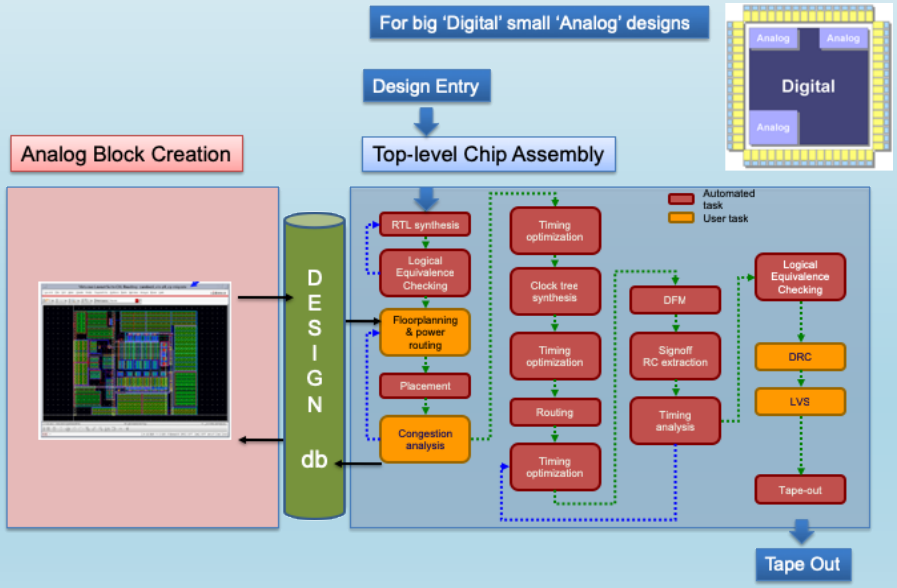


Analog on Top - Historical design flow

Blocks are prepared separately then added one-by-one to the design

Ok for small designs but extremely risky for complex ASICs

Digital On Top workflow



Digital on Top – New approach for complex designs

System-on-chip design

High level simulation and verification throughout design

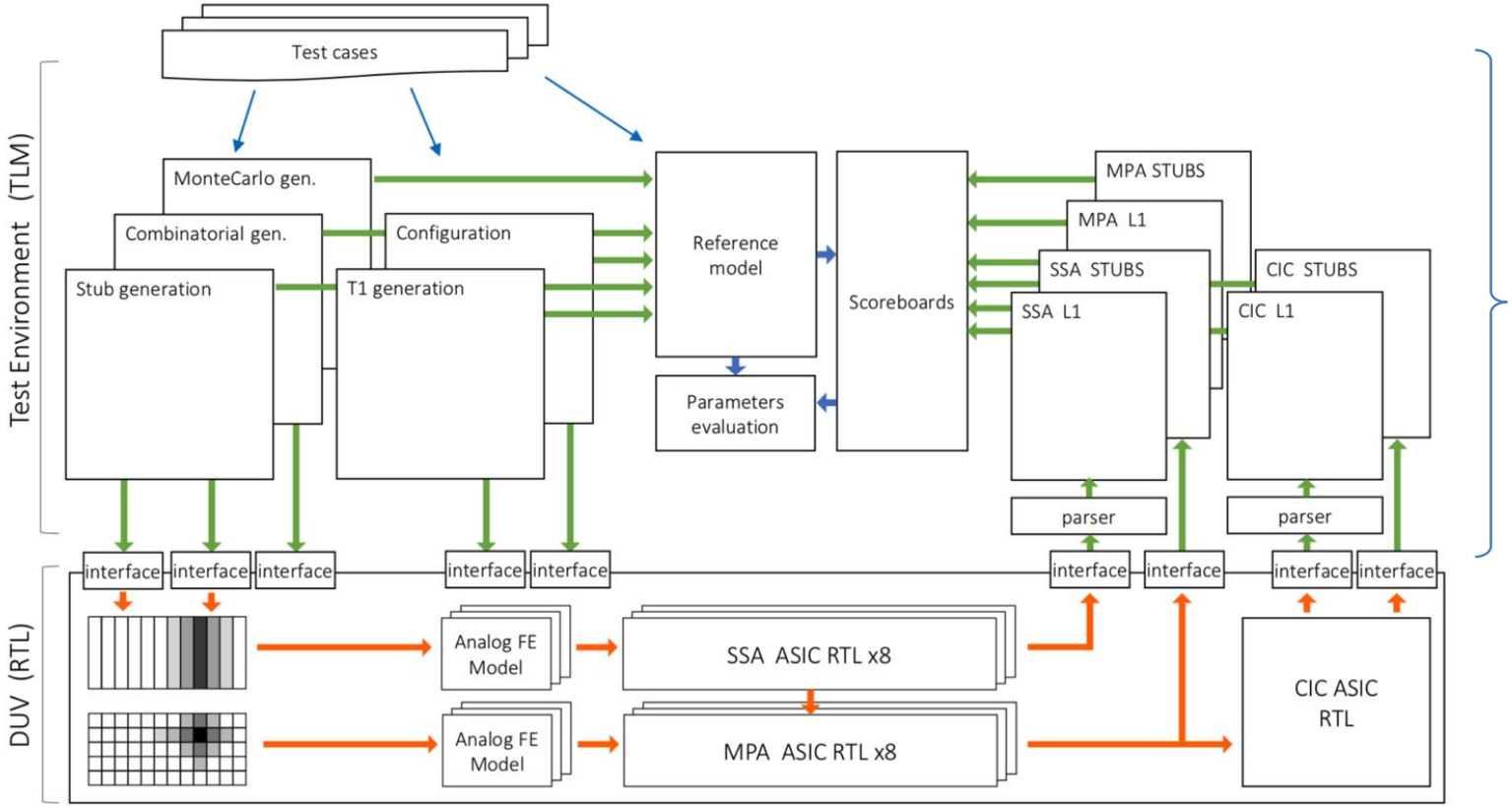
Requires different skill set and generally more resources

Strong mitigation of risk if *all* steps are *fully* followed

System Level verification framework

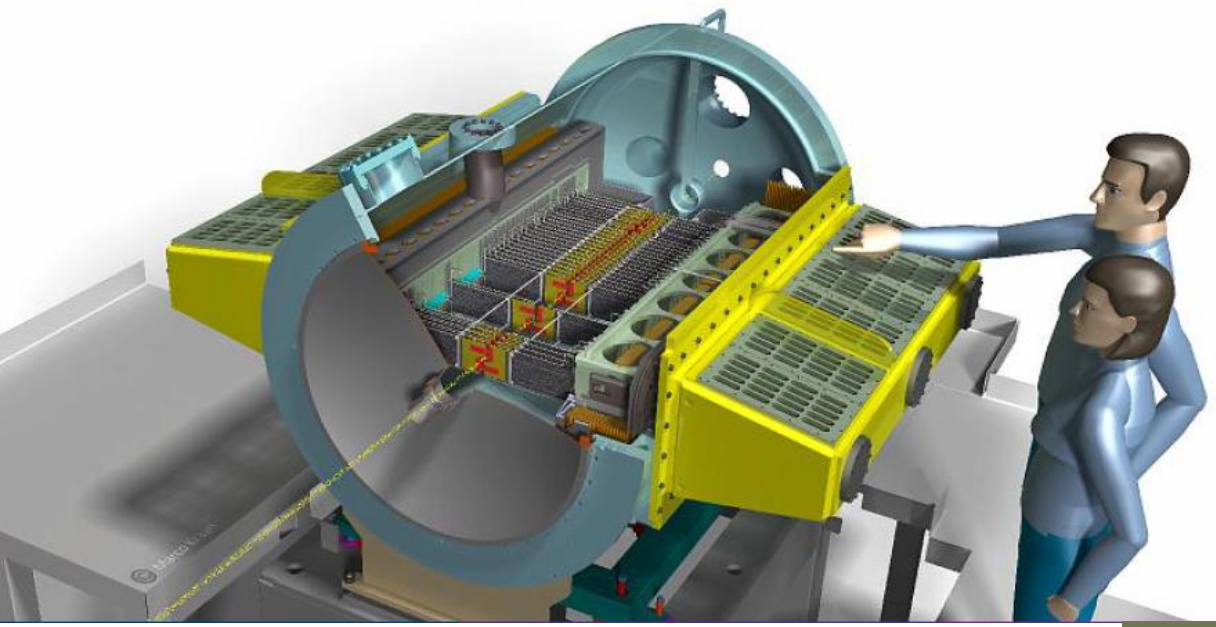
CMS Outer Tracker ASICs (MPA/SSA/CIC) verification framework

Simone Scarfi
Alessandro Caratelli



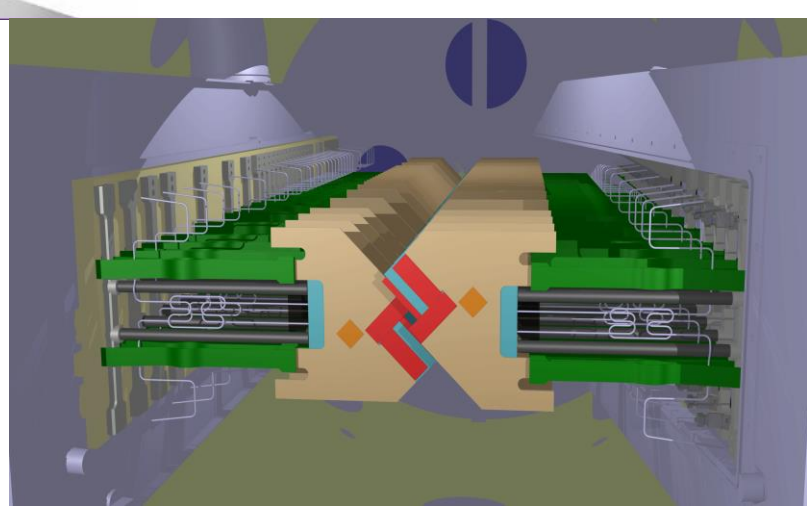
5-10 times more lines of code than RTL

Vertex Locator Upgrade



LHCb will be upgraded in 2019→2020
→ very tight planning

- Vertex detector surrounding collision region
  - In vacuum
  - Close to the beam: 5.1 mm
- From silicon strips to pixels
- New R/O chip VeloPix, derived from Timepix3
- In total 624 ASICs, ~41 Mpixels
- Trigger-less readout (~2.9 Tbits/s)



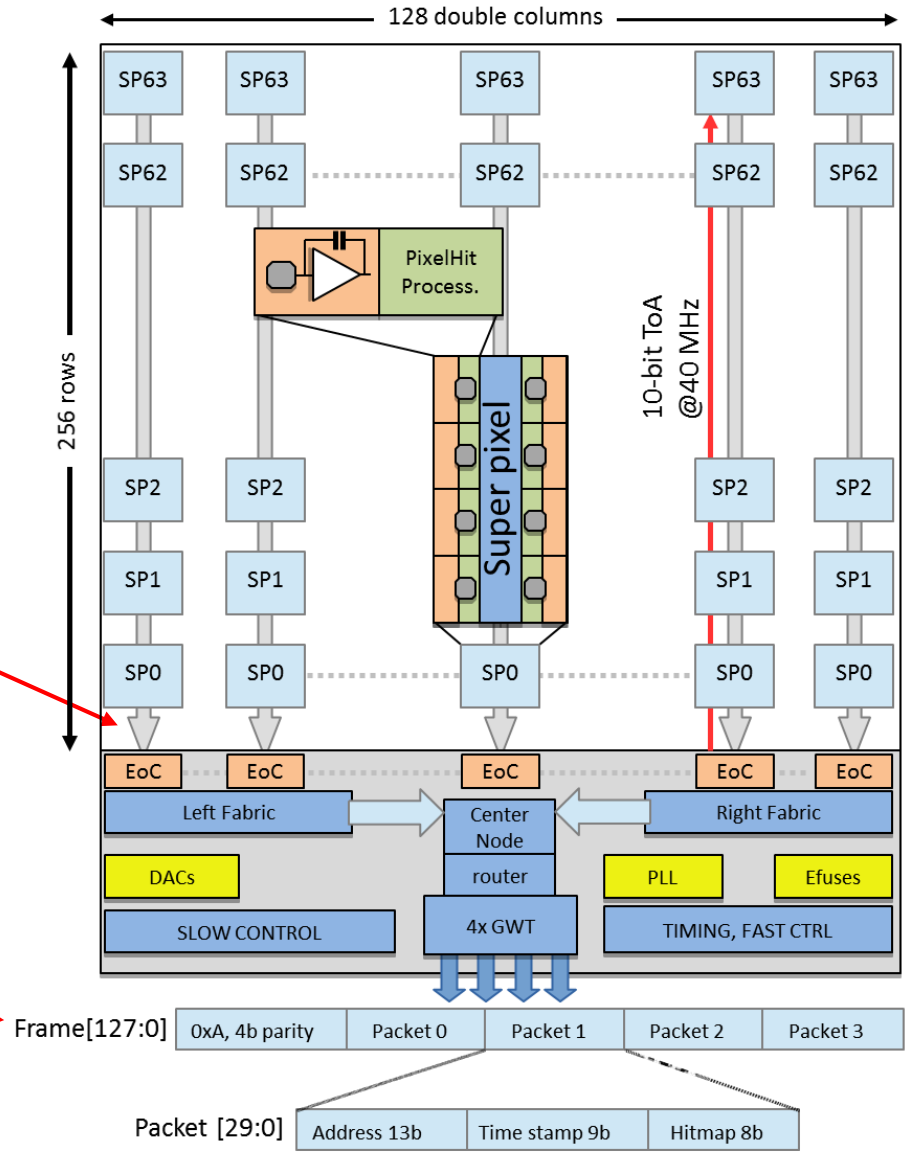
"The VeloPix ASIC test results" E. Lemos (poster)
"The LHCb Vertex Locator Upgrade" E. Lemos (talk)

From Timepix3 → Velopix

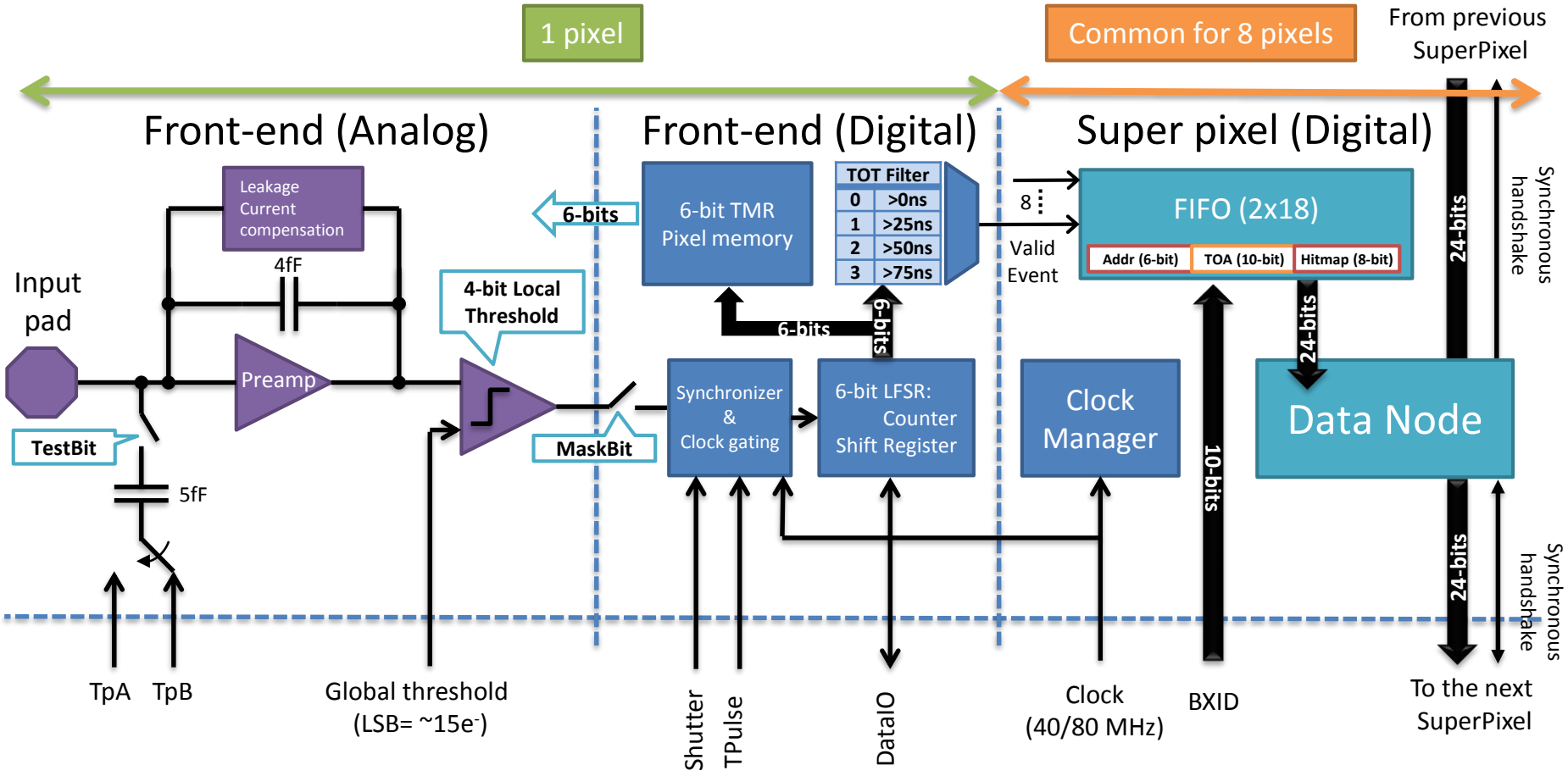
	Timepix3 (2013)	VeloPix (2016)
Pixel arrangement	256 x 256	
Pixel size	55 x 55 µm²	
Peak hit rate	80 Mhits/s/ASIC	800 Mhits/s/ASIC 50 khits/s/pixel **10x**
Readout type	Continuous, trigger-less, TOT	Continuous, trigger-less, binary
Timing resolution/range	1.5625 ns, 18 bits	25 ns, 9 bits
Total Power consumption	<1.5 W	< 3 W
Radiation hardness		400 Mrad, SEU tolerant
Sensor type	Various, e- and h+ collection	Planar silicon, e- collection
Max. data rate	5.12 Gbps	20.48 Gbps **4x**
Technology	IBM 130 nm CMOS	TSMC 130 nm CMOS

VeloPix Chip Architecture

- Pixel matrix:
  - 256 x 256 pixels
  - 128 x 64 super pixels (2x4 pixels each)
  - @40MHz
- Packet-based architecture:
  - 8 pixels/packet + 9 bit time stamp → 30% reduction in data rate
- Data-driven readout:
  - 20 Mpackets/s/double column
- 40, 80, 160 and 320 MHz TMR clock domains in the periphery
- 1 to 4 configurable serializers (GWT)
- Similar to the GBT frame



VeloPix pixel schematic

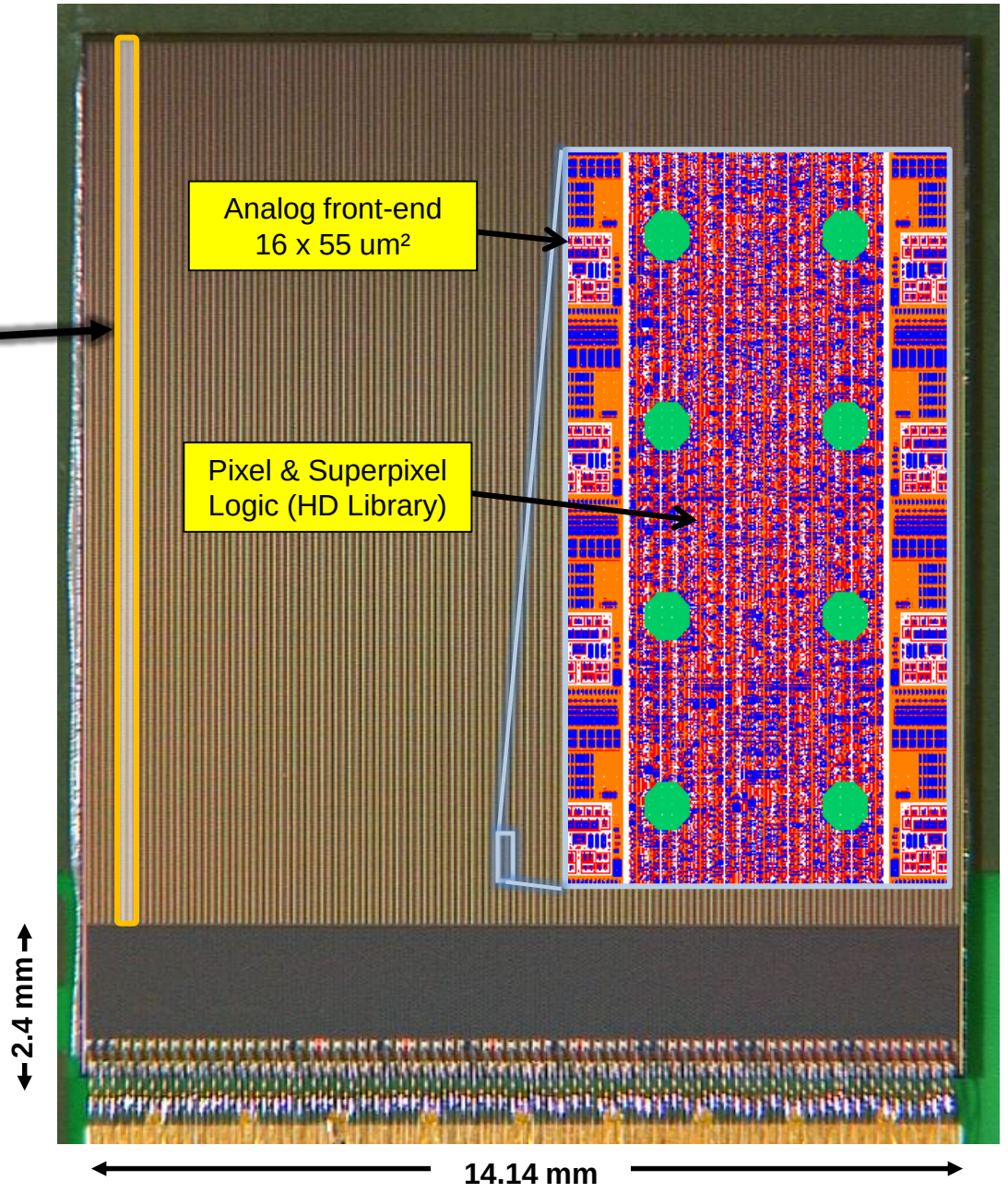


VeloPix (2016)

Double column:
2x256 pixels
64 super pixels

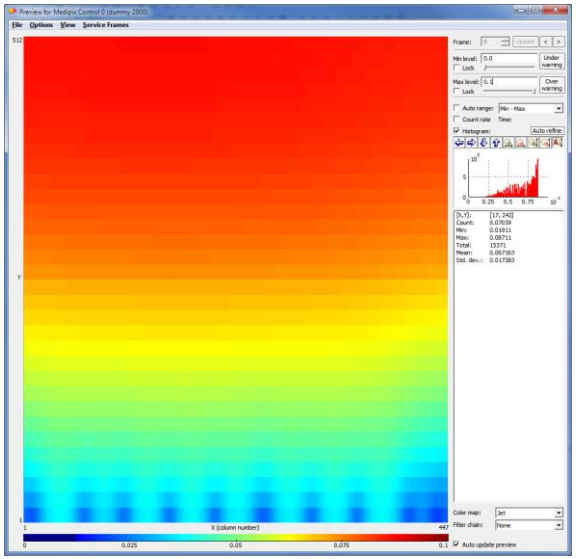
Full matrix:
128 Double columns
~190 Mtransistors

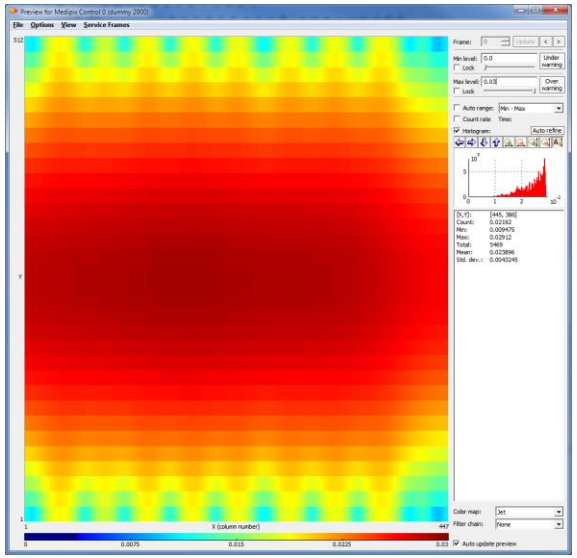
Active Periphery

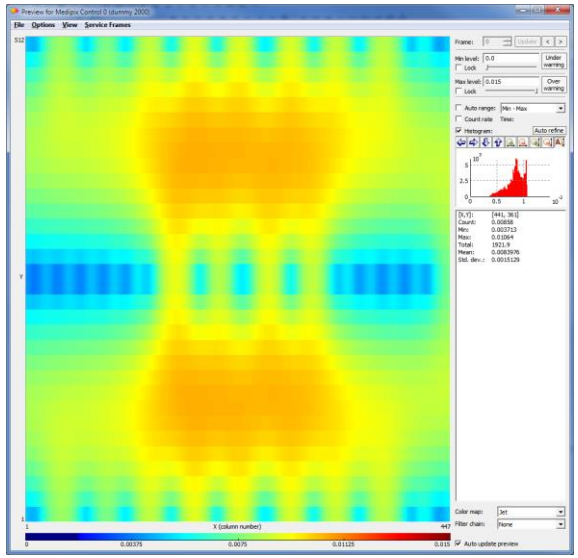


Analog (static) power supply distribution

	1 WB		2WB	3TSV
Nominal Analog Power [10 µA/pixel]	V_{drop} [max-min]	68 mV	19.6 mV	6.9 mV
	Imax pad	118 mA	60 mA	57 mA
Low Analog Power [1 µA/pixel]	V_{drop} [max-min]	6.8 mV	1.96mV	0.69mV
	Imax pad	11.8 mA	6 mA	5.7 mA







Timepix Applications

- New Tracking Technologies
  - LHCb Upgrade
  - CLIC detectors
  - Solid state Detector Development
- TPC instrumentation
  - EUDET
- Emission Channeling Crystal Lattice Experiments
  - ISOLDE
- Image Intensifiers / Optical Photon Detectors
  - Adaptive Optics
  - Bioimaging
  - LHCb RICH
- ToF Mass Spectrometry
  - Proteomic Imaging at AMOLF and Oxford
- Imaging Mass Spec
  - Functional Cellular Biology at Kiev
- Photo Electron Emission Microscopy and Low Energy Electron Micrsocopy
- Neutron Monitoring at CNGS
- Space Dosimetry
- Education - CERN@School