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The Timepix4 chip and its design approach

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The Timepix4 chip is the new hybrid pixel detector ASIC designed at CERN in the frame of the Medipix4 collaboration. This new chip will consist of an array of 512x448 pixels with 55 um square pixels. The chip is highly configurable in order to cover a large range of applications and it can be programmed to work in particle tracking mode or in frame based mode. In particle tracking mode the chip works in a data driven readout mode where the chip sends out a 64-bit data packet containing pixel coordinate, time over threshold and time of arrival immediately after the hit is processed by the pixel. The maximum hit rate in particle tracking mode is 360 Mhits/cm2/s with a time tagging bin size of 195 ps. In frame based mode the pixel works in photon counting mode with a maximum count rate of 800 Ghits/cm2/s. The chip includes 16 10 Gbps serializers in order to cope with the maximum particle hit rate in data-driven. The aim of this publication is to present the chip as an example of the usage of modern ASIC design tools and how the designers approach the design of such complex chip.

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