Hybridization of the HPK Planar Pixel Modules for ATLAS ITK upgrade

Koji Nakamura (KEK)

On behalf of ATLAS Japan Pixel group and Hamamatsu Photonics K.K.

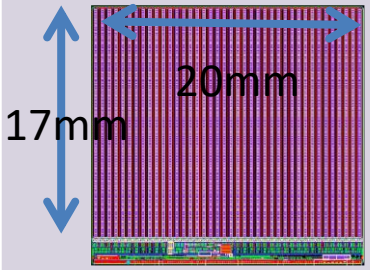
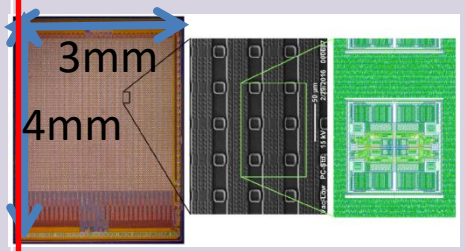
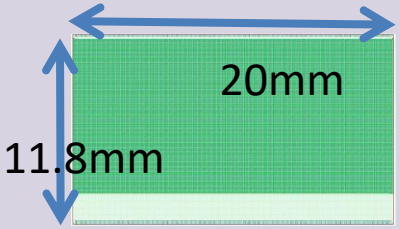
Introduction

- ***High Luminosity LHC (HL-LHC)***
  - Start around 2026- with new crab cavity in the interaction region.
  - Target : $\sqrt{s}$=14TeV L=7x10^{34} $\int Ldt$=4000fb^{-1}
  - Physics program focus the precise measurement of the Higgs coupling (e.g. Y_τ, Y_b and λ_{HHH}) and BSM searches.
- ***Tracking detector is key element***
  - To keep B/τ-tagging performance up to μ=200 pileup in an event.
  - Mitigation of the pileup effect for MET calculation can be done by tracking as many tracks from primary vertex as possible.
- ***Development of middle-outer pixel layer***
  - Planar type Pixel detector (For ATLAS phase II upgrade : ITK pixel)
  - **n+-in-p sensor with Pixel size : 50um x 50um (or 25um x 100um)**
  - **Radiation tolerance : up to 3x10^{15} n_{eq}/cm^2**

Hybridization technology and module performance are presented in this presentation

Available Front End ASICs

- Three FE, FE-I4, FE65p2 and RD53A were produced.
  - **Hybridization study was based on FE-I4 the same outer size of production chip.**
  - For Module performance study, RD53A was used the same pixel pitch of production chip.

	FE-I4 (2012)	FE65p2 (2016)	RD53A (Nov. 2017)
ASIC demention			
CMOS process	130nm	65nm	65nm
Pixel size	**50um x 250um (25um x 500um)**	**50um x 50um (25um x 100um)**	**50um x 50um (25um x 100um)**
Pixel matrix	336 x 80	**64 x 64**	400 x 192
Max data output rate	160Mbps	160Mbps	**1.28Gbps x 4**
stable threshold (typical threshold)	**~1500 e^- (2000-3000 e^-)**	**500 e^- (700 e^-)**	**500 e^- (1000-1500e^-)**

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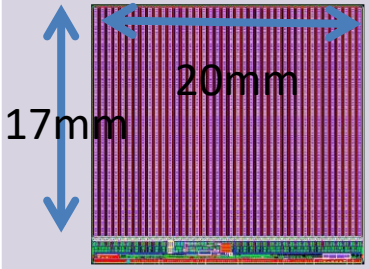
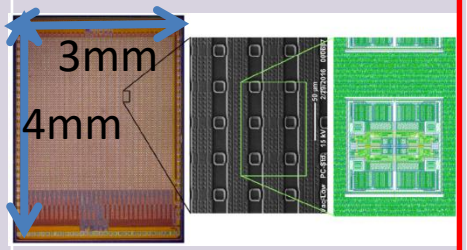
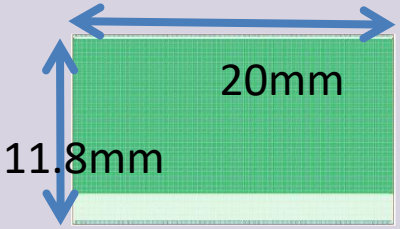
ASIC demention			
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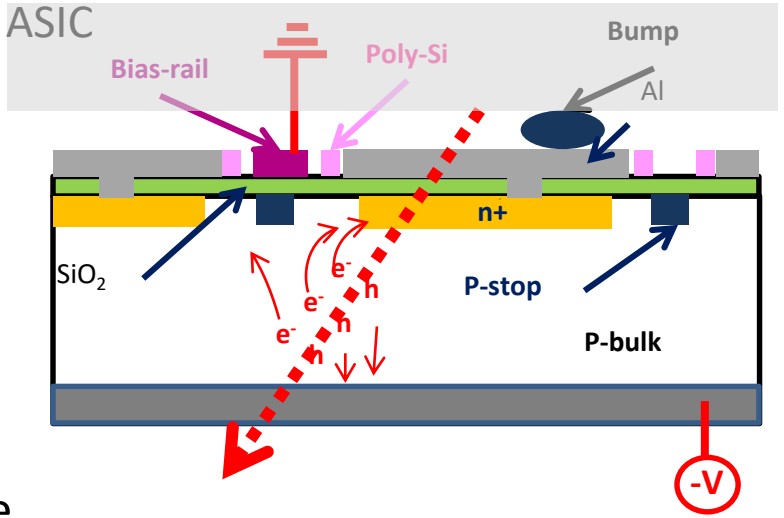
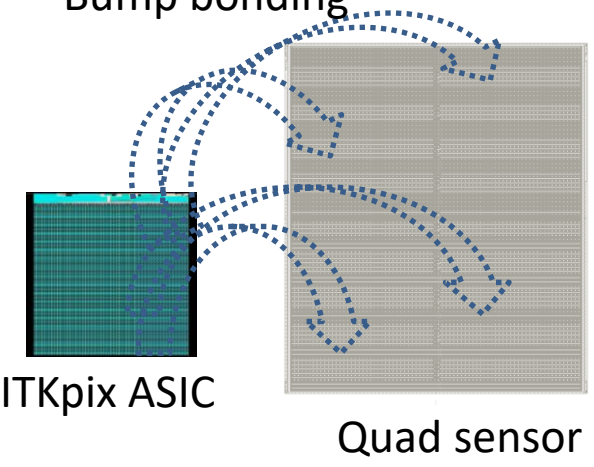
Hybrization at HPK

- To readout signals from 2 dimensionally placed electrodes (pixels), readout ASIC needed to be connected.
  - the signal from each channel is read out through a solder bump
  - ***Bump bonding :***
    - Solder bump deposition to the ASIC side
    - Under bump metallization to Sensor side
    - Flip-chipping : 4 chips to one sensor.
- ATLAS Japan group investigated with HPK using bias resistor to each pixel. This allows us to sensor testing before costly bump bonding process



Bump bonding



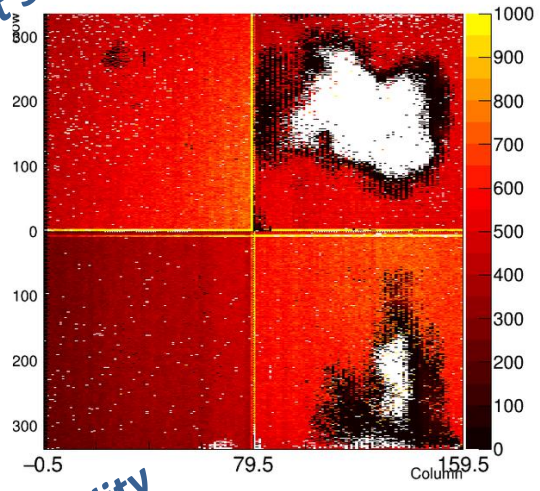
ITKpix ASIC

Quad sensor

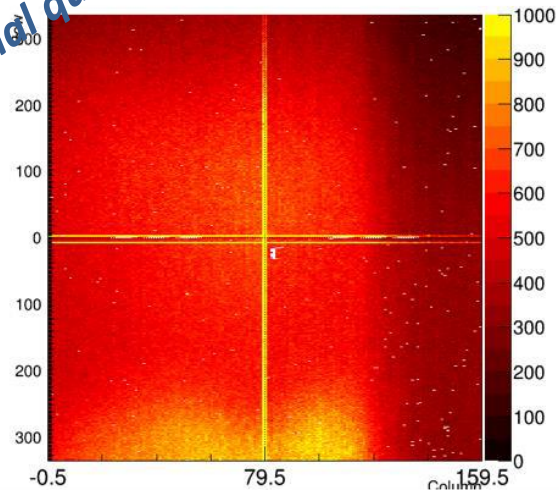
Flip chipping development at HPK

- **Development of Lead-free(SnAg) Bumpbonding (Since 2012)**
  1. ***No Flux used (to avoid corrosion)***
     - confirmed flux improve connection, though
  2. ***No backside compensation***
     - Improvement of Vacuum chuck jig to hold and flatten the ASIC/Sensor…(jig size ~ FE-I4 area)
  3. ***Special UBM*** (key element: confidential…)
     - Simple Ni/Au UBM do not reach 100% yield …
  4. ***Hydrogen plasma reflow*** to remove surface oxide
- Thin sensor/Thin ASIC : 150um/150um
  - **Established Bumpbonding method in the beginning of 2016.**
  - Quite stable quality for both single and four ASICs. 100% yield for last one year (>100 chips are bumpbonded.)

Without 3 and 4



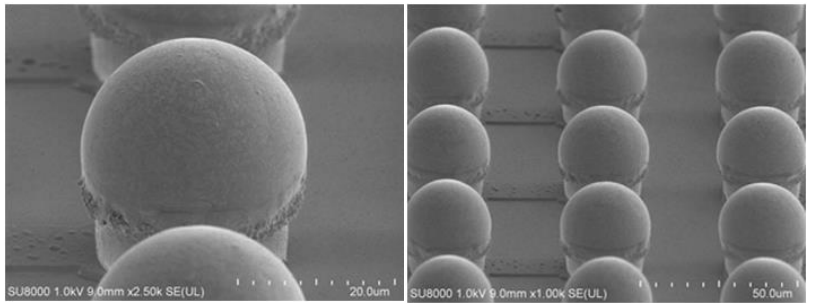
Final quality



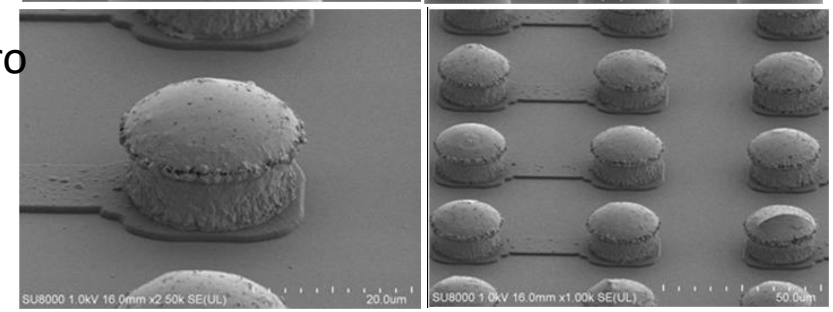
Bump deposition in IZM and T-micro

- For FE-I4 based study, HPK did bump deposition to the 8inch FE-I4 wafer.
- For RD53A and production chip, wafer size is 12 inch and HPK do not perform bump deposition process.
- Tested two vendors with dummy wafer :
  - IZM bump
  - T-micro bump
- Connectivity to the HPK UBM has been checked.
  - Confirmed connectivity is ok for both venders.

IZM

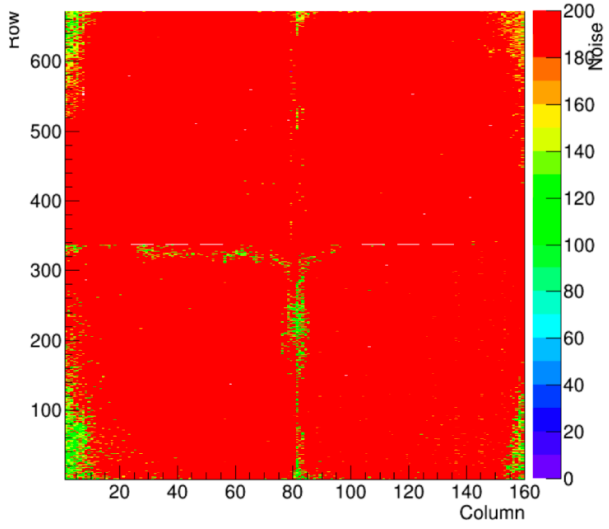


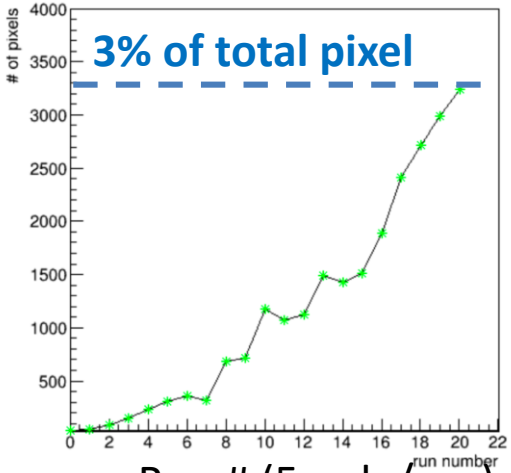
T-micro



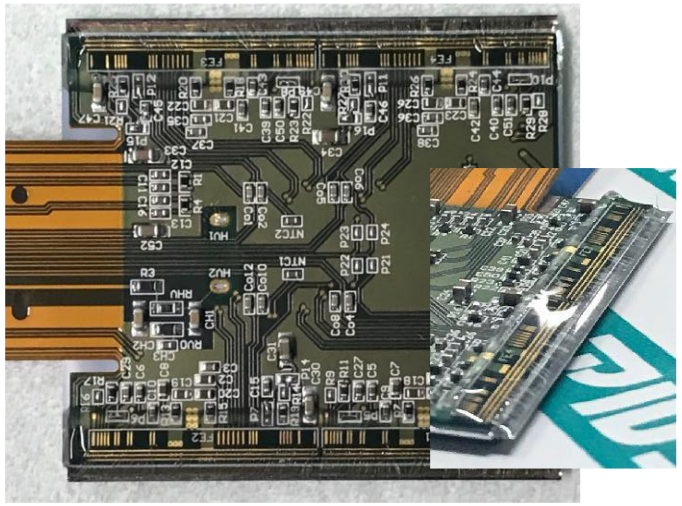
Thermal Cycle and irradiation test

- bare module w/o flex glued to Aluminum plate.
  - **No visible bump disconnection issue for following tests.**
    - Tested >100 thermal cycle [-40,40°C] .
    - 5e10^{15}n$_{eq}$/cm^2 proton irradiated.
- After Flex attached and wire bonds encapsulated.
  - Visible increase of disconnected bumps.
  - **About 3% of bumps are disconnected in 100 cycle.**
    - Due to CTE mismatch to the Copper of Flex PCB.



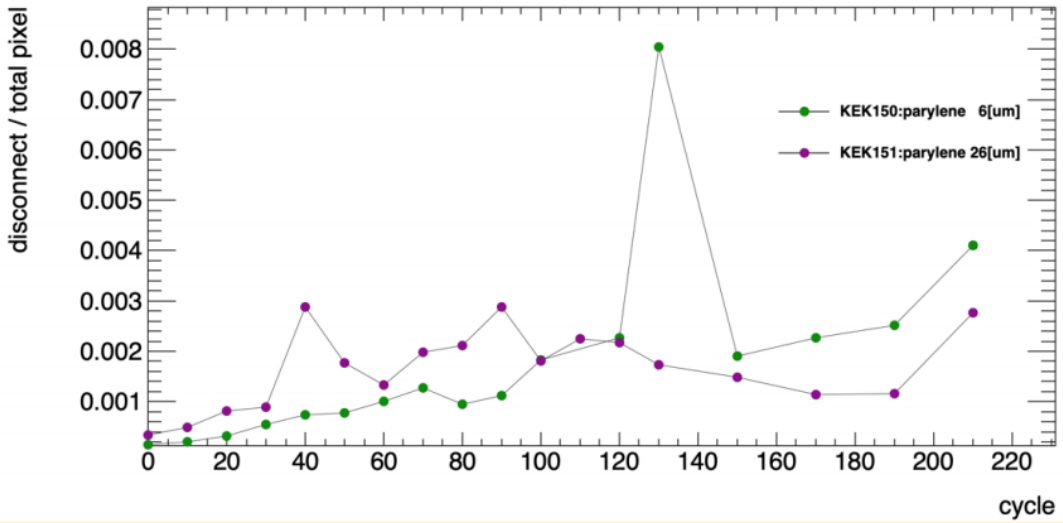


Run # (5cycle/run)



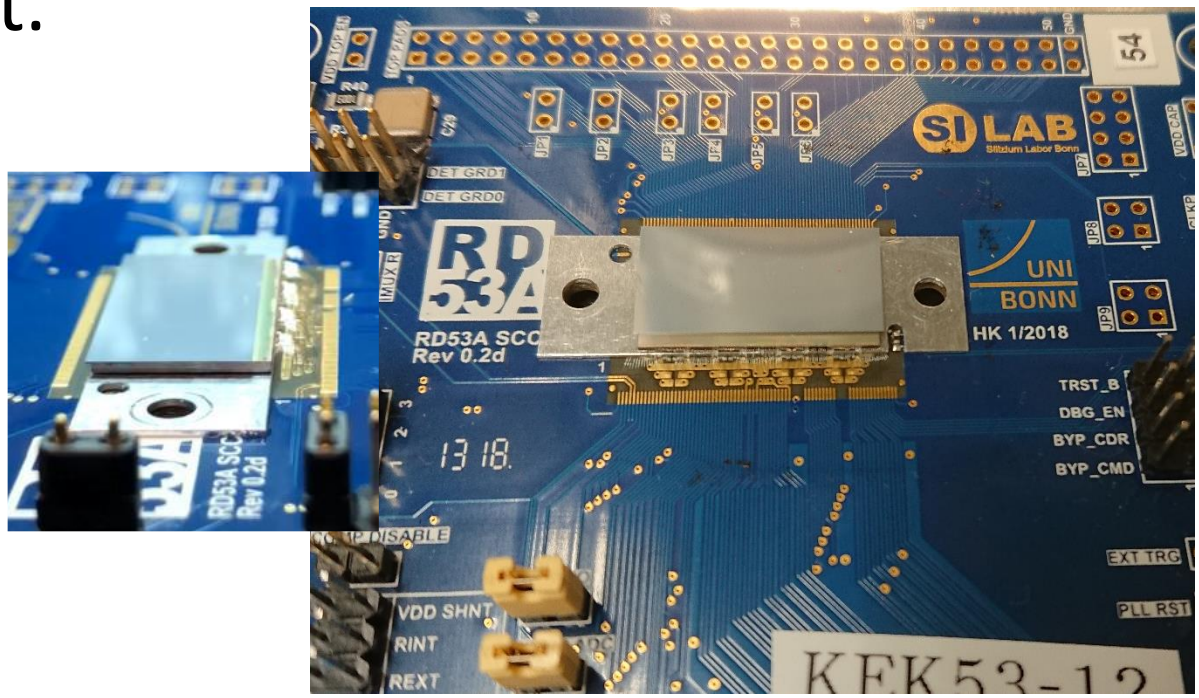
Solutions

- Two solution are investigated.
  - Use low CTE material for the Flex base.
    - Still under discussion with the PCB vendors.
  - Parylene coating
    - Observed Parylene coated modules show much better performance.
    - **Modules with 7um/15um Parylene coating are tested and disconnected bump after 200 cycle is 0.5%**



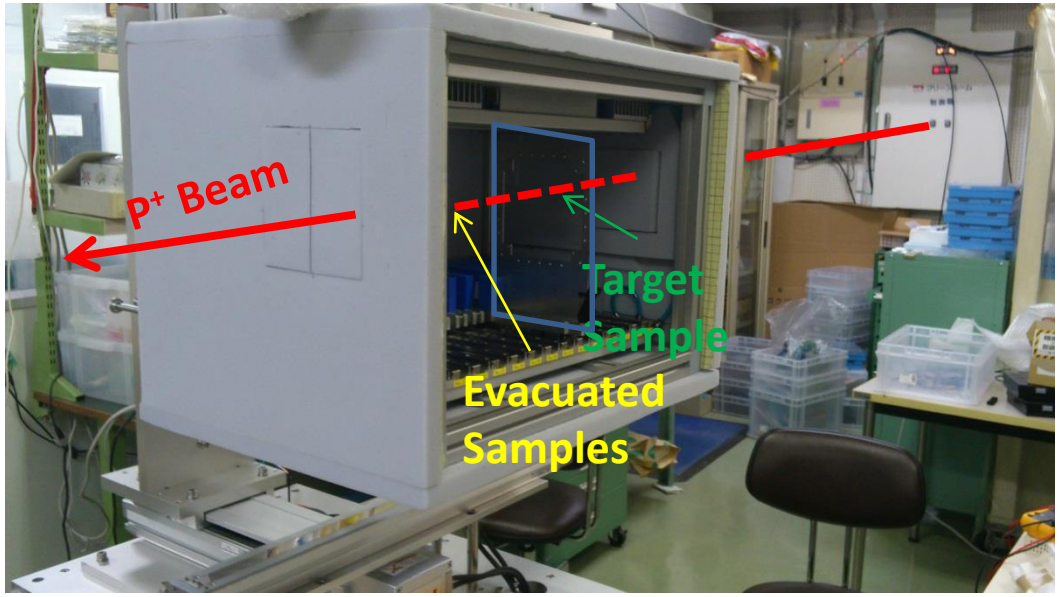
Module performance measurement

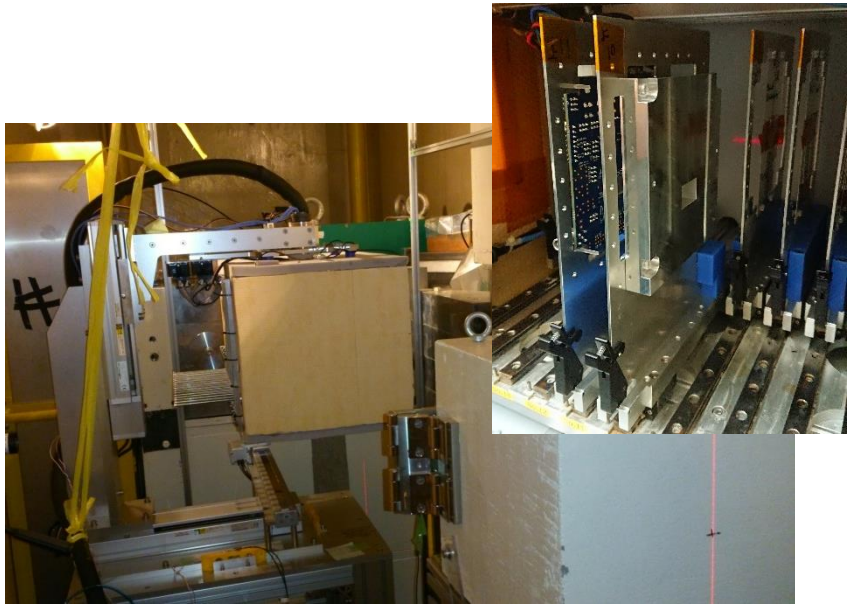
- Tested full performance of FE-I4 ASIC based modules. ***K. Nakamura et al 2015 JINST 10 C06008***
- RD53A FE chip which is the same pixel pitch to the production chip was used further module performance test.



Irradiation Facility in Japan

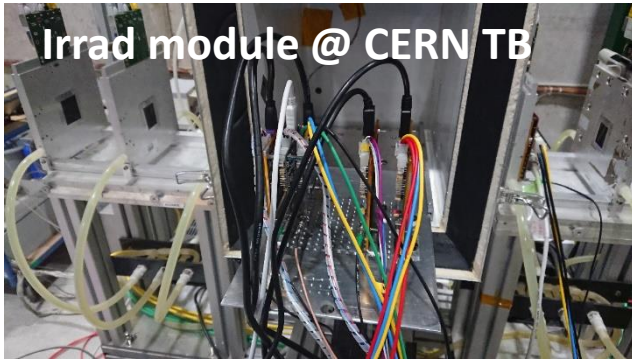
- CYRIC@Tohoku Univ. is an irradiation facility with 70MeV proton beam (~1μA).
  - This allows 5-6 pixel modules with backing Al plate at the same time(3% E loss/pixel).
  - Operated at -15℃ temperature with dry N_2 gas.
- Programmable X-Y stage and "push-pull" mechanism are implemented to the machine.
  - Choose to irradiate one or more target samples in max 15 pre-installed samples.
- Scanning over full pixel range during irradiation.
- **Actual Fluence difference relative to the target fluence is within ~10%.**

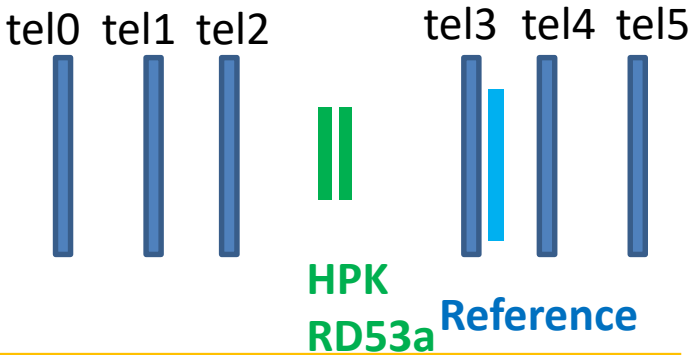




Testbeam at CERN SPS H6A/B

- To evaluate efficiency in pixel, performed testbeam before/after irradiation.
  - CERN H6 (Fermilab MT6) beam line
    - 120GeV pion (proton) beam
    - 7 testbeams in 2016-2018 at CERN and Fermilab
  - Typical CERN(Fermilab) TB
    - 6 layers of telescope
    - 3-5um(7-10um) pointing resolution
    - DUTs are in the cooling box

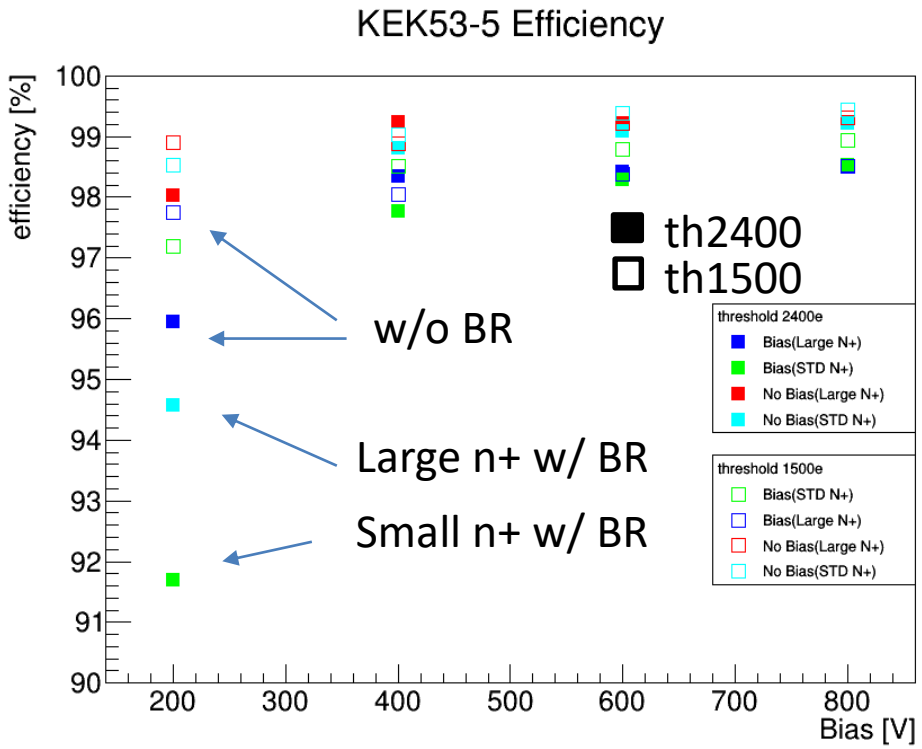


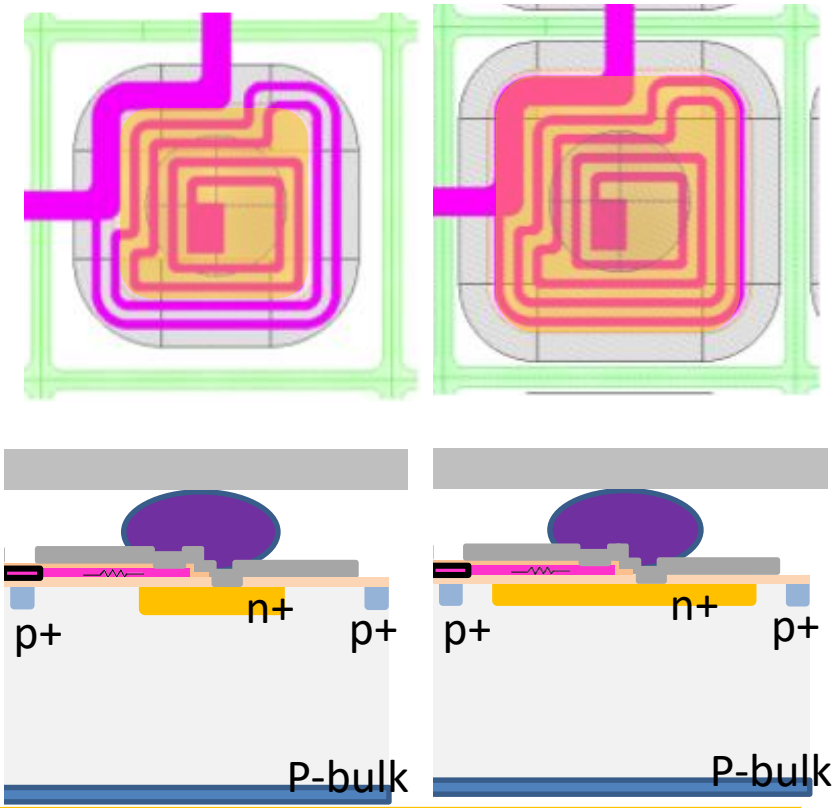


Efficiency result (irrad $3x10^{15}n_{eq}/cm^2$)

- Efficiencies of HV scan 200-800V have been evaluated.
  - **Analyzed both 1500e and 2400e threshold data for different types.**
  - **All types have over 98% efficiency at 600V.**
    - 1500e threshold results have over 99% efficiency.
    - Small n+ w/ BR have low efficiency at 200V

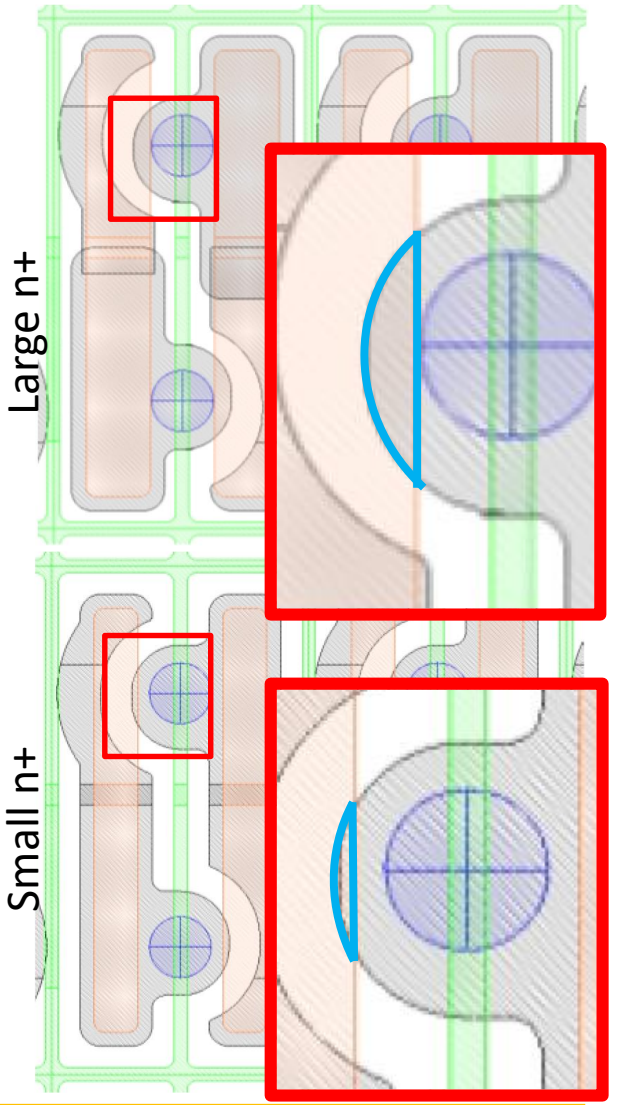
K. Nakamura Pixel 2018





25x100um^2 option

- To achieve better momentum resolution in the ATLAS detector, 25x100um^2 pixel size option exists using the same 50x50um^2 pitch ASIC.
  - **Inter-pixel capacitance must be higher than 50x50um^2 case**
    - **More cross talk is expected.**
    - **Smaller n+ electrode (smaller overlap) was compared.**
  - Bias structure also produces additional capacitance between pixels.



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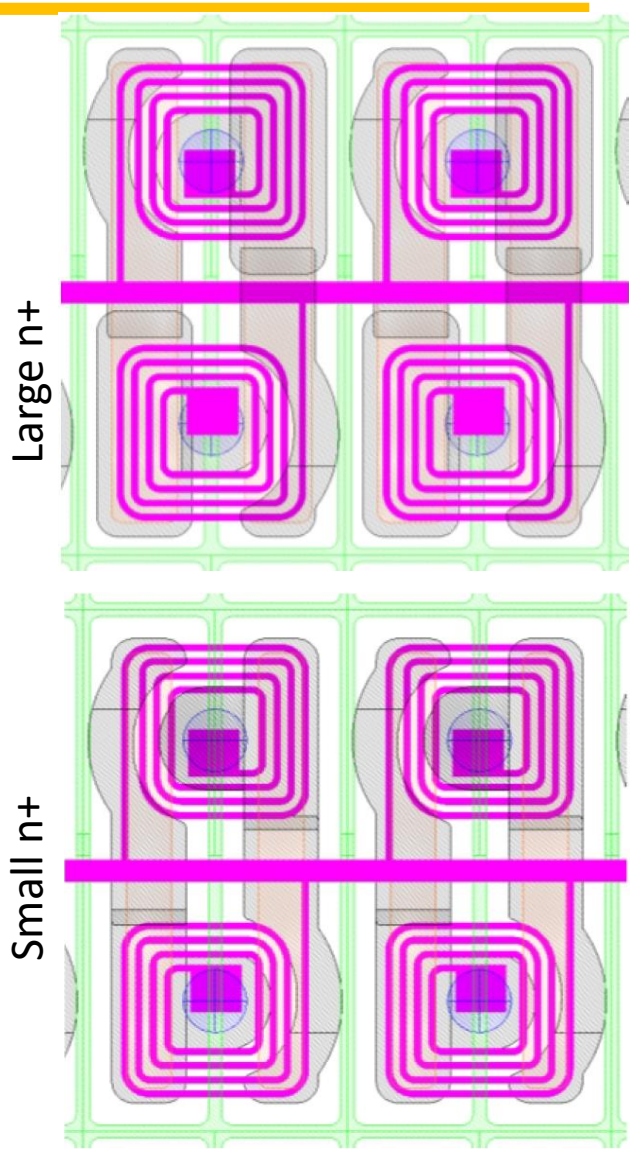
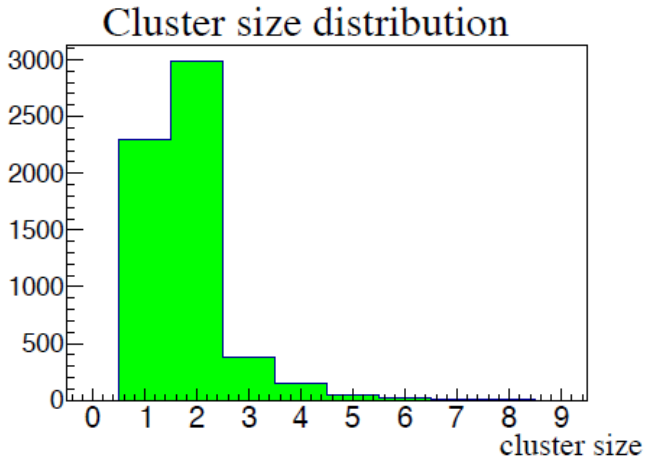
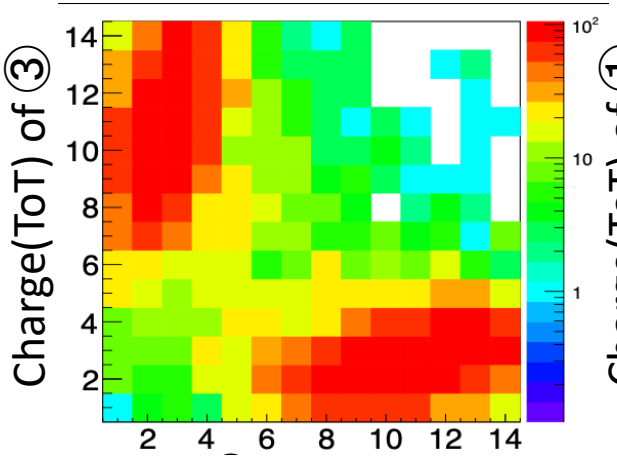


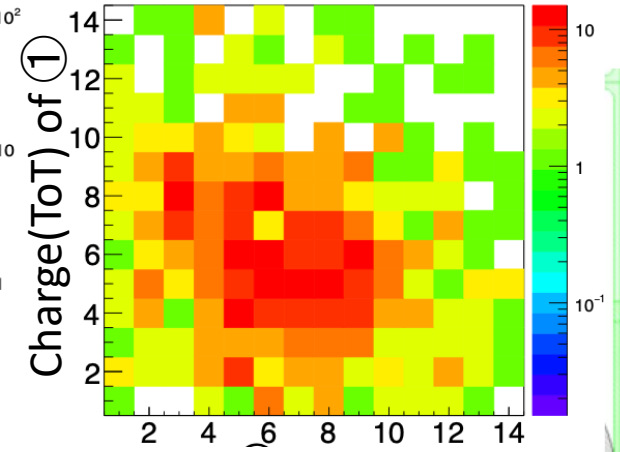
Cross talk

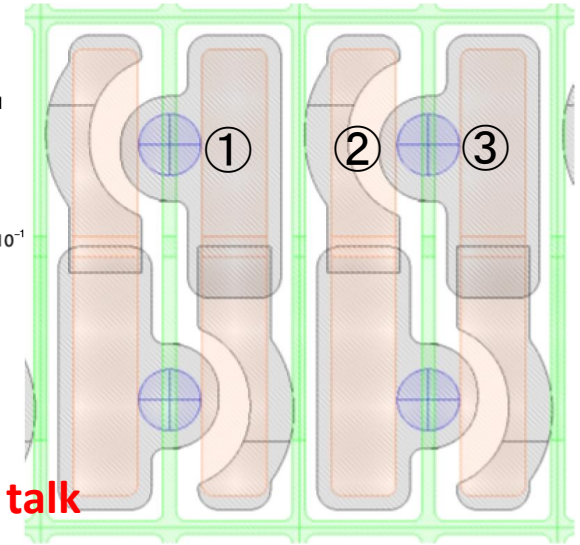
- In the testbeam data, cross talk has been checked with 1500e threshold.
  - Non-bias structure pixels
- # of hit pixels in a cluster
  - 43.5% of clusters have two hit pixels.
  - 86.5% of 2 hit clusters are coupled pixels(②+③) and 9.5% is uncoupled pixels (①+②)



# of hit in a cluster







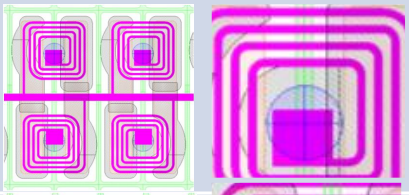
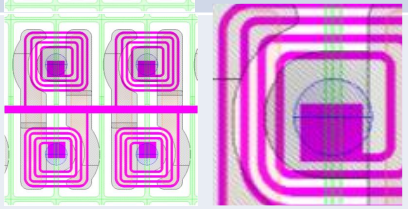
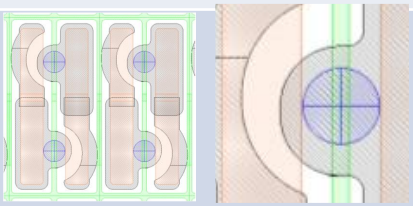
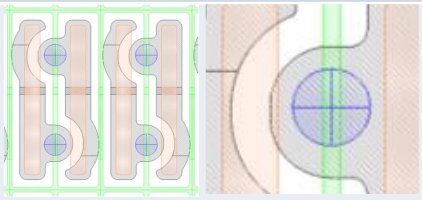
2 hit clusters with couple pixels seems dominated by cross talk

Amount of cross talk : **33.5%** @ non-bias str. @ 1500e threshold

Cross talk

- Tested 4 variations :

* Statistical uncertainty only

	Bias structure	N+ size	Cross talk fraction
	Yes	Large	46.7±0.59*%
	Yes	Small	52.9±0.61*%
	No	Large	33.5 ±0.78*%
	No	Small	21.9±0.77*%

Cross talk with the minimized overlap between n+ and Al is 21.9%

Biasing structure affect 15-25% increase of cross talk.

Conclusion and plan

- Conclusion
  - Develop optimized Hybridization technology with HPK for HL-LHC ATLAS phase-II upgrade.
  - Established hybridization method based on FE-I4 ASIC and quad size sensors.
  - Observed bump disconnection by CTE mismatch to the Flex PCB.
    - **At least 5um parylene coating works to reduce disconnection bump to 0.5% level after 200 thermal cycle [-40°C,40°C].**
  - Efficiency results based on the RD53A ASIC.
    - Non-irrad samples have over 99% efficiency
    - **Irrad modules have over 98 % efficiency for both w/ and w/o BR.**

→ **Fulfilled ATLAS ITK-pixel requirements**

  - Considered 25x100um^2 option with the same 50x50um^2 pitch ASIC.
    - Cross talks to the coupled pixel are visible (minimum 22% for small n+ w/o BR)
    - Still keep 50x50um^2 as baseline and decision will be taken soon.

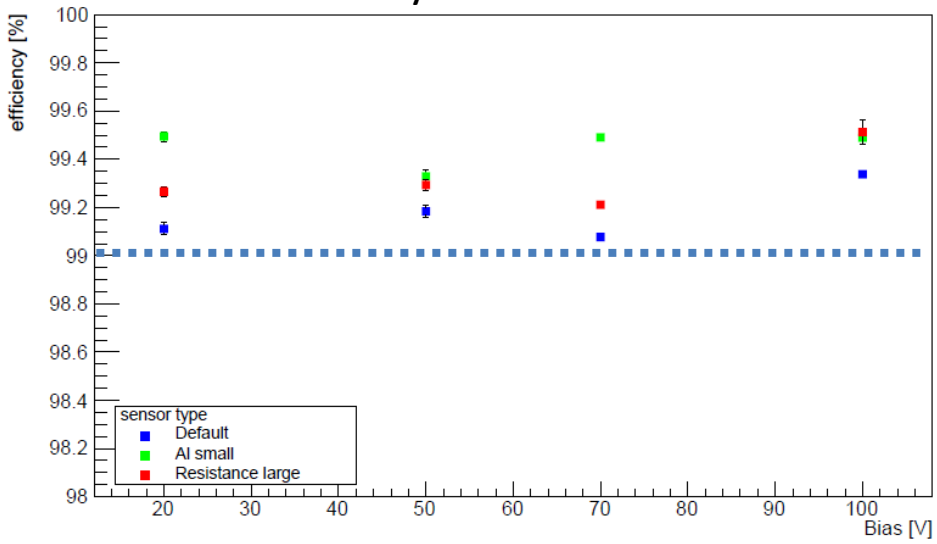
Contributors

backup

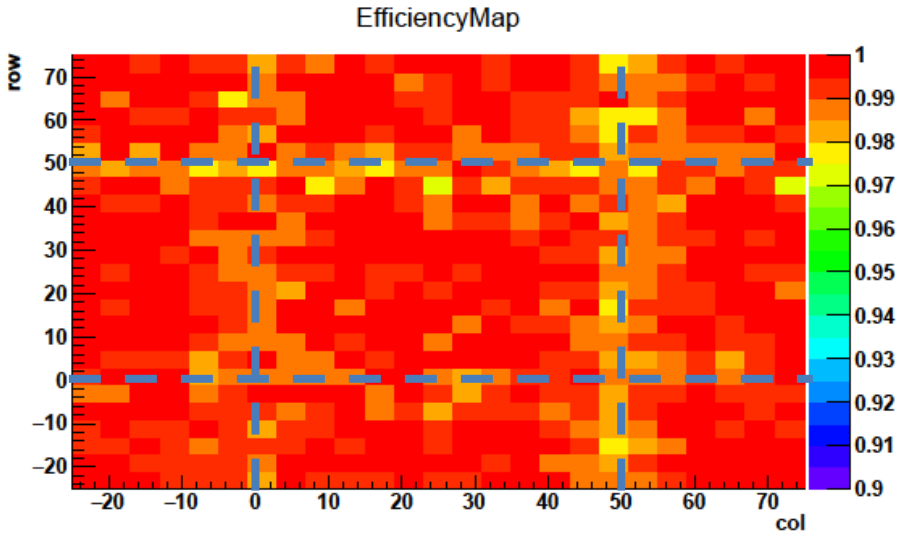
Efficiency results (non-irrad)

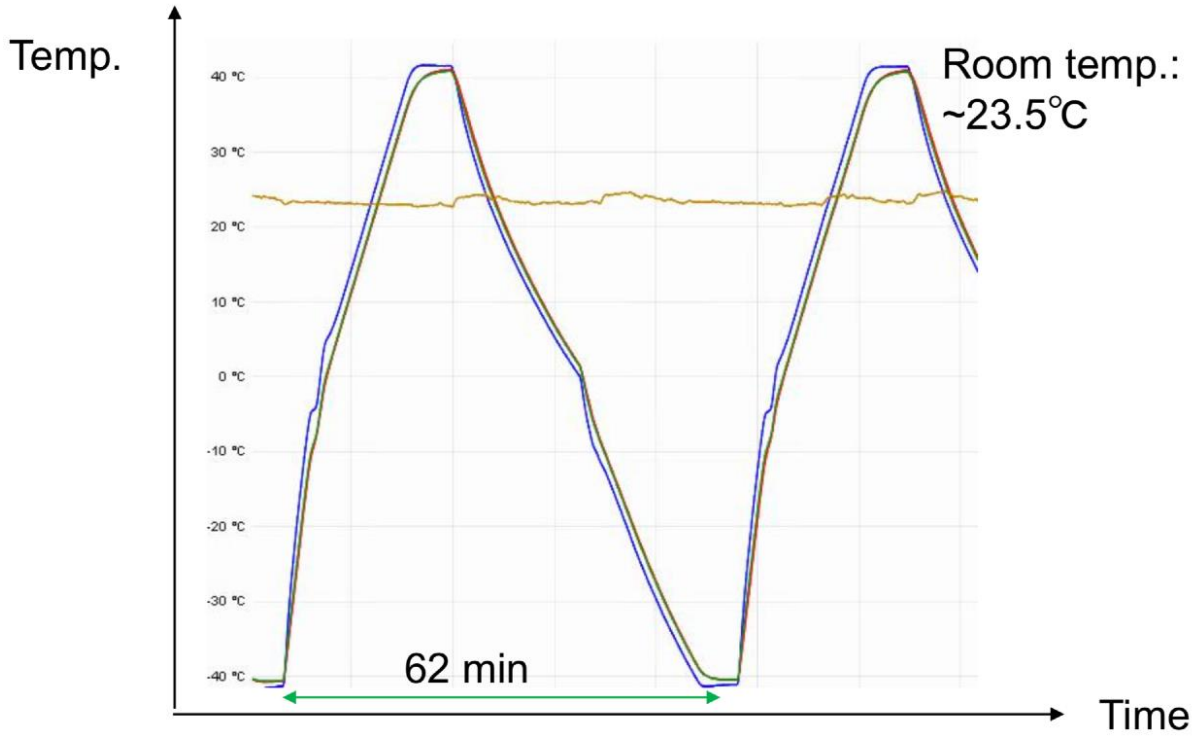
- Results with 2000e thresholds.
  - Efficiency is over 99% for all types.
    - Still checking the proper mask has been applied.
    - No visible efficiency drop at the corner of pixel.
  - 20V is already enough voltage to have 99% efficiency.

Overall efficiency



Default type Bias -100V




Temp.
40 °C
30 °C
20 °C
10 °C
0 °C
-10 °C
-20 °C
-30 °C
-40 °C
Room temp.:
~23.5℃
62 min
Time