Serial Powering for the Tracker Phase-2 Upgrade

Dominik Koukola on behalf of the CMS Tracker Group

Lopud Island, Croatia October 13-18, 2019

Outline

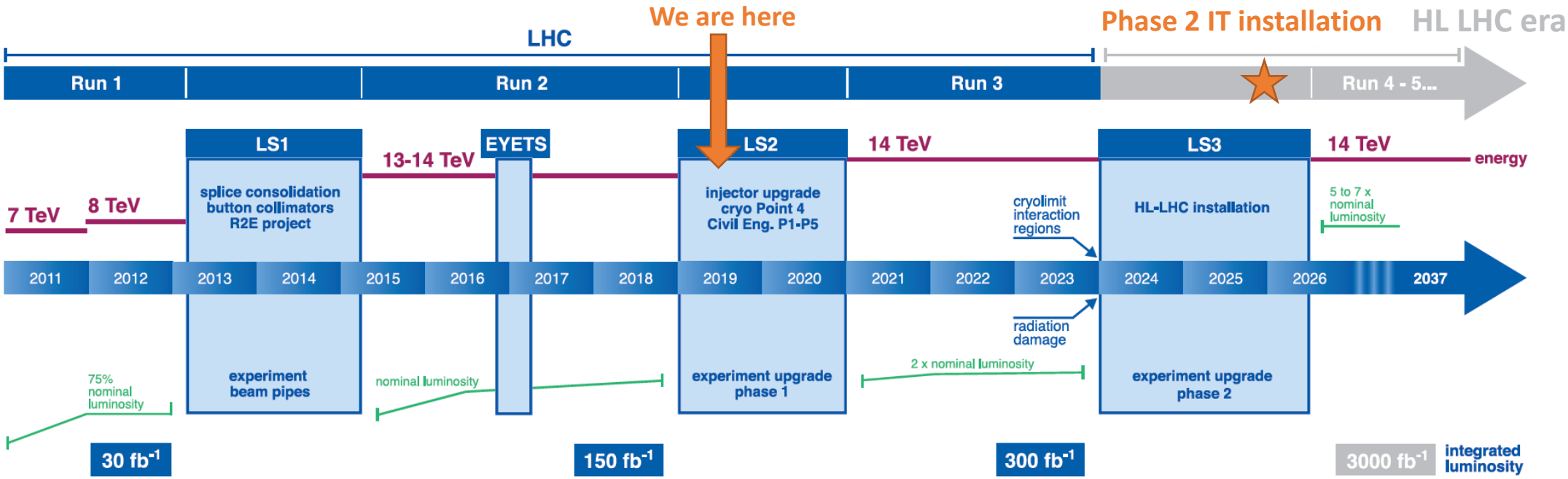
Serial powering scheme

- Introduction and motivation
- Shunt-LDO regulator and RD53A readout chip
- System issues

Recent system tests and developments

- Serial powering chains with RD53A Quad modules

LHC Plan



- ATLAS and CMS will upgrade their Inner Trackers for HL-LHC
- Both will use **Serial Powering** to power the pixel readout chips

  => Never been used in HEP experiments

- Presentation will give a CMS Inner Tracker biased view on Serial Powering
  - ➢ Largely also applicable for ATLAS Pixel ITk

Power related challenges for Phase 2 IT

HL LHC era will bring increased requirements for the Inner Tracker:

- ❑ High radiation levels up to:
  - Fluence of 2.3 x 10^{16} $n_{eq}cm^{-2}$
  - Total ionizing dose of 1.25 Grad

=> Radiation hard design

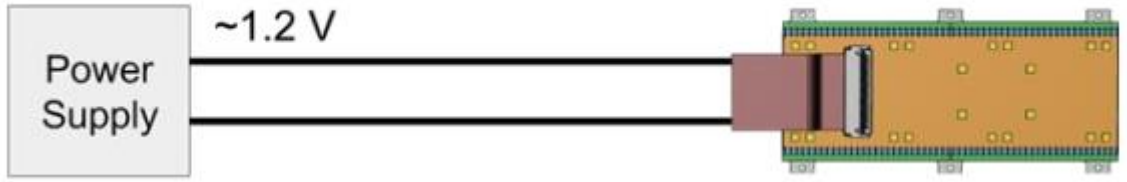
- ❑ Increased latency, granularity and hit rate:
  - Big buffers, many pixels, high bandwidth

=> High supply current (~2A / chip)

- ❑ Minimize material budget for good tracking performance:
  - Light cables and mechanical structures
  - Tight space constraints
  - CO_2 cooling

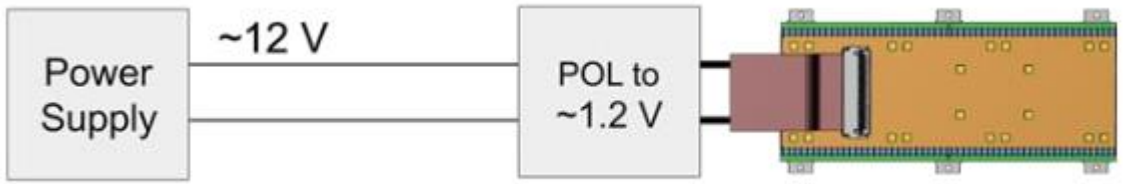
=> Compact and low mass design

Why serial powering?



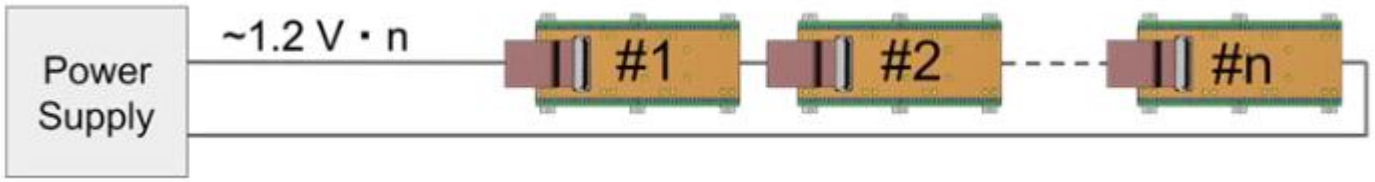
Direct parallel powering

- Requires many thick cables to maintain voltage



Parallel powering with DCDC converters

- Not sufficiently radiation hard
- Space limitations



Serial powering

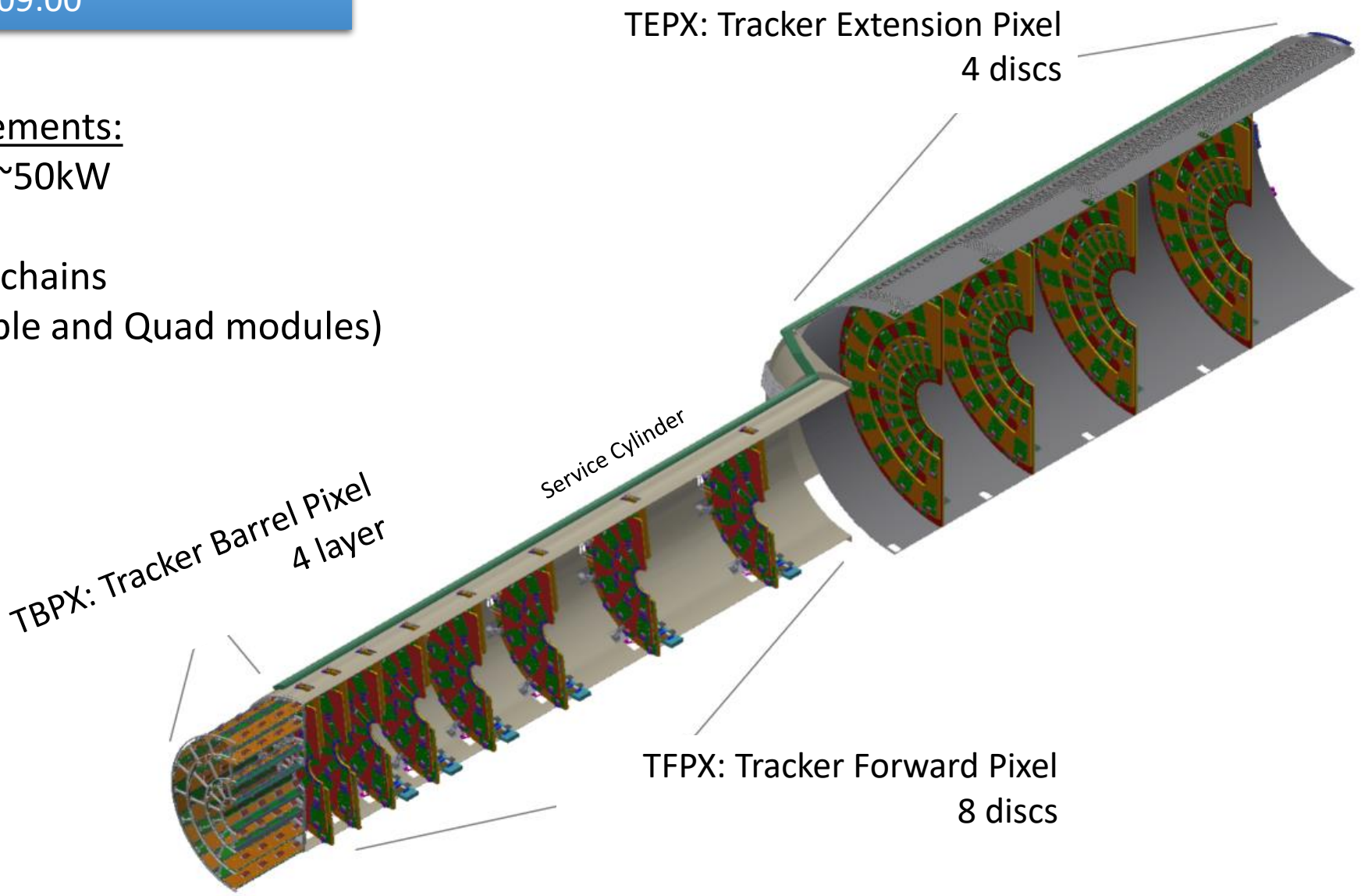
- Fewer (n≈8 times) and lighter cables

CMS Inner Tracker Phase 2 Overview

More in talk on “CMS Inner Tracker Upgrade ” by Panja Luuka Tuesday 09:00

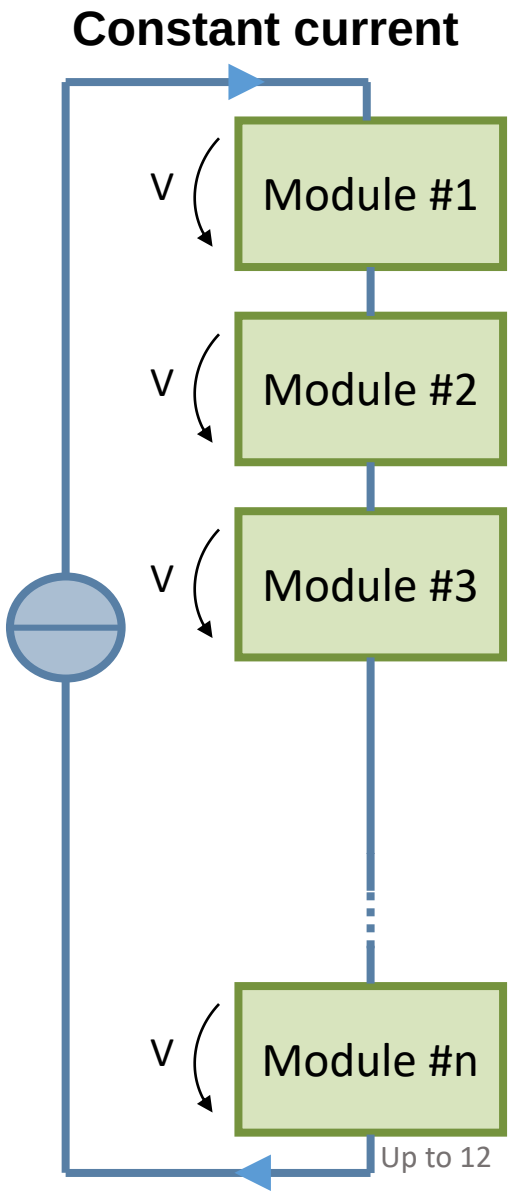
Serial powering requirements:

- On-detector power ~50kW
- Supply current ~3kA
- 500 serial powering chains
- 3900 modules (Double and Quad modules)



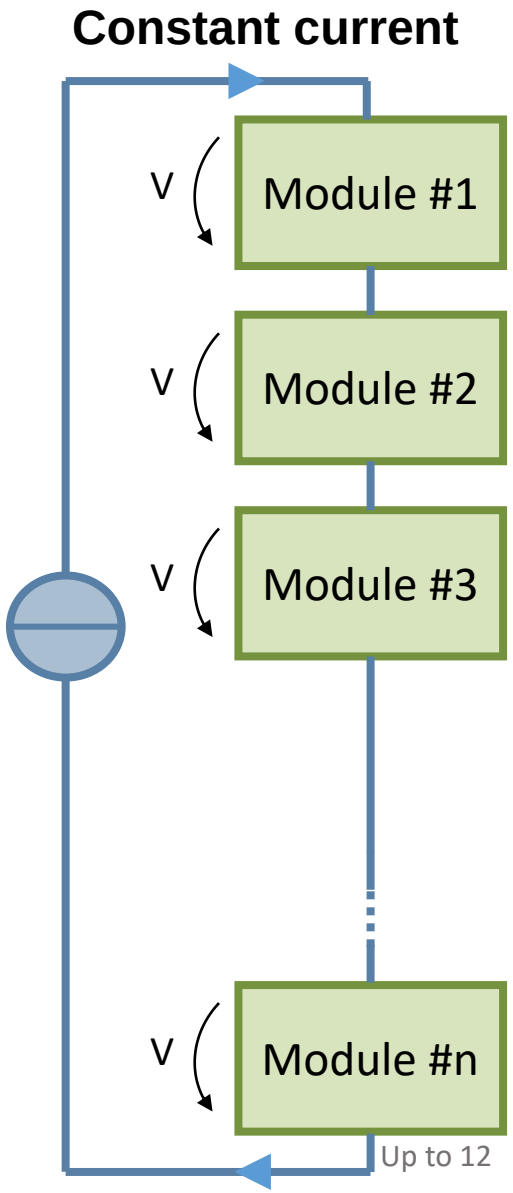
Serial powering scheme

Serial powering scheme



- Serial chain is powered with a **constant input current**
- Up to 12 modules are connected in series in a **serial chain**
  - Modules have **different local grounds**
- Current based powering system => Insensitive to voltage drops on cables

Serial powering scheme



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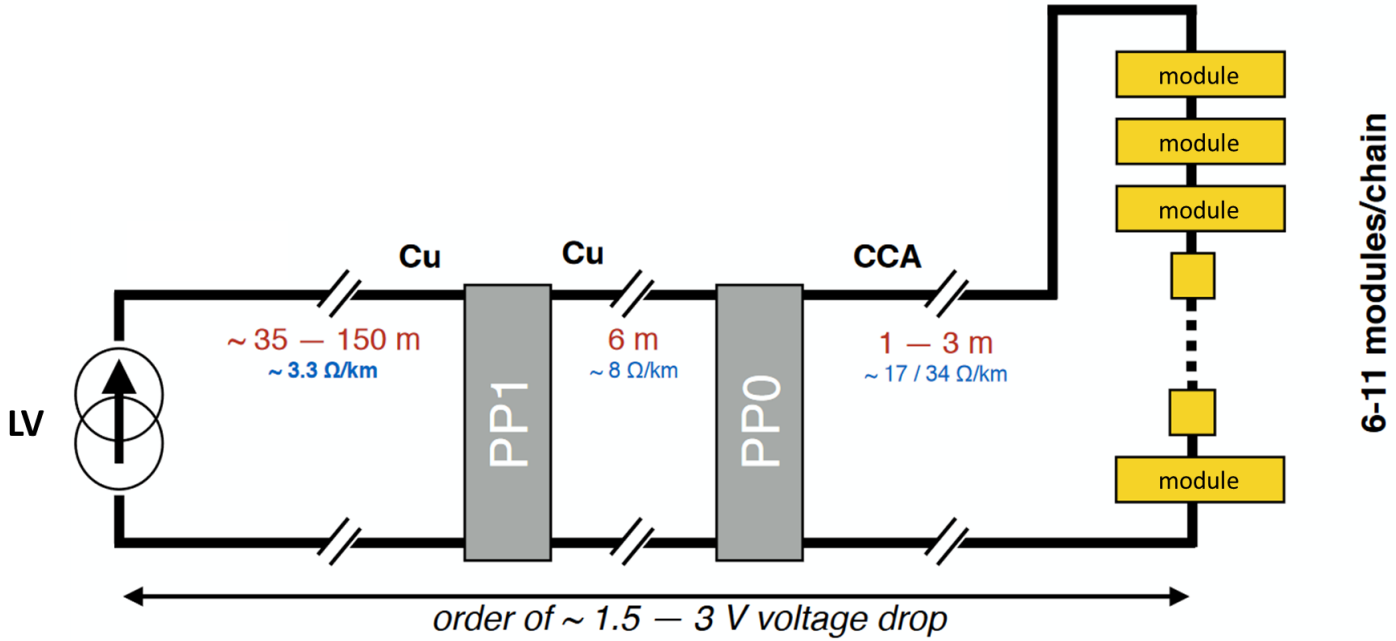
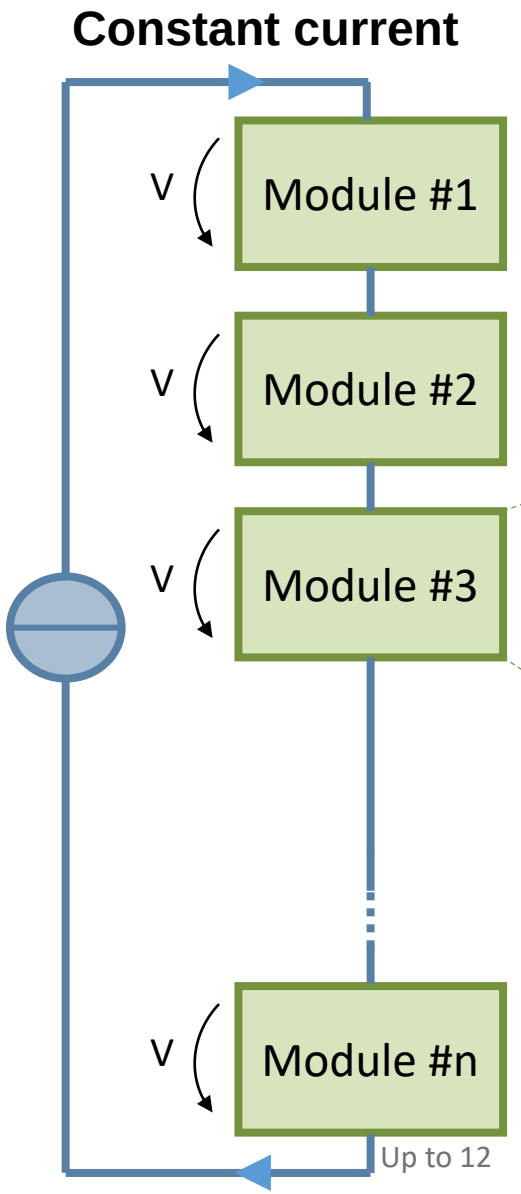
- No auxiliary on-detector electronics needed for serial powering
  - ➢ Only cabling between power supply and readout chips



Serial powering scheme



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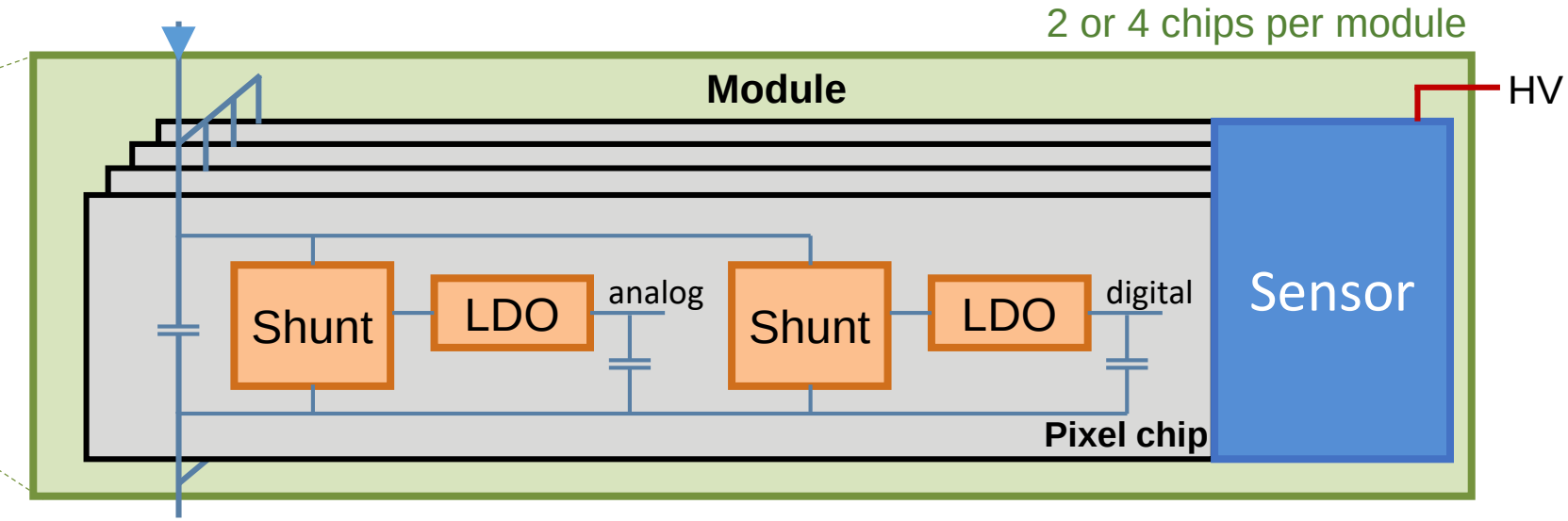
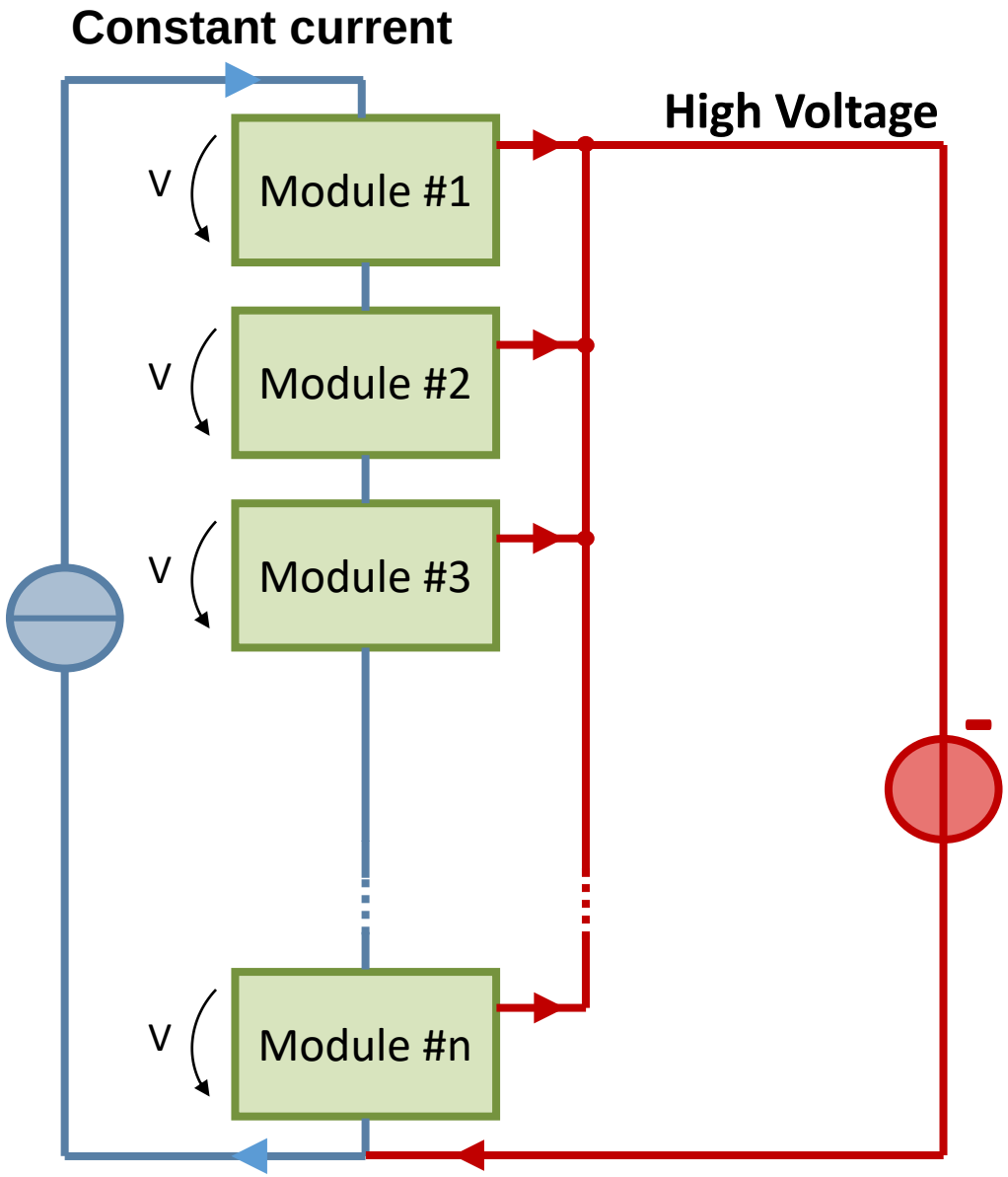


- Chips (2 or 4) on a module are powered in parallel
  - ➢ The constant input **current is shared** between the chips on a module
- Two power regulators are integrated in each chip
- Chips on a module share one sensor

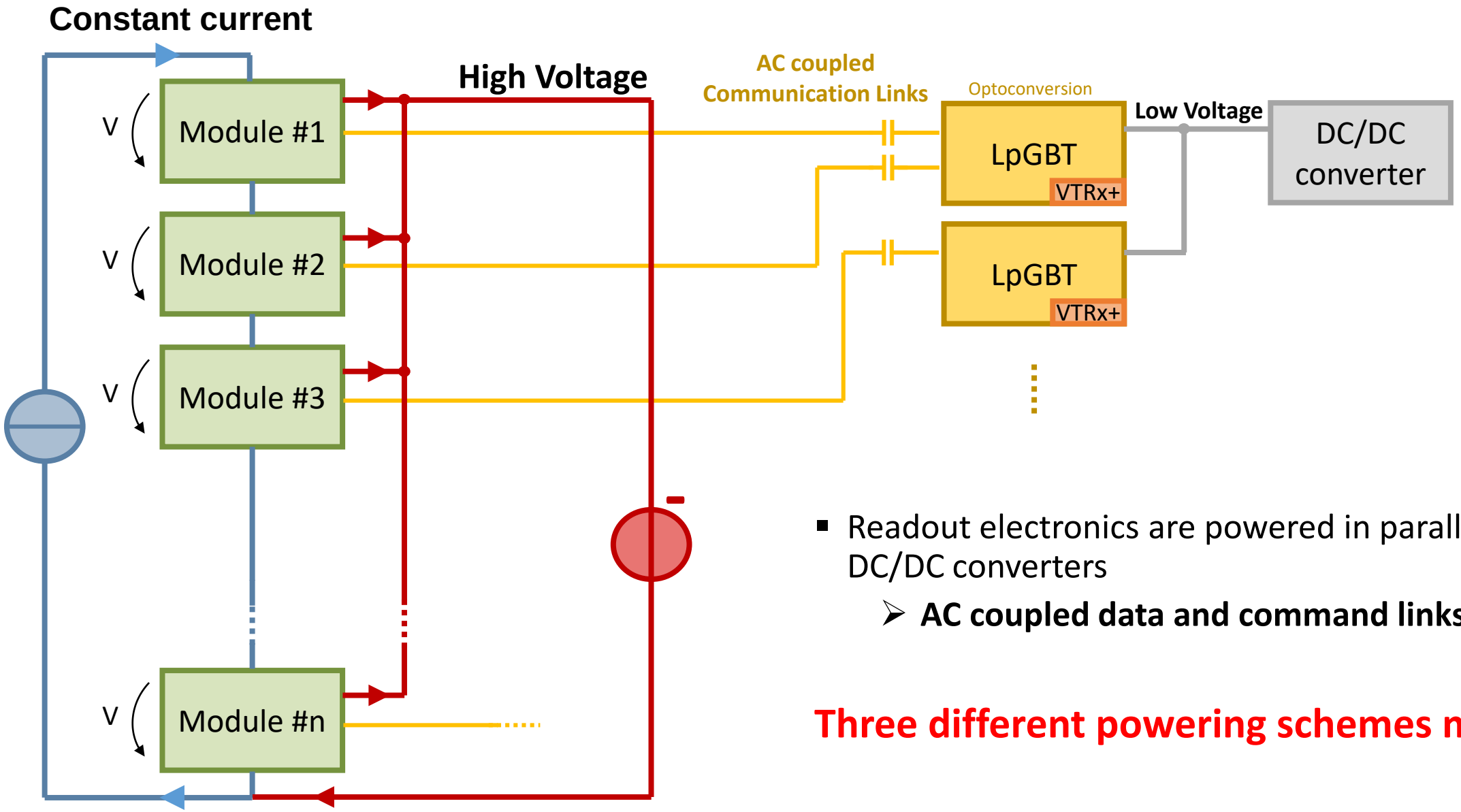
High voltage bias for Sensors



- High voltage is **provided in parallel**
  - Baseline choice is **one parallel HV supply line** per serial chain
- HV return path is through the serial chain

- Modules have different local grounds
  - Sensors see different HV due to different ground potential
  - **Up to 20V differences** in sensor HV in a chain
    - => Not problematic for planar sensors
    - => For 3D sensors higher HV granularity foreseen
  - **Sensor forward biasing possible when HV off and LV on**
    - => Several solutions to avoid this

On-detector readout electronics



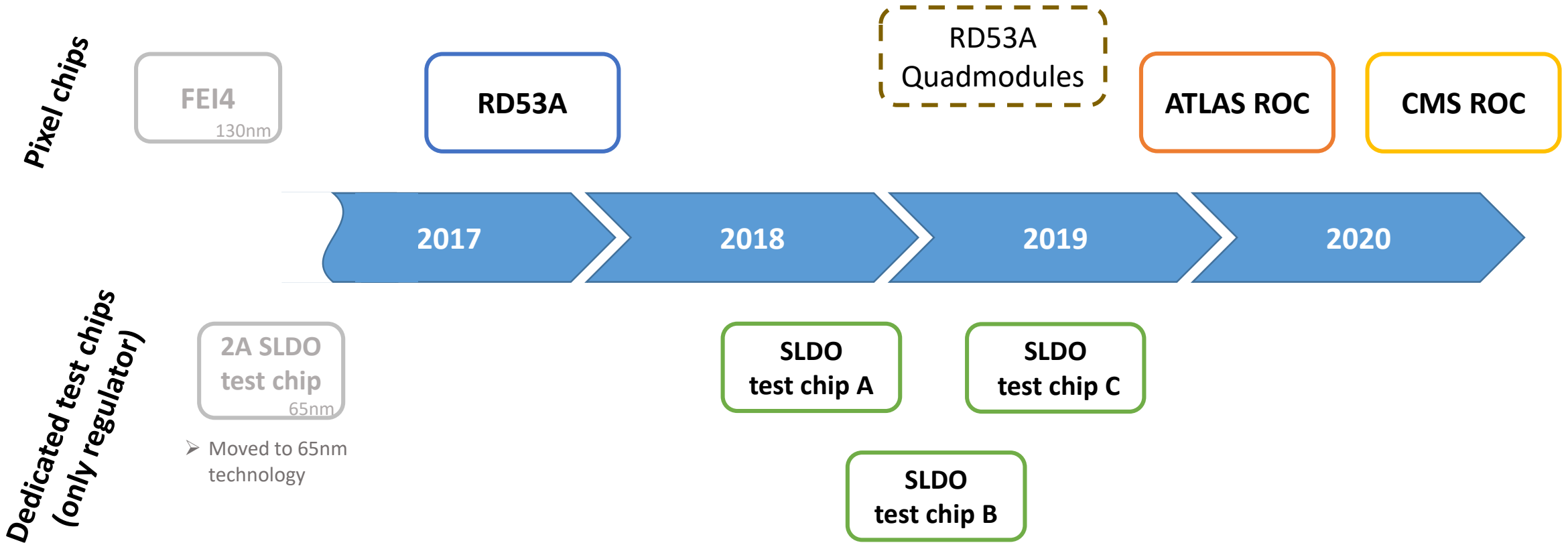
- Readout electronics are powered in parallel with DC/DC converters
  - **AC coupled data and command links required**

Three different powering schemes mixed!

Shunt-LDO regulator
&
RD53A readout chip

Overview of recent chips with Shunt-LDO regulators

- Date corresponds to the first (expected) availability

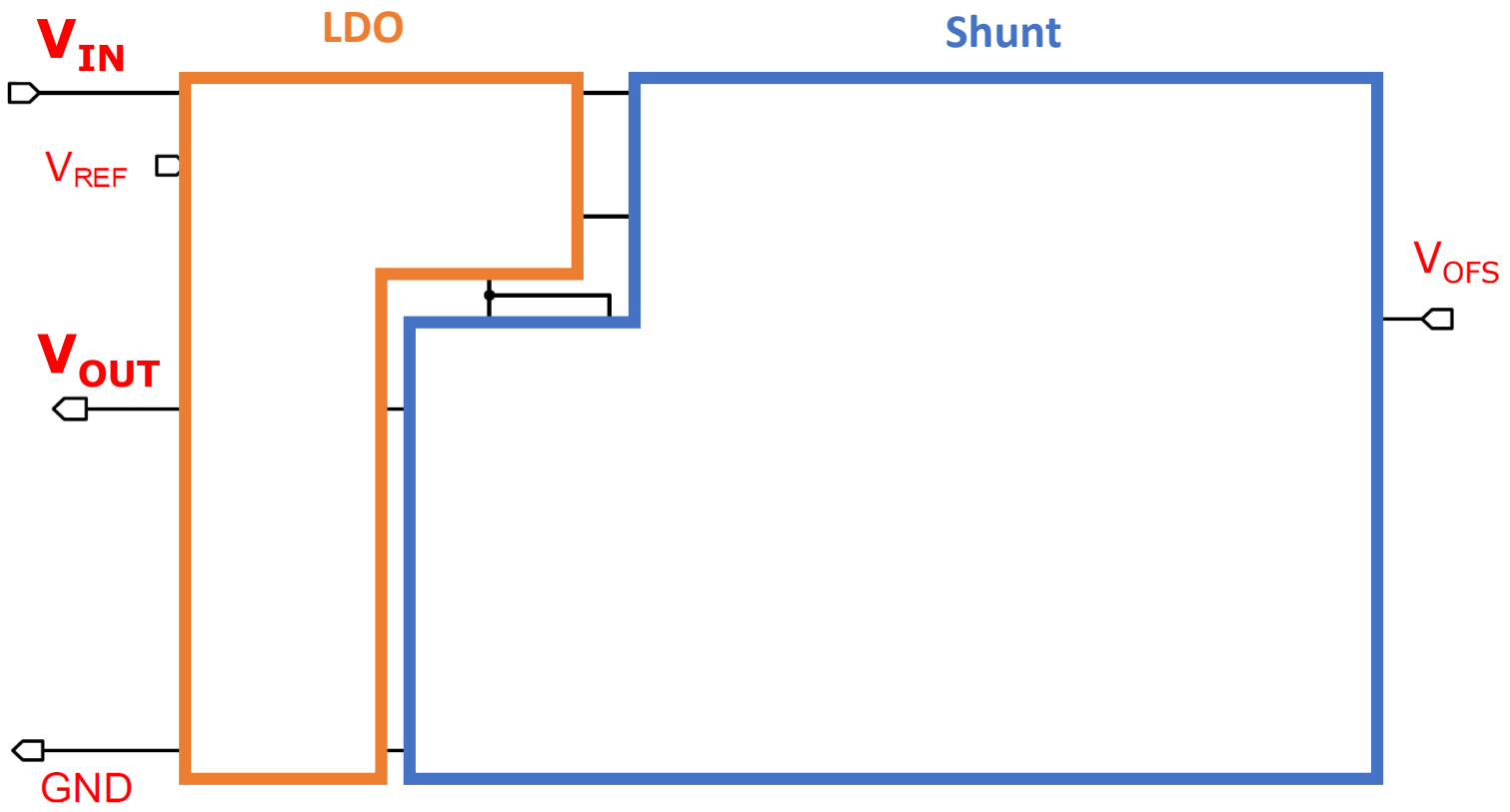


Improved performance (Startup, voltage accuracy, ..)
New features (Overvoltage/overload protection, ..)

Shunt-LDO regulator

“Constant current to constant voltage converter”

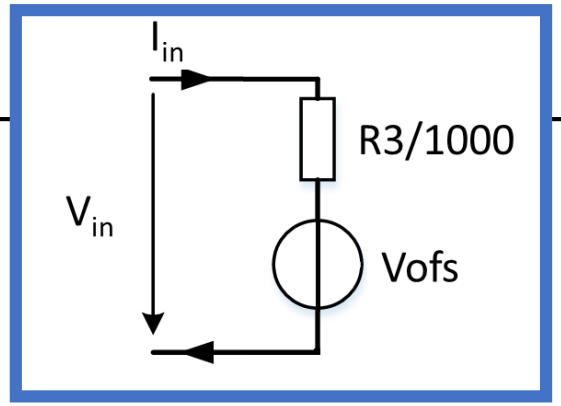
- Combines two functionalities: **Shunt** + **LDO**

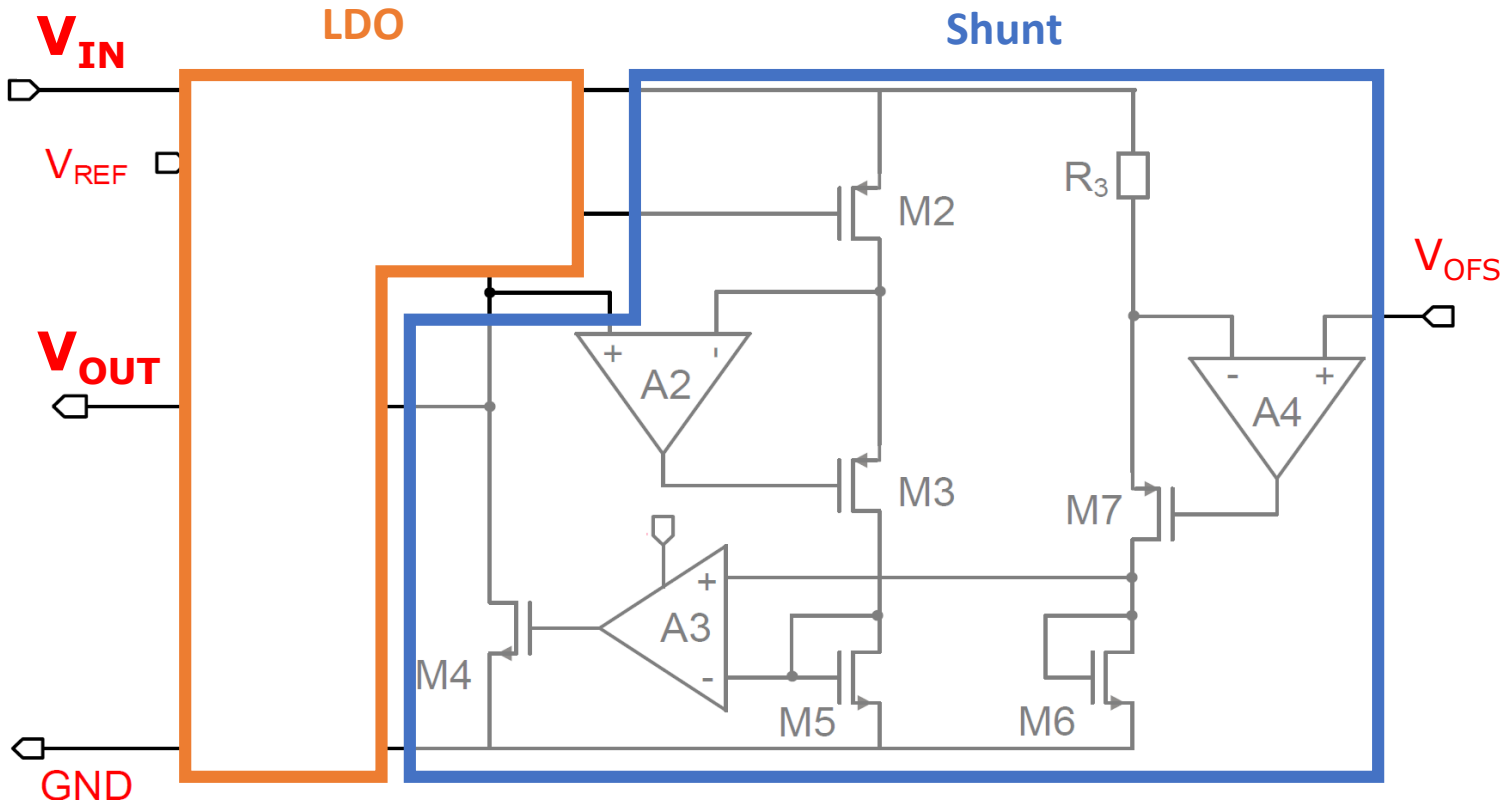


Shunt-LDO regulator

Shunt part:

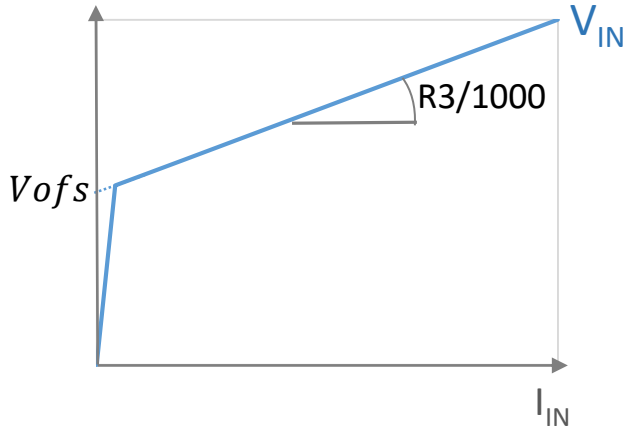
- Regulates input voltage => resistive behavior
- Shunts not used current to ground





Relationships

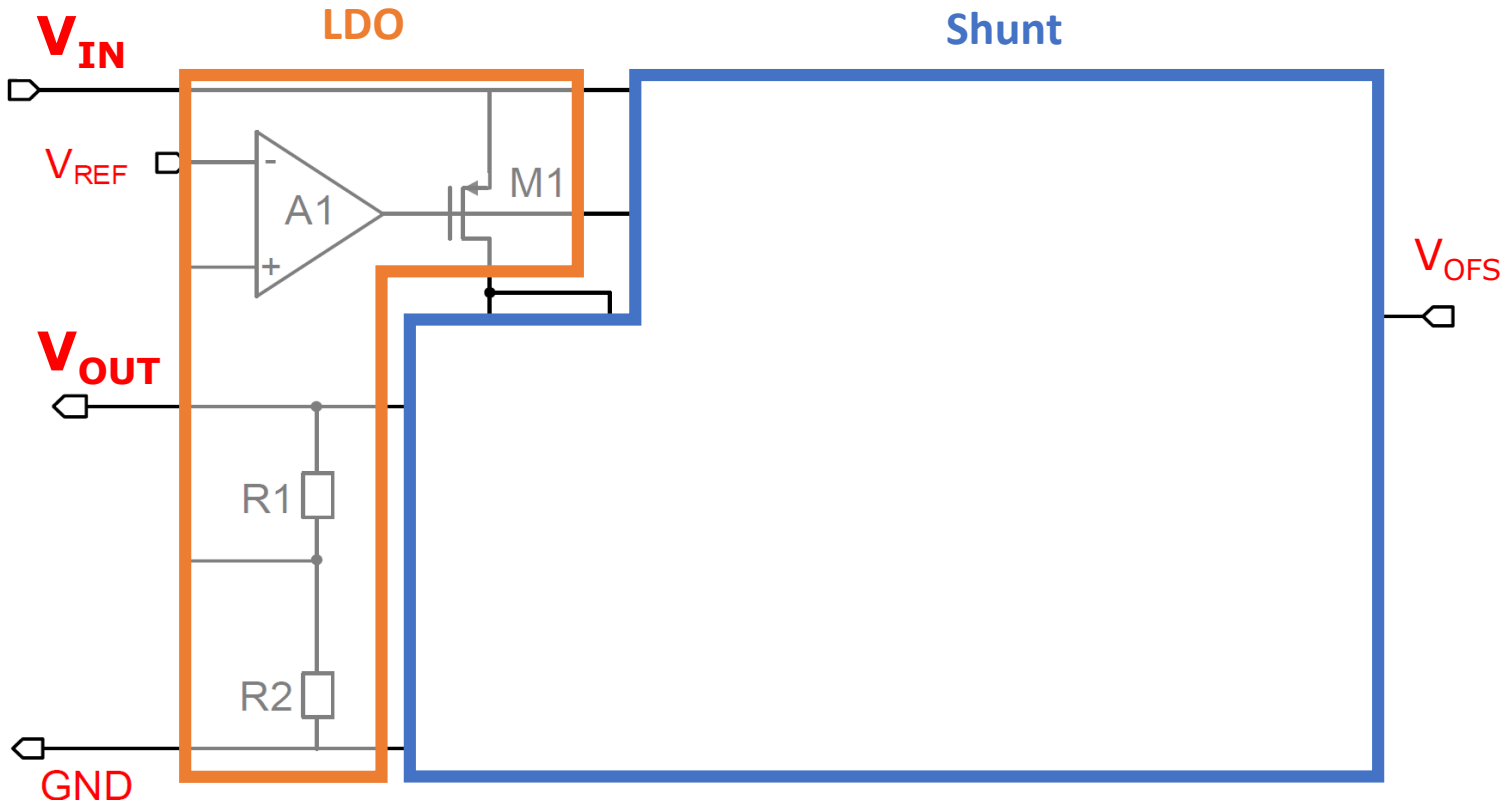
$$Vin = Vofs + \frac{R3}{1000} * Iin$$



Shunt-LDO regulator

LDO part:

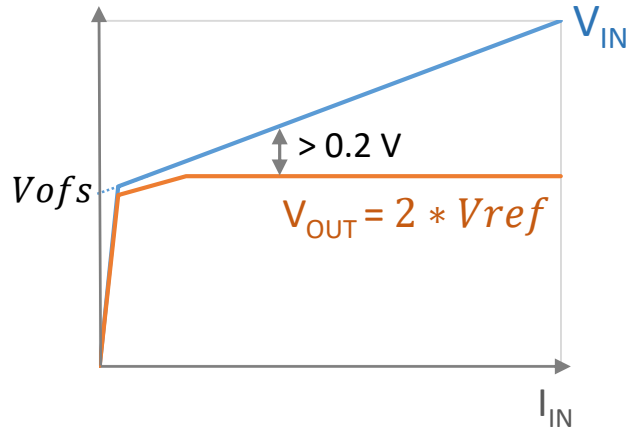
- Provides constant output voltage
- Requires 0.2 V drop out voltage => Vin > Vout + 0.2V



Relationships

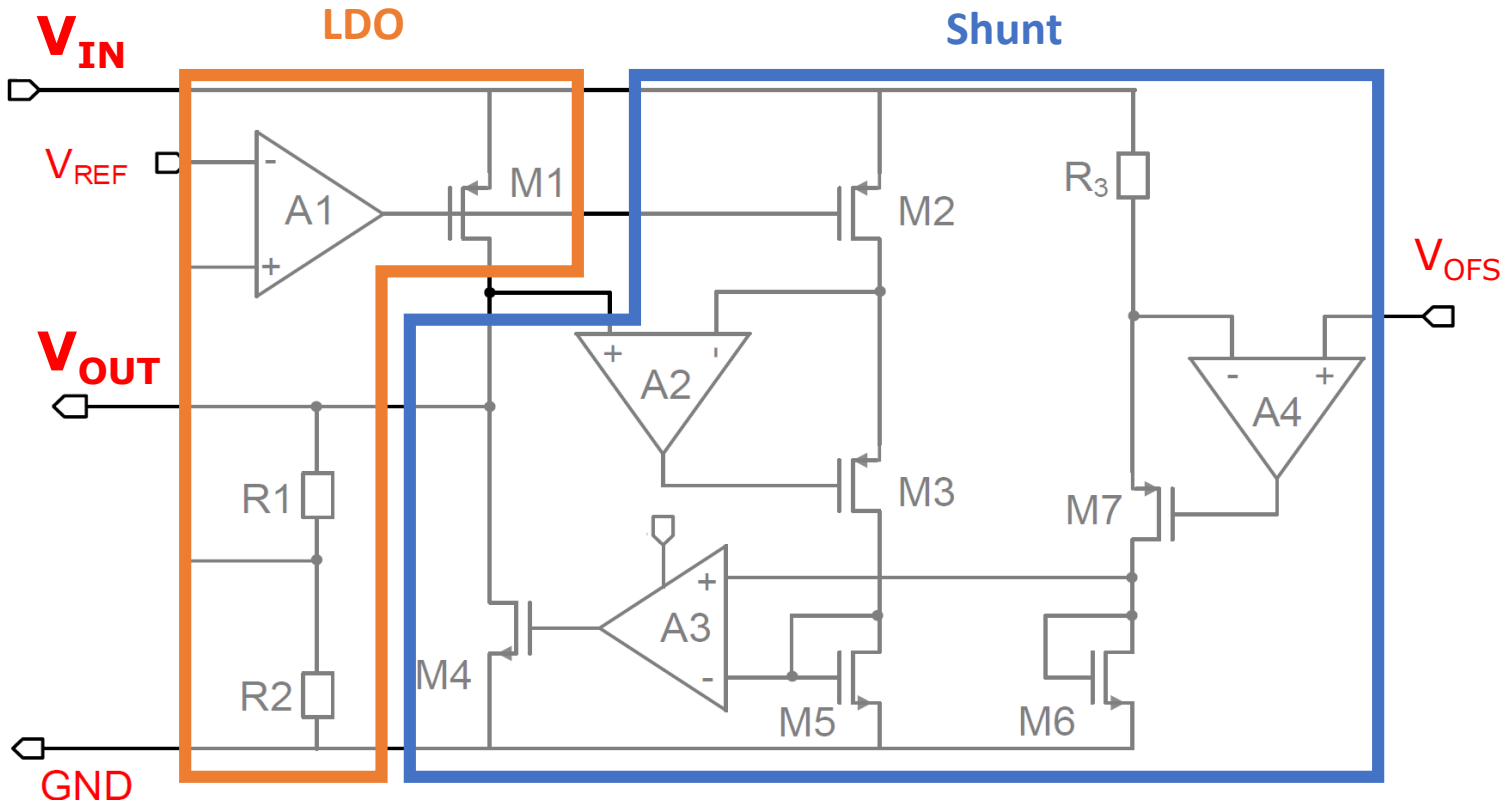
$$Vin = Vofs + \frac{R3}{1000} * Iin$$

$$Vout = 2 * Vref$$



Shunt-LDO regulator

- Resistive input behavior
- Provides constant voltage to the chip
- Input impedance, Vofs and Vref **are configurable**



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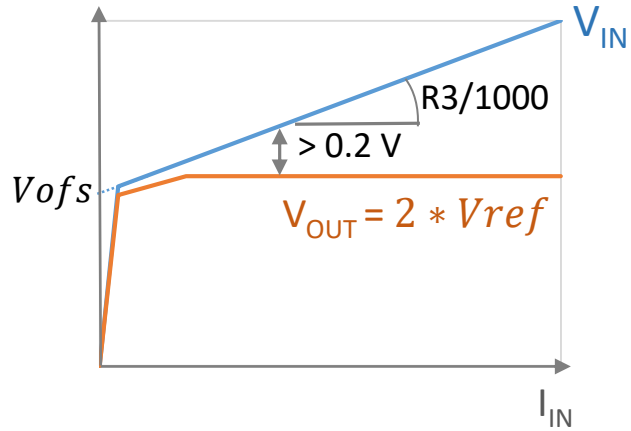
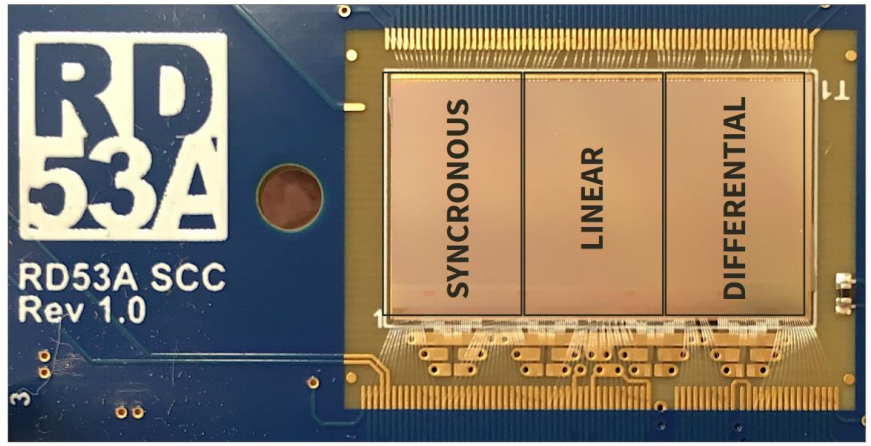


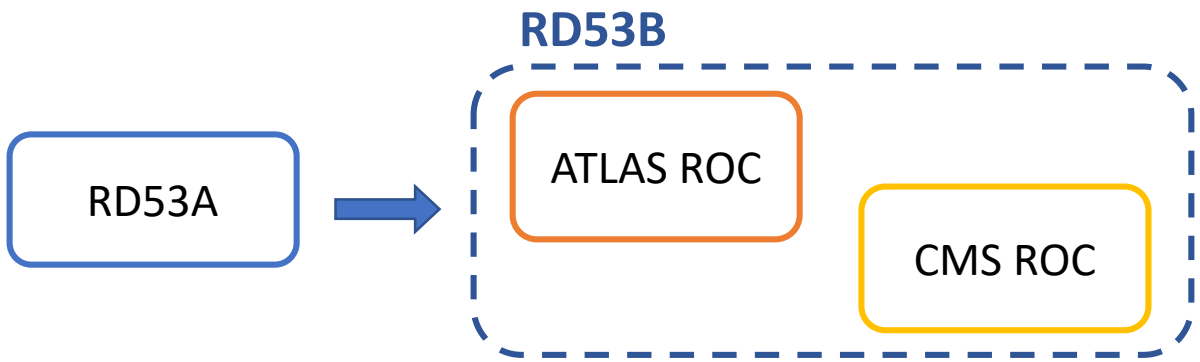
RD53A readout chip

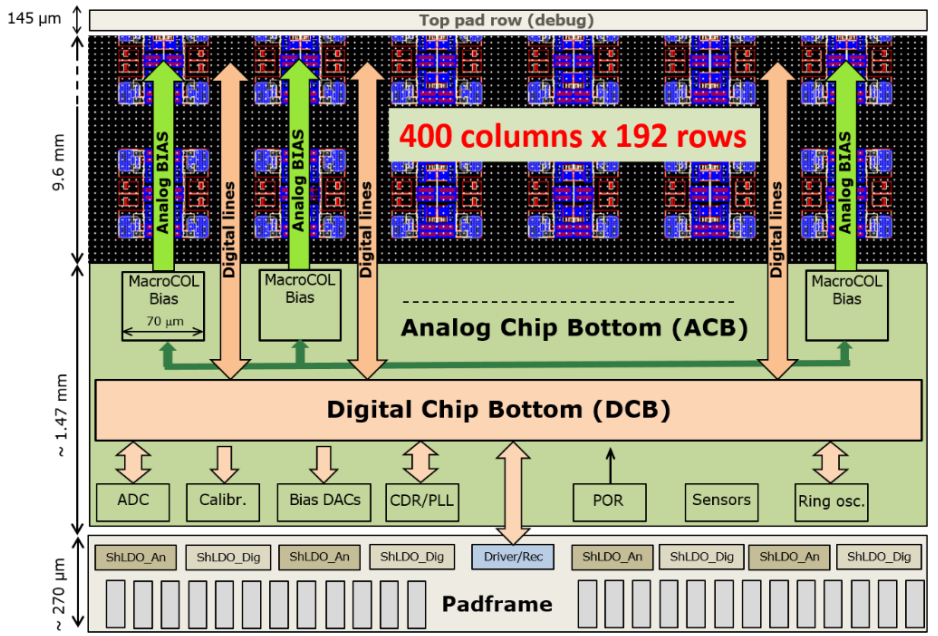
Demonstrator pixel readout chip designed by the RD53 collaboration (22 institutes - ATLAS and CMS)

- 400x192 pixels (50x50 μm^2 each)
- Three analog front end architectures
- ½ size of final chip => ~ ½ power (~1A)
- 65nm CMOS technology => 1.2V core voltage
- Radiation hardness > 500 Mrad



Final prototype of production chips expected in 2020:

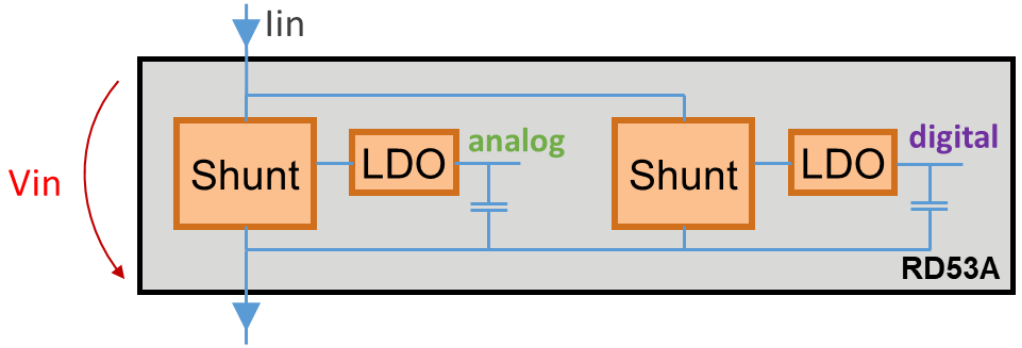




More in talk on “RD53 analog front-end processors” by Luigi Gaioni Tuesday 15:00

RD53A readout chip - Power

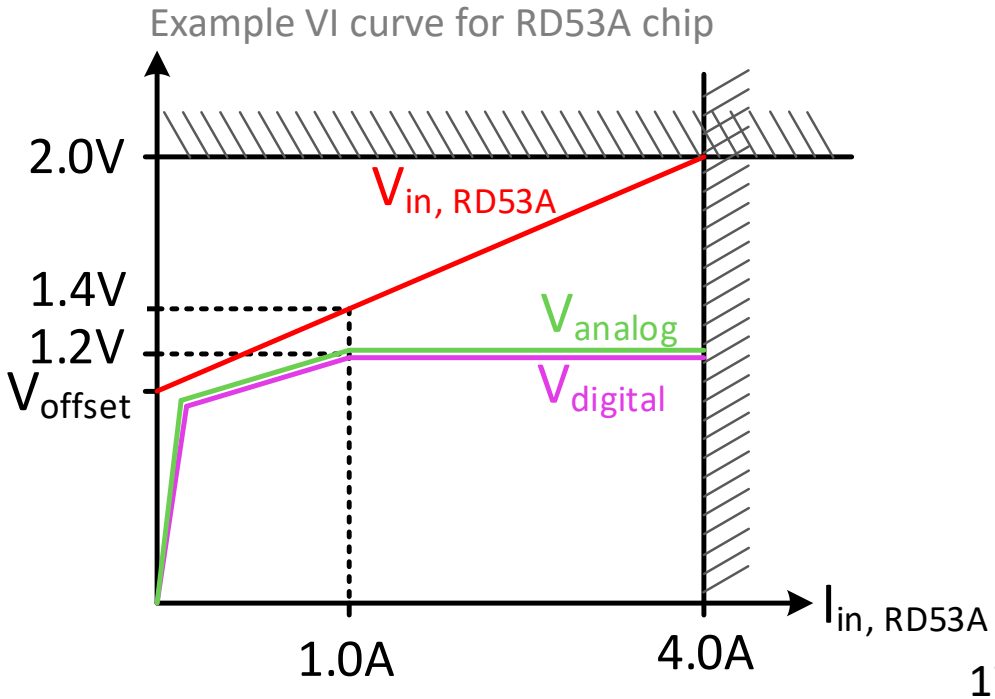
- ½ size of final chip => **~ ½ power (~1A)**
- 65nm CMOS technology => **1.2V core voltage**



- **Two power domains** => one for digital, one for analog
  - ➢ To decouple noisy digital from sensitive analog

- **Two Shunt-LDO regulator integrated** (one per domain)
  - Dimensioned for production chip
  - Can take 2A each => more than twice the expected load of final chip
  - Maximum input voltage 2V

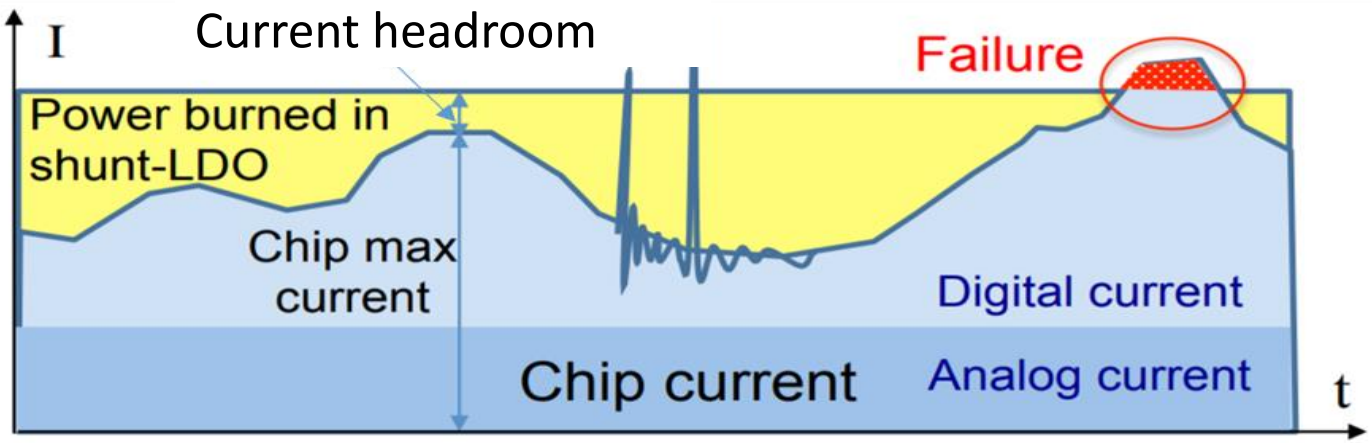
- **Three powering modes:**
  - ➢ Shunt-LDO mode (nominal mode)
  - ➢ LDO mode (Shunt disabled)
  - ➢ Direct (Shunt-LDO bypassed)



System issues

Constant supply current

Constant input current



Example current consumption of one readout chip

- Need to **provide enough <u>constant</u> current** for the chip to operate:

$$I_{constant} = I_{Max\ chip} + I_{headroom}$$

- **Surplus current is dissipated** in shunt part of regulator => **intrinsically inefficient**
- Load variations on chip are not propagated to power supply => resistive load to power supply
- If more current is drawn than provided (overload), regulator will fall out of regulation

  => Fast transients are filtered by external decoupling capacitors

- **Headroom also needed to cover imbalances in current sharing among parallel chips**

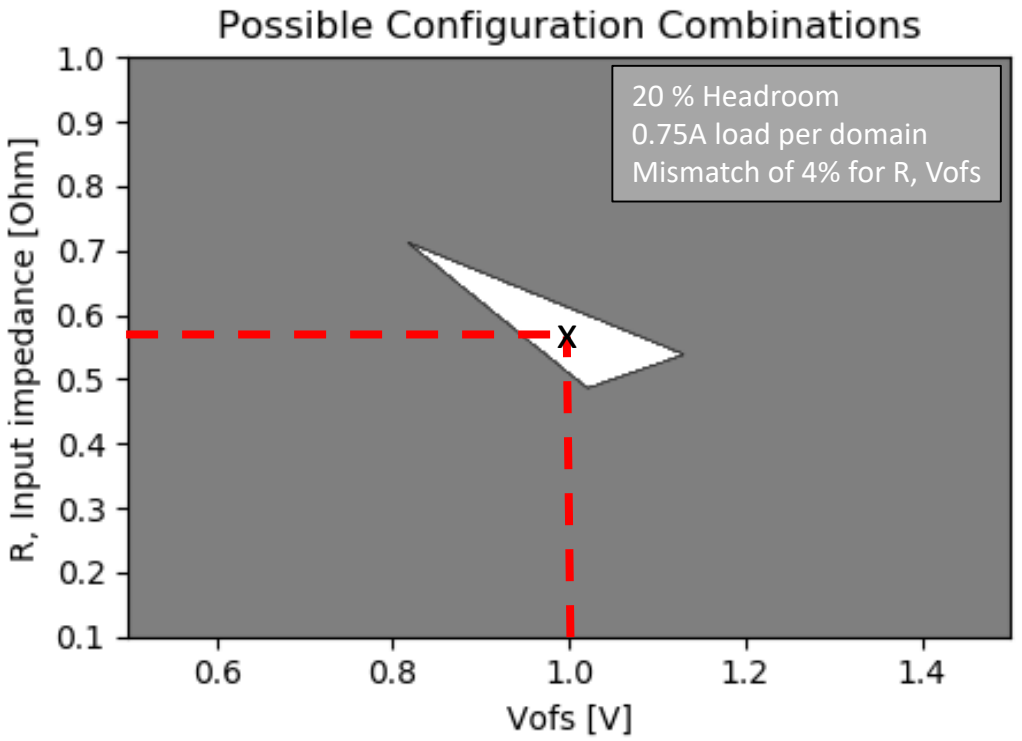
Optimizing the working point

- Optimize choice of: **Current headroom, Input behavior (slope, offset)**
- Goal is to have **power efficient and reliable powering** => compromise between the two

Low headroom

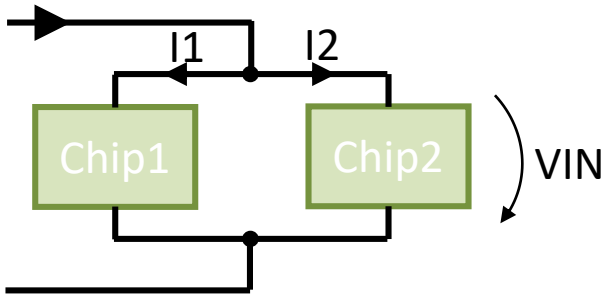
Sufficient current (> max load)
Sufficient voltage (> 1.4V)

- **Mismatches and parasitics need to be taken into account**
- First studies confirm that **20% headroom** is sufficient to cover estimated mismatches



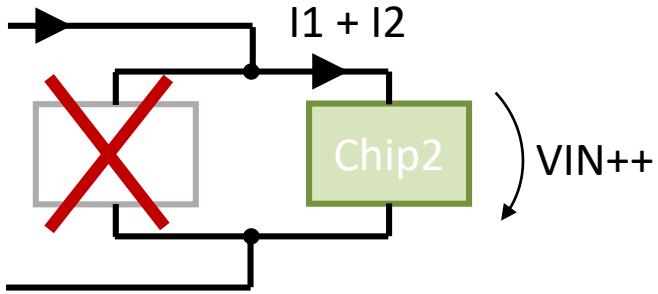
Typical failure cases

Normal operation



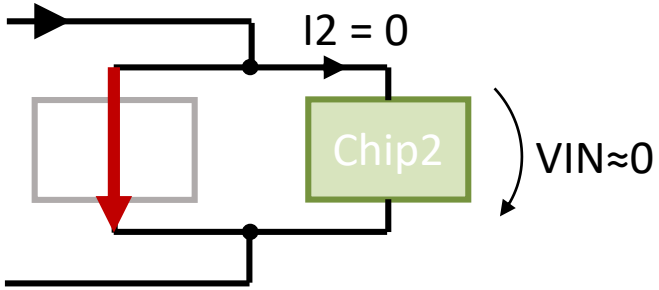
- Current is shared equally between parallel chips

Open on one chip



- Remaining chip has to take **double the current**

Short on one chip



- All current goes through shorted chip
- Parallel chips don't receive power anymore

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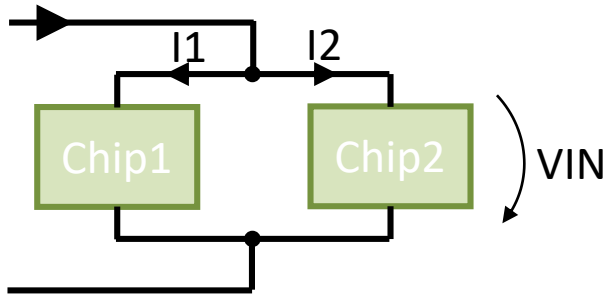

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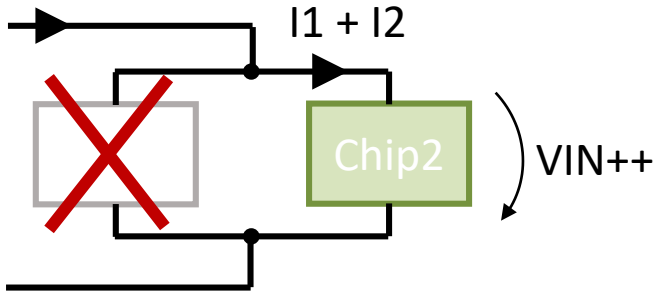

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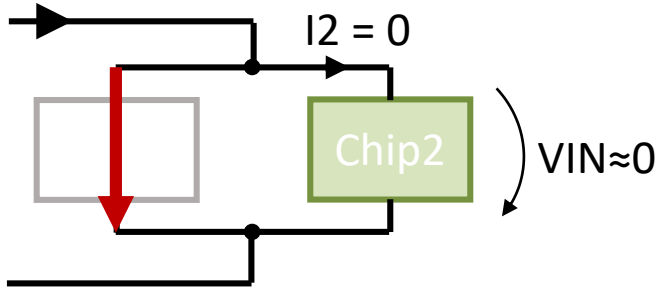

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- Parallel chips don't receive power anymore

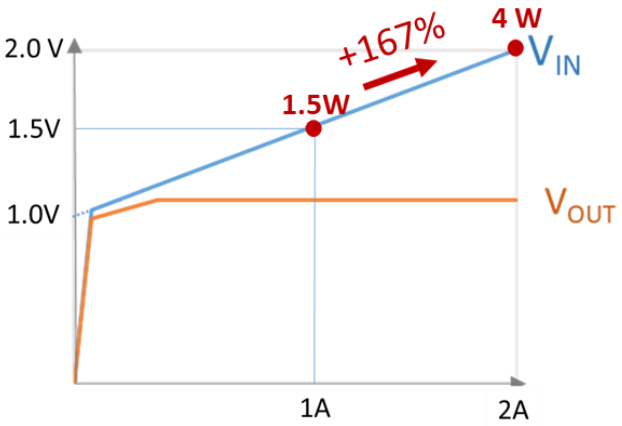
- **Serial powering chain stays operable when one chip of a module fails**
  - Shunt-LDO designed to take twice the nominal operation current
- Additional protection features have been added since RD53A
  => **Overvoltage & Overload protection**

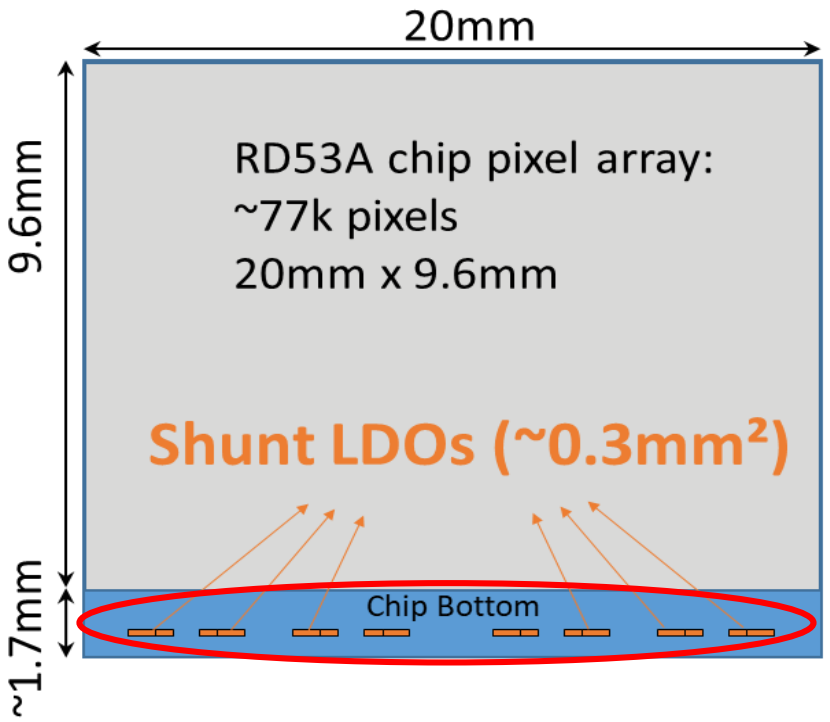
Hotspots and possible temperature gradient

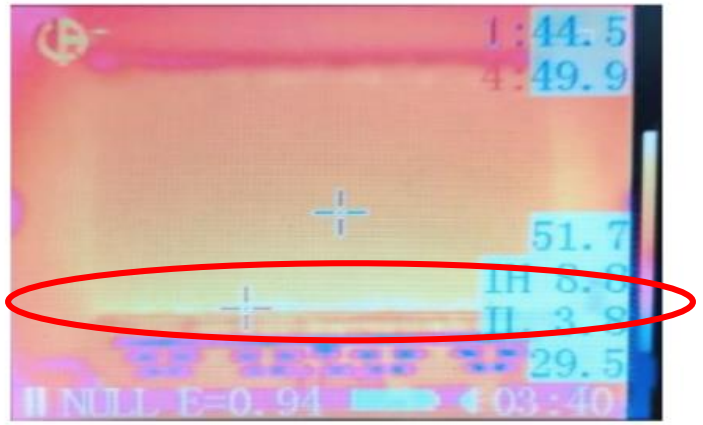
- Shunt-LDO is located in **very small area** on the chip bottom
- Excessive current and drop out voltage are “burned” there
  - ➢ **Up to 35% of power** in nominal operation!

=> Highly efficient CO2 cooling allows for this intrinsic inefficiency

- In case of one chip fails the power dissipated in the shunt parts can significantly increase

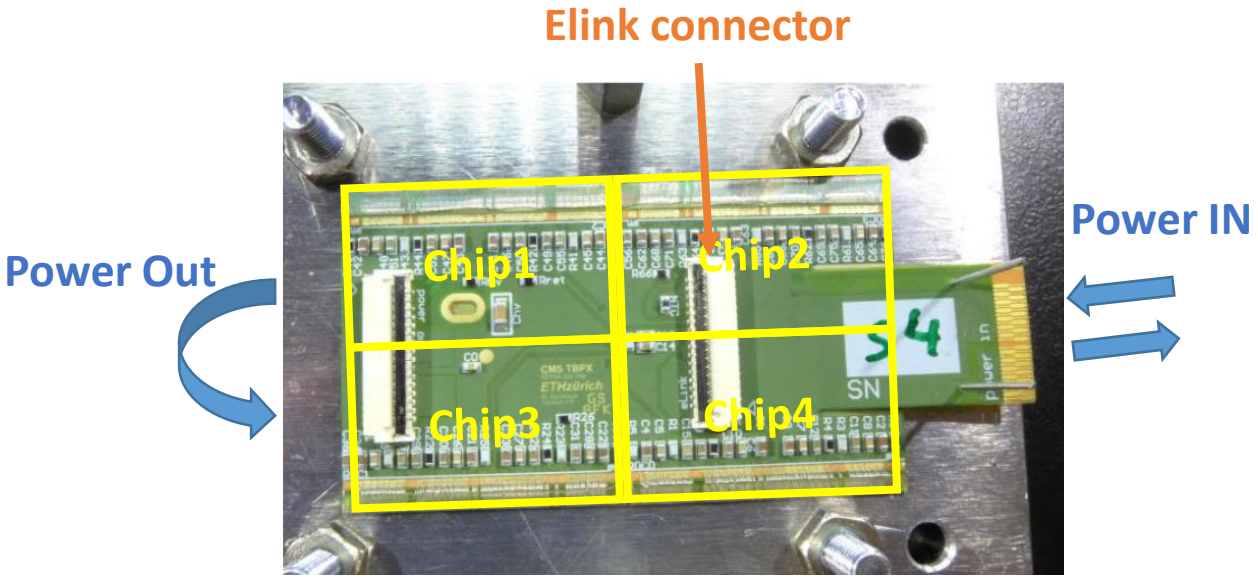


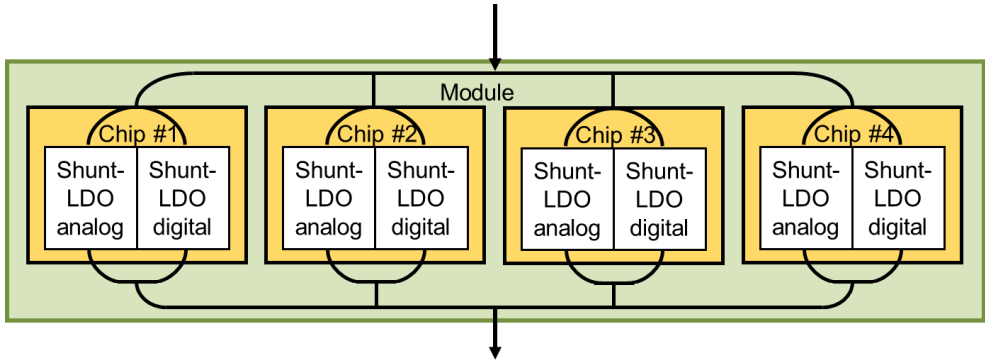




Recent system tests and developments

RD53A Quad modules



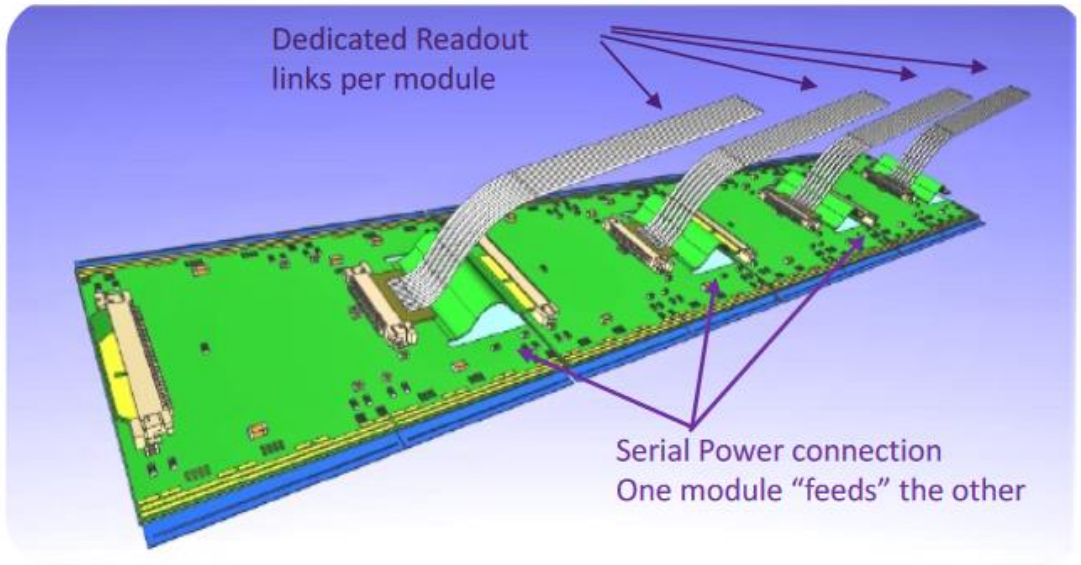


- First RD53A Quad modules were produced (without sensor so far)
  - Four chips are powered in Shunt-LDO mode in parallel
- Successful operations (powering and readout) of all four chips
  - Including operation of multiple modules in a serial chain

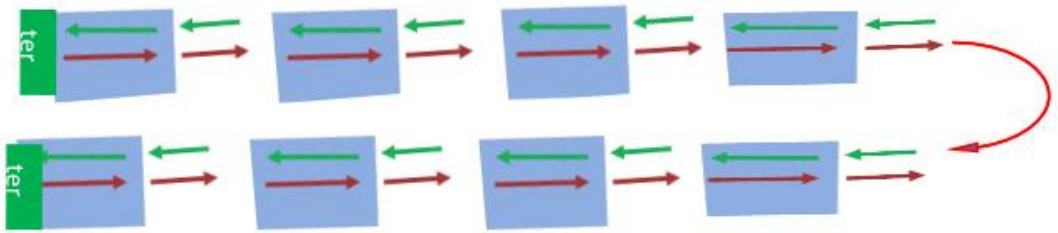
More in poster on “Prototype module construction for the high luminosity upgrade of the CMS pixel detector ” by Branislav Ristic

Two flavors of serial power chains in CMS

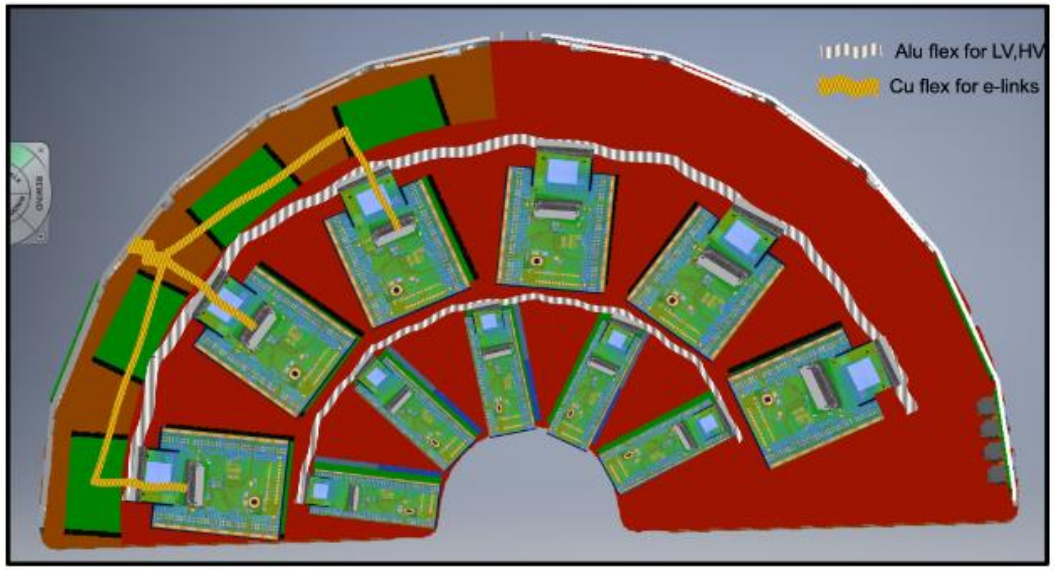
Ladder structure



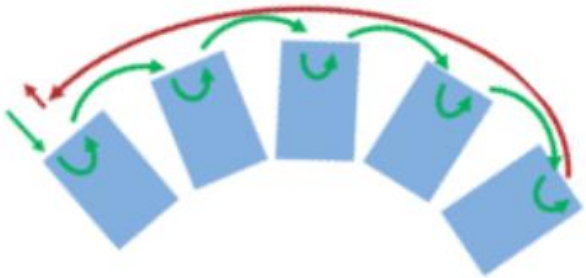
TBPX: 1 chain for 2 consecutive ladders in Phi



Disk structure



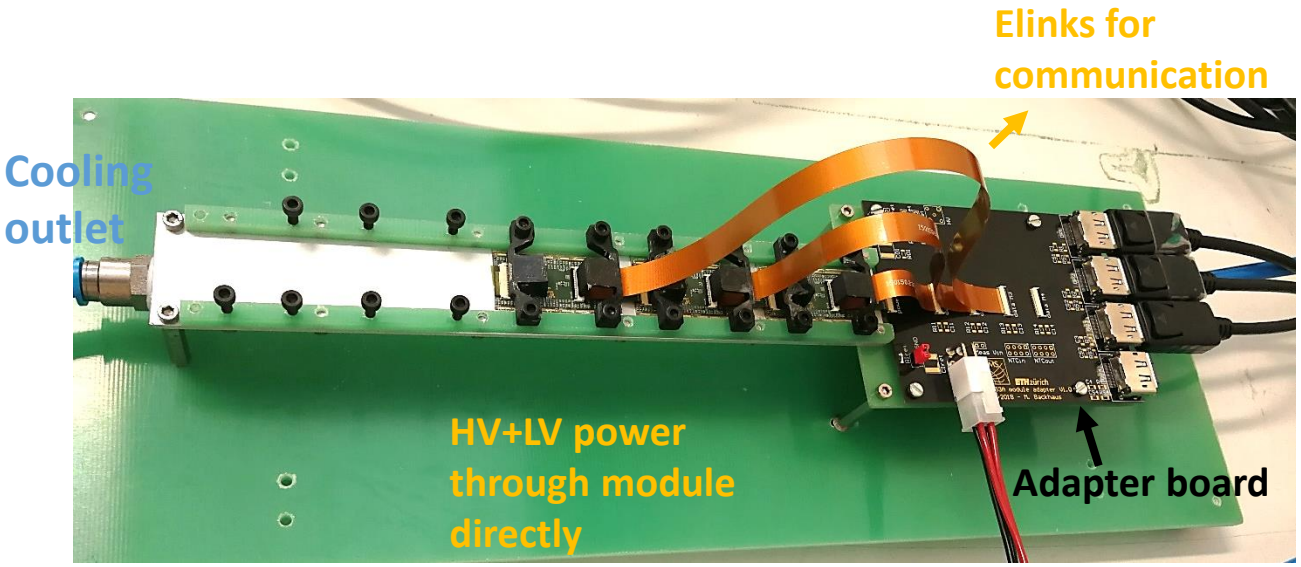
TFPX/TEPX: 1 chain per ring



Prototyping detector-like structures for electrical tests

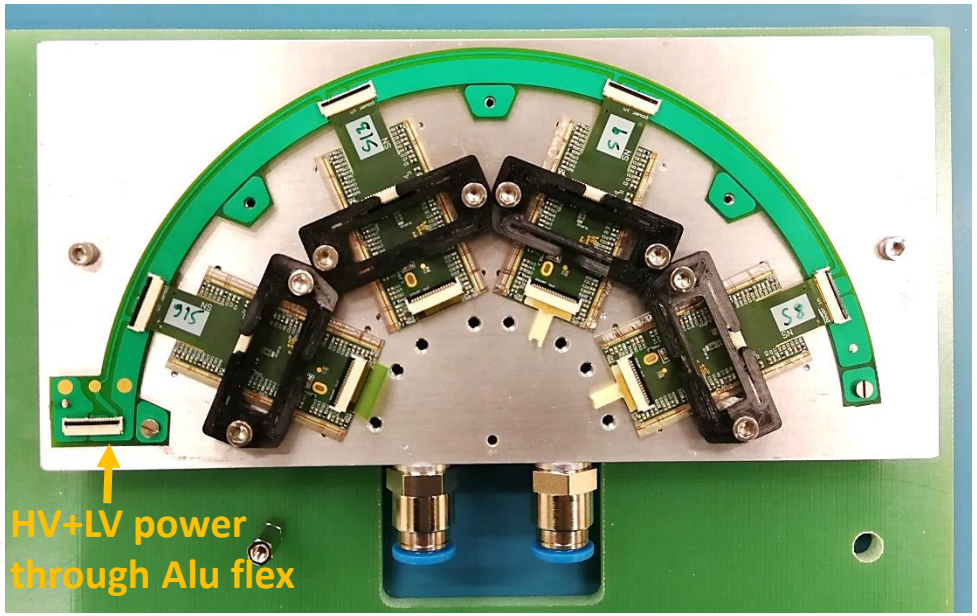
Ladder structure

Up to 5 modules in series



Disk structure

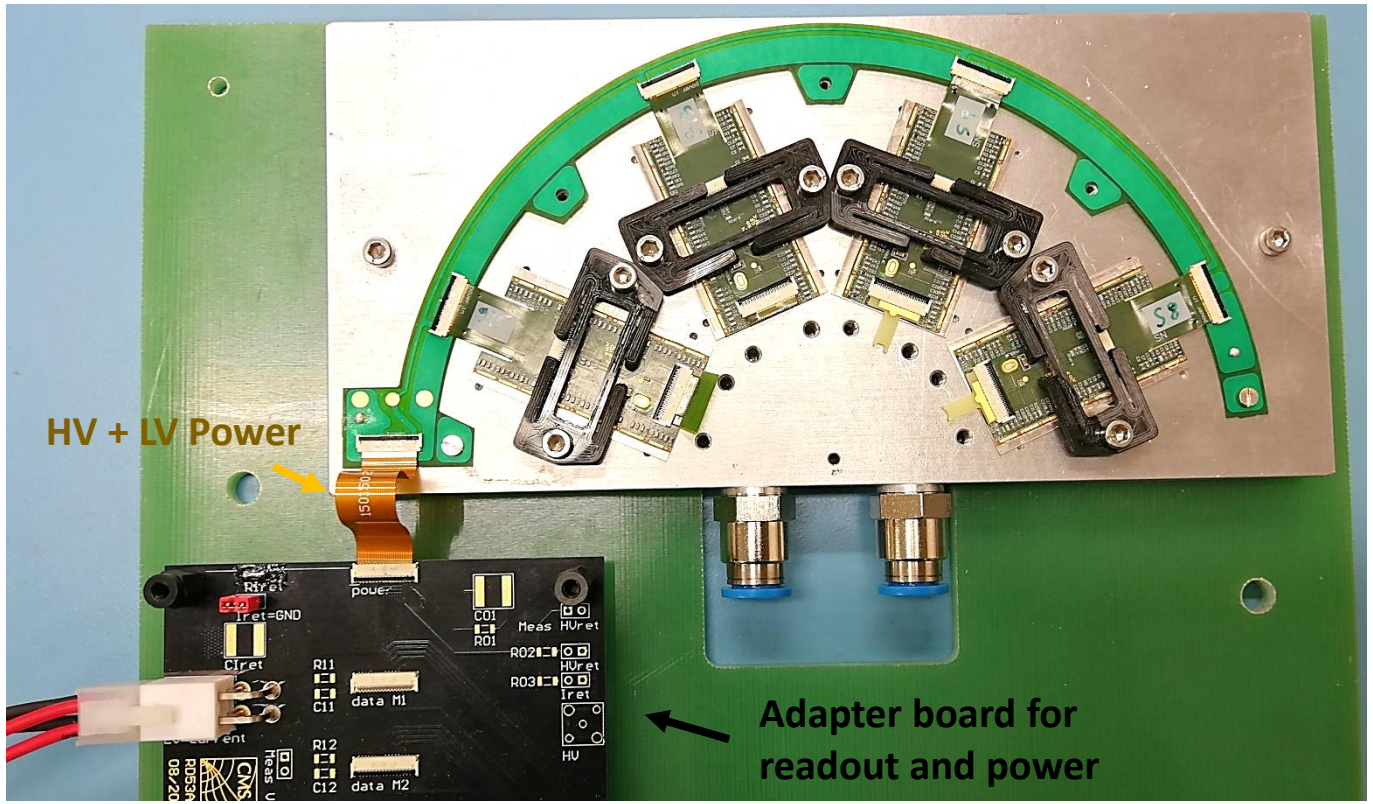
4 modules in series

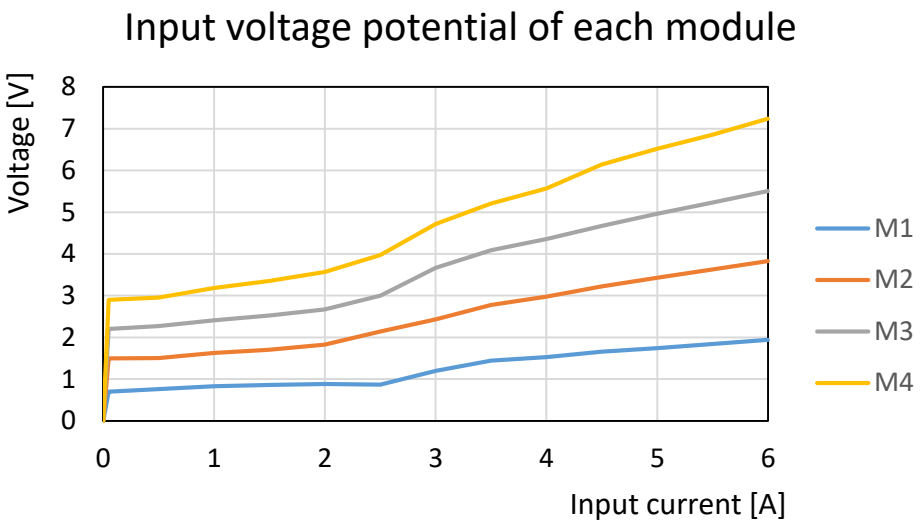


(Elinks and readout board not shown)

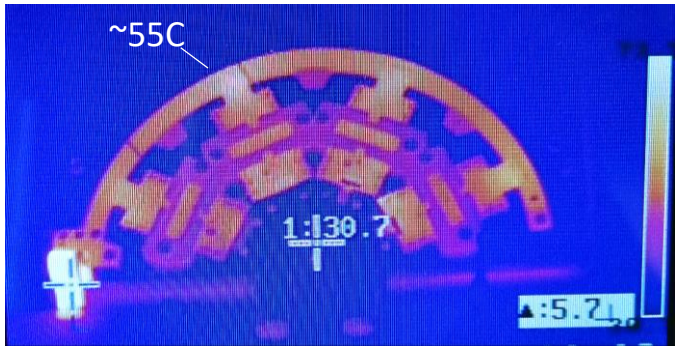
- Electrical connections similar to final detector
- Aluminum structure with water cooling pipe inside
  - ➢ Cooling is essential: ~10 W per module are dissipated

Measurements with Alu Power Flex for Disks





Picture with thermal camera



- Started electrical tests with disk structure
- Want to study RD53A power performance in detector like setup
- Demonstrate full chain operation (power + optical readout)

Conclusion

- Serial powering concept is **well established**

- Active R&D communities in ATLAS, CMS and RD53
  - Demonstrated **robust performance** in tests and simulations
  - Many **improvements** in Shunt-LDO regulator performance since RD53A

- System developments and tests are ongoing
  - Basic tests with **RD53A Quad modules** including chain operation were successful
  - Started tests with **detector like structures** for ladder and disk geometries

- Future challenges are still ahead
  - **Ensure efficient current sharing**
  - **Optimization** of serial powering parameters (working point, headroom)


Thank you

Backup

Possible sensor forward bias issue

Setting a work point for the Shunt-LDO

Shunt-LDO evaluation

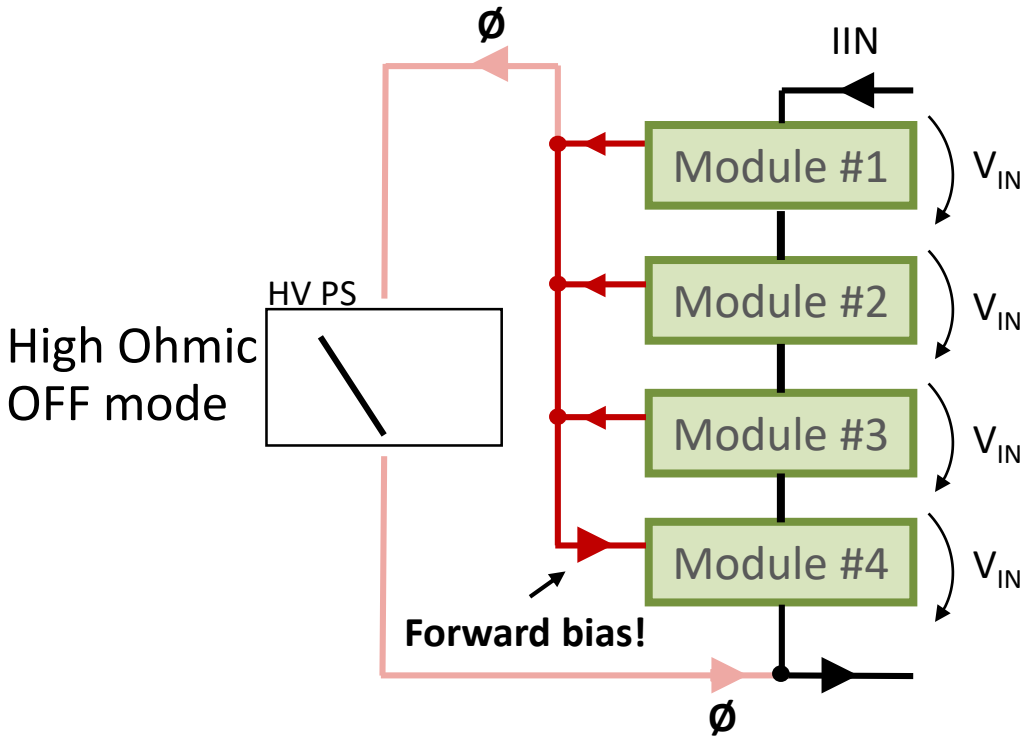
- Irradiation campaign
- Overvoltage protection
- Overload protection

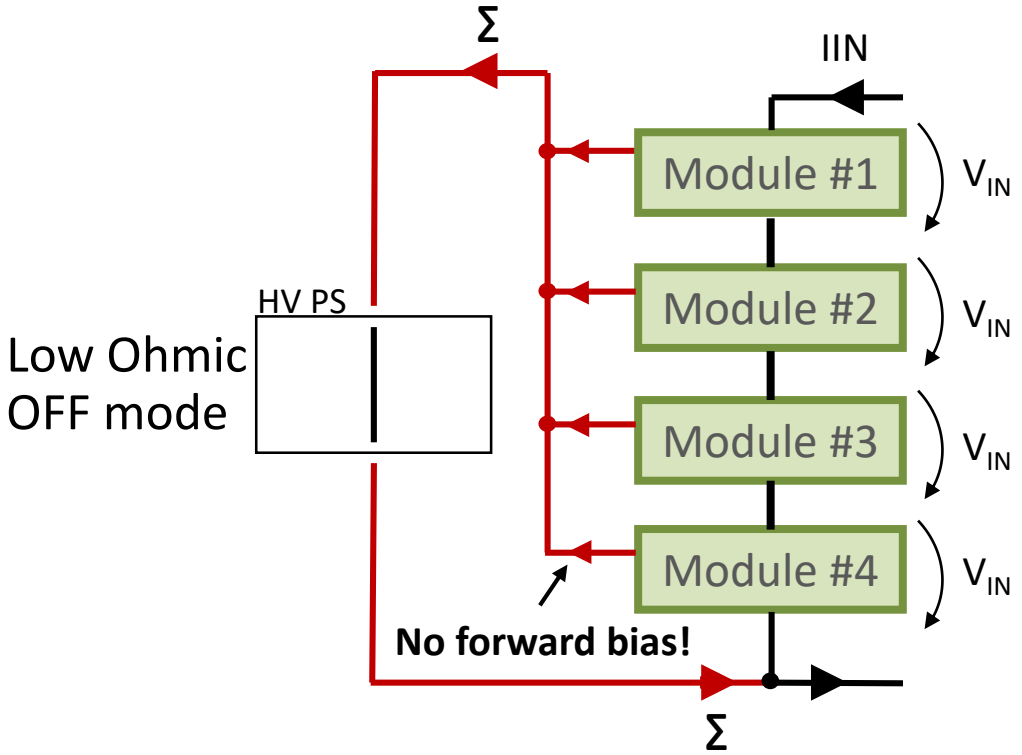
Serial Powering system tests with RD53A chips

Possible sensor forward bias when HV off and LV on

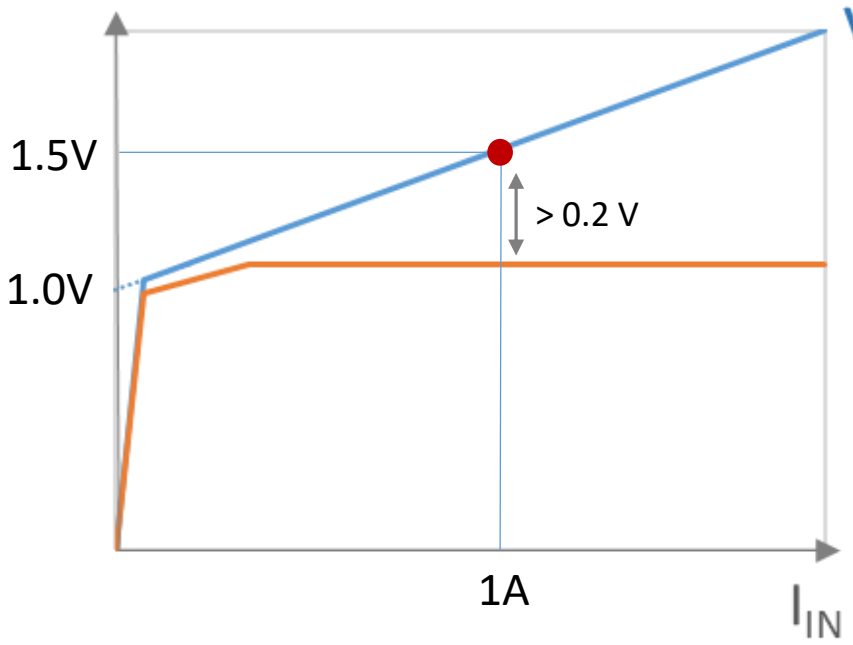
- Can generate **forward bias** of sensors when HV off and LV on
- Different local ground on each module => HV OFF is not 0V on sensor <u>when LV on</u>

  => Biased sensors and leakage current in off mode possible
- Power supply off mode (high/low ohmic) important for leakage current path





Setting a working point for the Shunt-LDO



V_{out} = 1.2 V = 2 ∗ 0.6 V

Relationships

$$Vin = Vofs + \frac{R3}{1000} * Iin$$

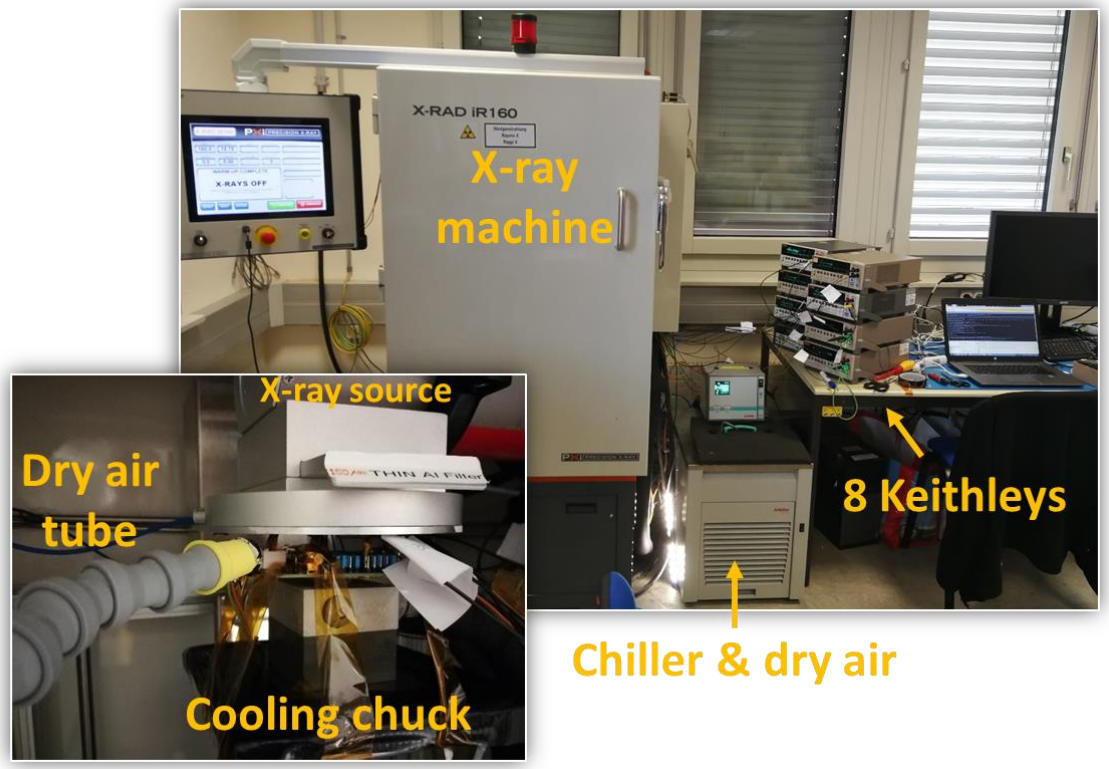
$$Vout = 2 * Vref$$

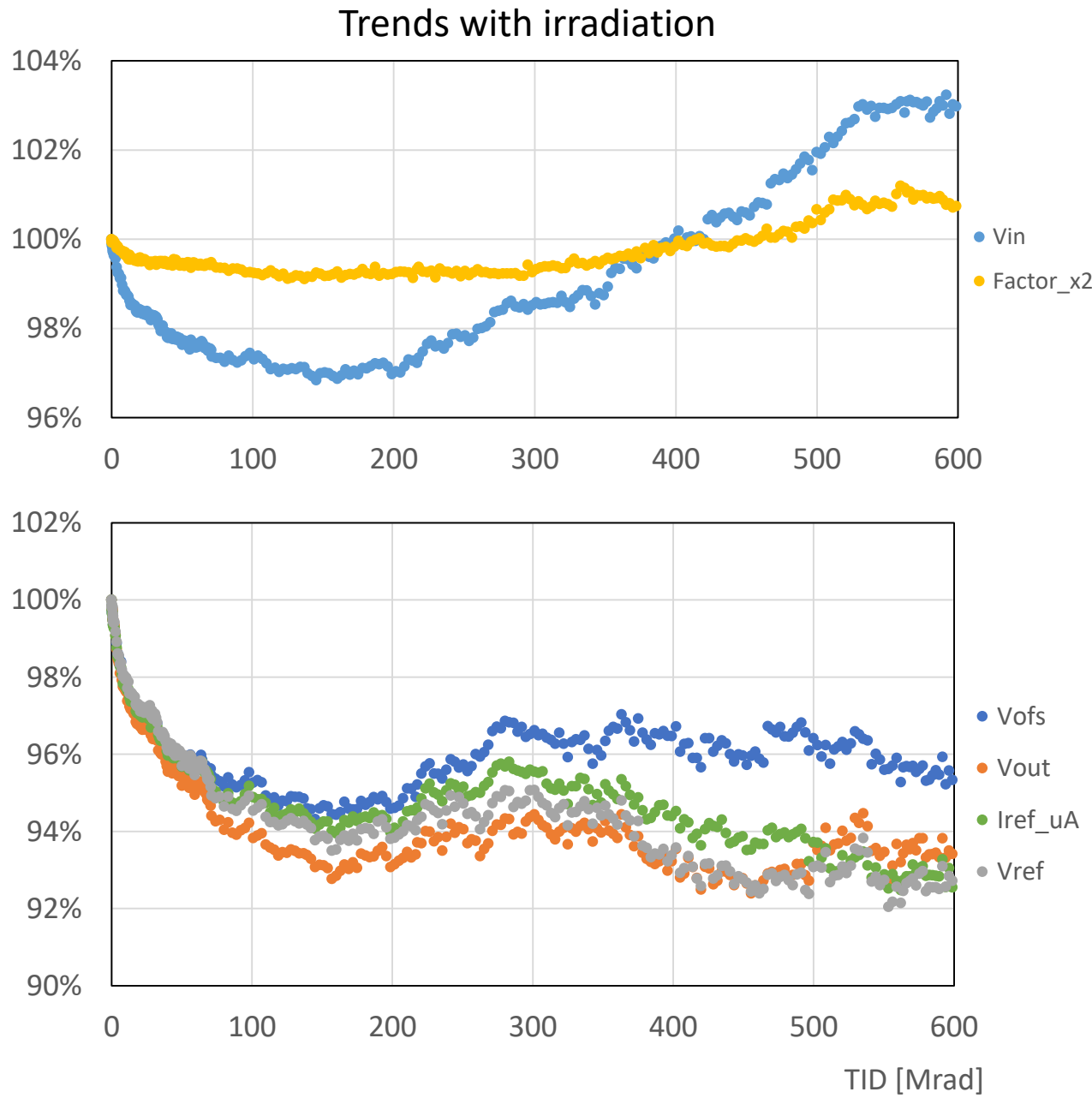
- Choose Vofs and Slope (with resistors) => For input behavior → **Fixed after installation**
- Trim Vref (with trimbits) => For output behavior → **Adjustable during operation**

- Provide constant input current
  - Shunt-LDO regulates input voltage accordingly
  - Has to be higher than maximum expected load
  - Limited by **1.4V < V_{IN} < 2.0V** and **$I_{IN,SLDO}$ < 2.0A**

Shunt-LDO evaluation

Irradiation campaign with Shunt-LDO testchips





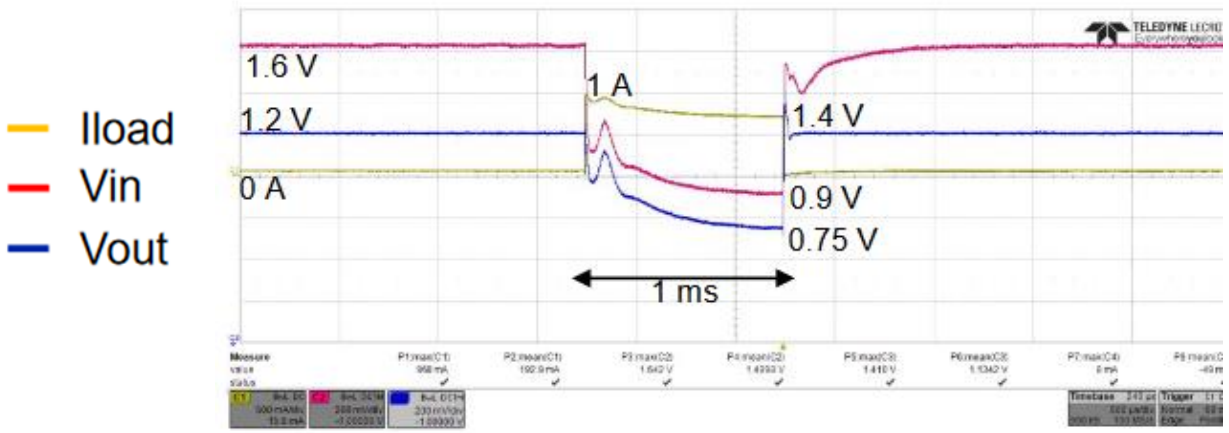
Shunt-LDO is fully functional after 600Mrad at 0C:

- Output behavior is very stable
- Some variations of input behavior
- Reference voltages change due to internal resistor
  => New design with radiation harder resistor

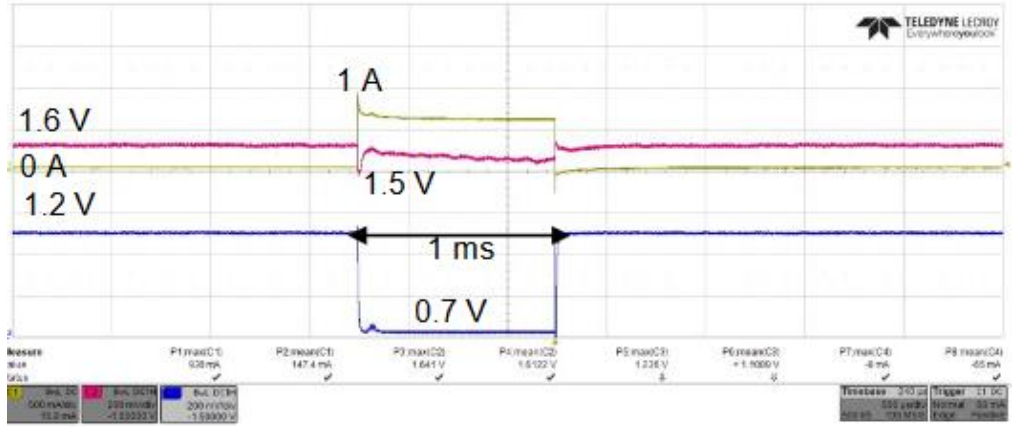
Additional feature: Overload protection

- Decreases output voltage if load current gets too high
  => Reduces transients propagated to other chips in the chain

Protection off



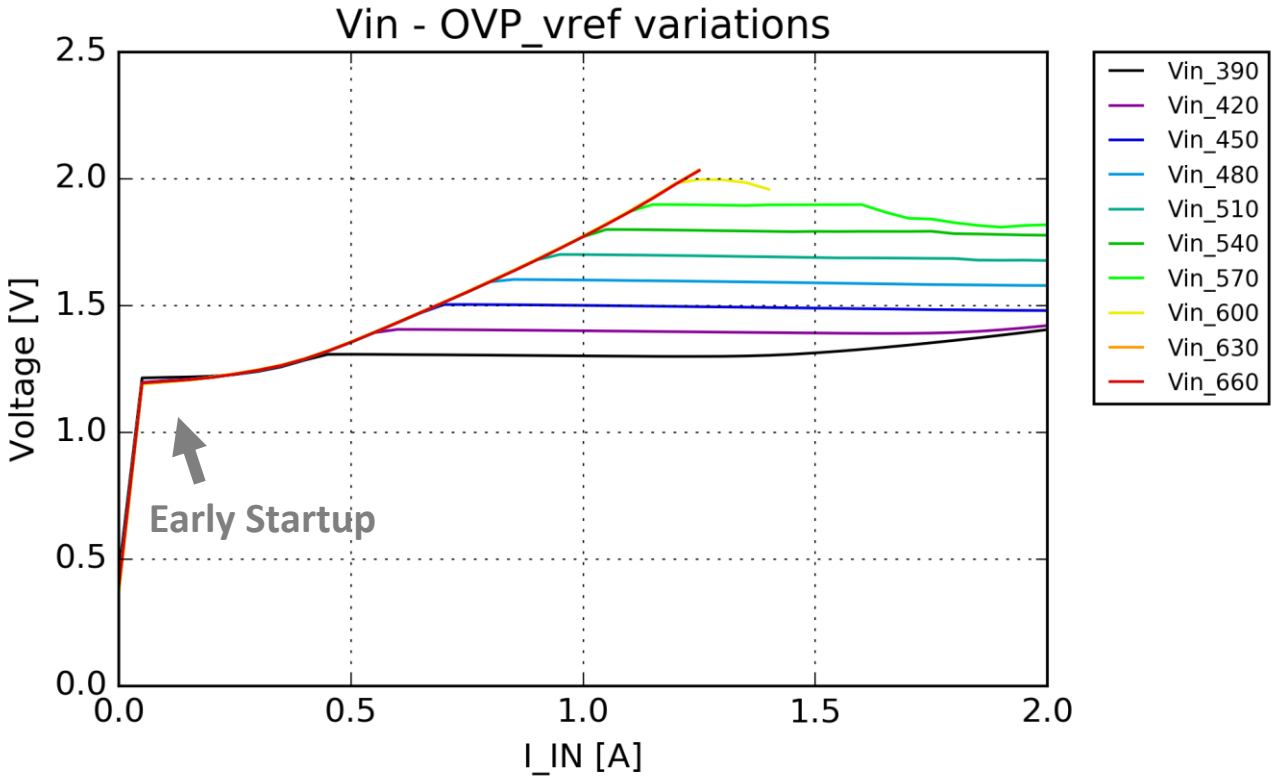
Protection on



- Creating 1 ms overload pulse and comparing with and without protection
  => Without protection huge transient on **input voltage**
  => **With protection reduced transient** on **input voltage**

Additional feature: Overvoltage protection

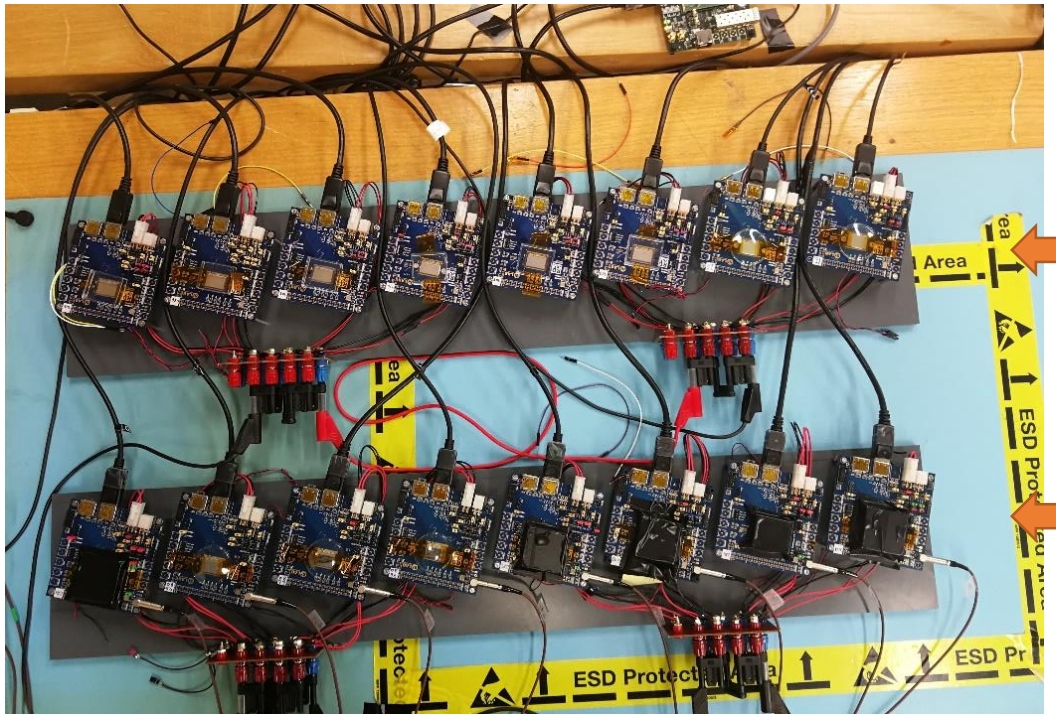
➢ Acts like a voltage clamp => **Limits maximum voltage**



- Tested with different configured maximum voltages
- **Startup significantly improved** compared to RD53A

Serial powering system tests with RD53A chips

Serial powering system tests with RD53A chips



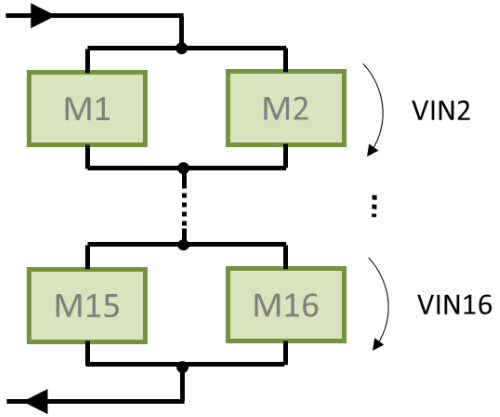
8 RD53A chips without sensor

8 RD53A chips **with sensor**

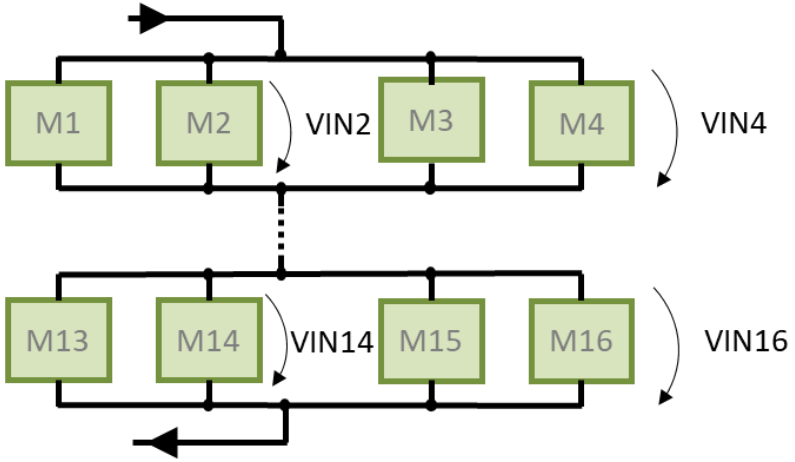
- First serial powering tests based on single RD53A chip cards connected externally
- Emulated serial power chains of double and quad modules with 16 RD53A chips

Emulating Quad and Double modules

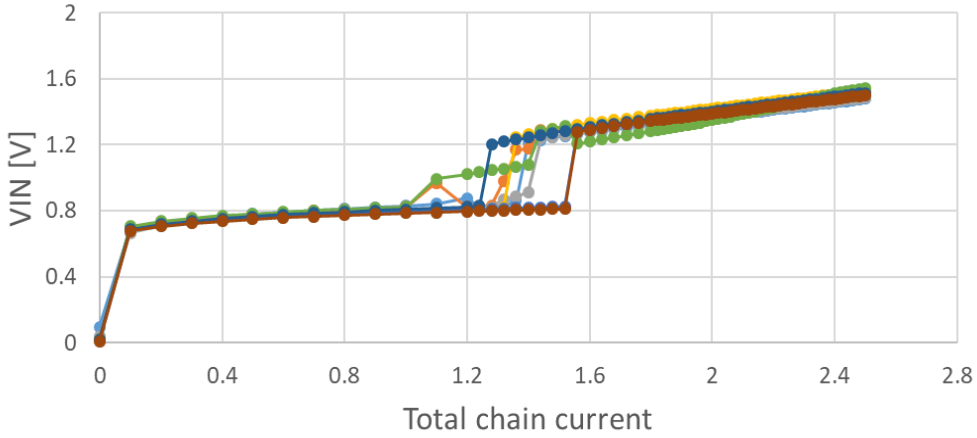
a) 8x “Double-chip modules”

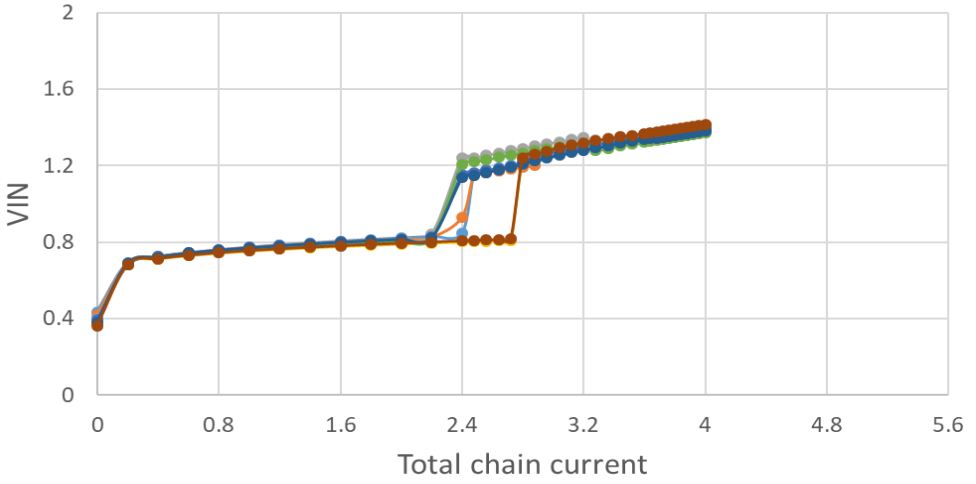


b) 4x “Quad-chip modules”



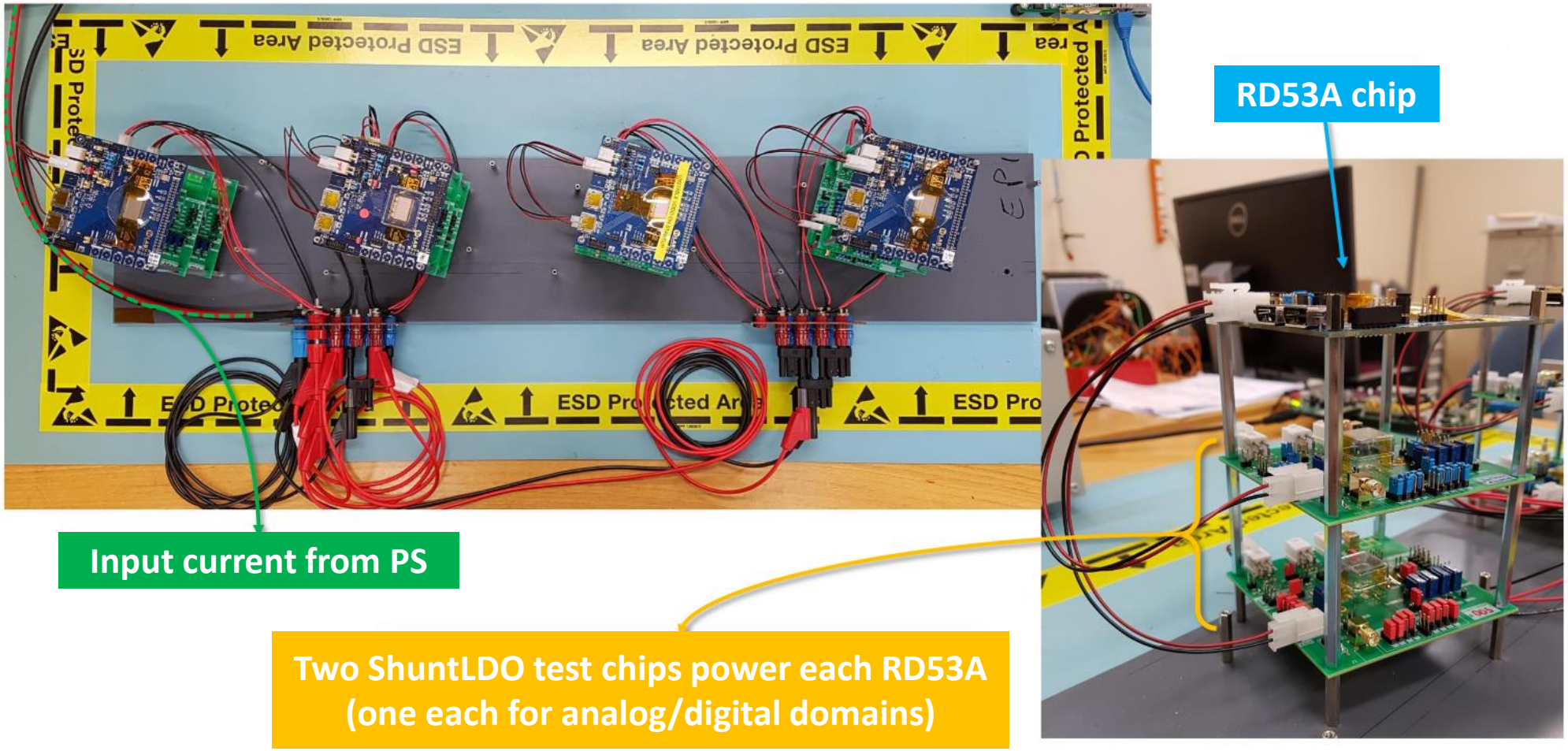
VI curves for each module group





=> Successfully operated serial chains with up to 16 RD53A chips on Single Chip Cards

Powering RD53A chips with new Shunt-LDO test chips



- Started to test new Shunt-LDO test chips with RD53A chip
  (By bypassing the RD53A Shunt-LDOs)
  - ➢ Want to evaluate new Shunt-LDO performance with RD53A chip