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Depleted Monolithic Active Pixel Sensors in the LFoundry 150 nm and TowerJazz 180 nm CMOS technologies

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The key ingredient to enhance the radiation tolerance and timing precision for CMOS pixel sensors is to achieve a fully depleted sensitive layer, where the charge collection is guided by strong drifting field. Such sensor concepts have been progressively demonstrated by recent R&D achievements with monolithic prototypes in large formats. These sensors are often referred to as DMAPS (Depleted Monolithic Active Pixel Sensor), and this talk will summarize the DMAPS development in LFoundry 150 nm and TowerJazz 150 nm CMOS processes.

The development of DMAPS in LFoundry 150 nm CMOS technology makes use of a so-called large electrode design to achieve a depleted sensitive layer by combining high resistive substrate ($> 2 \text{ k}\Omega\text{-cm}$) as sensitive layer and high bias voltage ($> 200 \text{ V}$). The implemented sensor structure mimics the standard planar sensor, and it incorporates a large-area implant as the collection node, thus is an intrinsically radiation-hard structure with uniform drifting field. The in-pixel electronics is integrated in the collection well thanks to the multiple nested wells offered by the foundry. The TowerJazz development line uses a small collection diode, and the resulting sensor capacitance can be as small as $\sim 5 \text{ fF}$, a value typically an order of magnitude smaller than that in the large electrode design case. A major benefit of small sensor capacitance is the possibility to employ an ultra-low power analog front-end design ($\sim 1 \mu\text{W}/\text{pixel}$), maintaining at the same time good noise, threshold and timing performances. In order to achieve a fully depleted sensitive layer, together with enhanced lateral collection field, dedicated process modifications are needed in such small electrode designs.

This talk will mostly focus on the two large scale demonstrator chips fabricated in the aforementioned two technologies, named LF-Monopix and TJ-Monopix. They both have the same column based, synchronous readout architecture, which is similar to the one implemented in the current ATLAS pixel detector (FE-I3). The design and characterization results, both in lab and in beam, will be presented. Issues for the current designs and fixes planned for the future will be discussed. Submission plans for the next-generation chips, i.e. LF-Monopix2 and TJ-Monopix2, will also be given.

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