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DAQ and Level-1 Track Finding for the CMS HL-LHC Upgrade

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The LHC will be upgraded to the High Luminosity (HL-LHC) in the late 2020 in order to reach an instantaneous luminosity as high as $7 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, hence increasing the discovery potential of the machine. In order to preserve its physics reach, the CMS detector will be significantly upgraded. A key component of the upgrade is the Outer Tracker detector that will be able to identify tracks with transverse momentum above $\sim 2 \text{ GeV}/c$ and provide them to the Level-1 trigger algorithm, thus maintaining manageable trigger rates and good performance. One of the main challenges of the Level-1 track finding is being able to reconstruct charged particles trajectories from a 40 MHz collision rate with a few microsecond latency budget. Dedicated FPGA hardware systems have been developed for track finding to address this challenge. Another stringent requirement on the Tracker DAQ system is set by the unprecedented number of channels, reaching 2 billions for the Inner Tracker only. To handle this, the Tracker DAQ back-end boards will be equipped with commercial CPUs that will guarantee the system scalability and ensure an effective monitoring of the detector conditions. The DAQ proposal to handle this distributed computational power as well as the design choices of the Level 1 track finding will be presented.

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