CMS Phase-1 Pixel Detector :

Operational Experience, Performance and Lessons Learned

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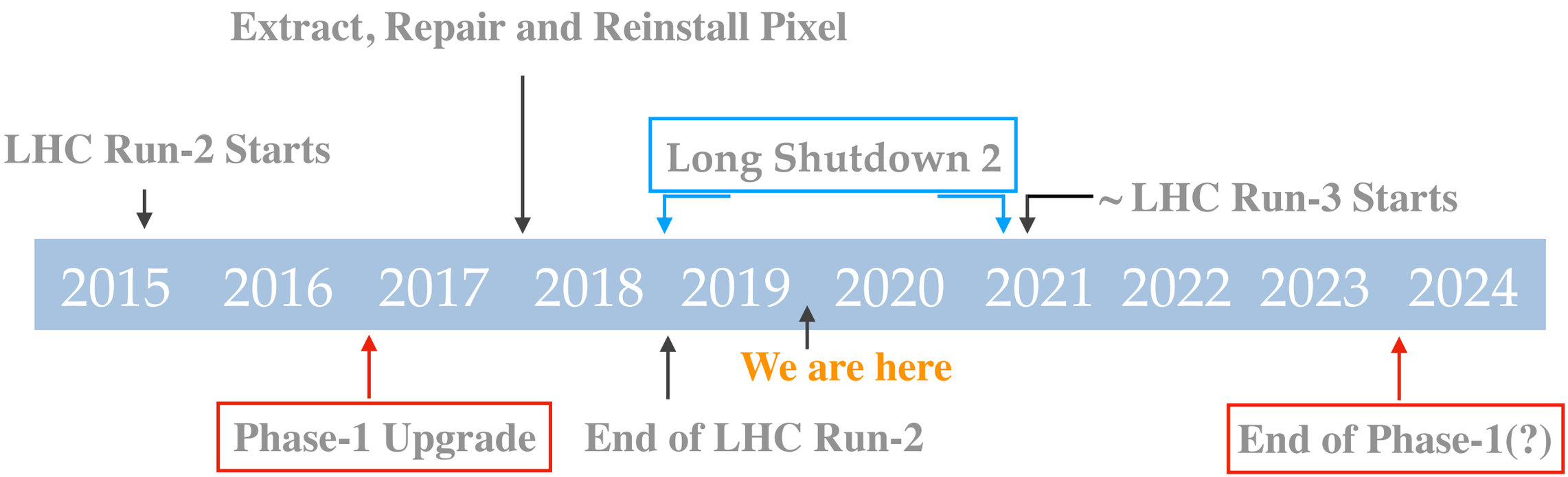
On Behalf of the CMS Collaboration

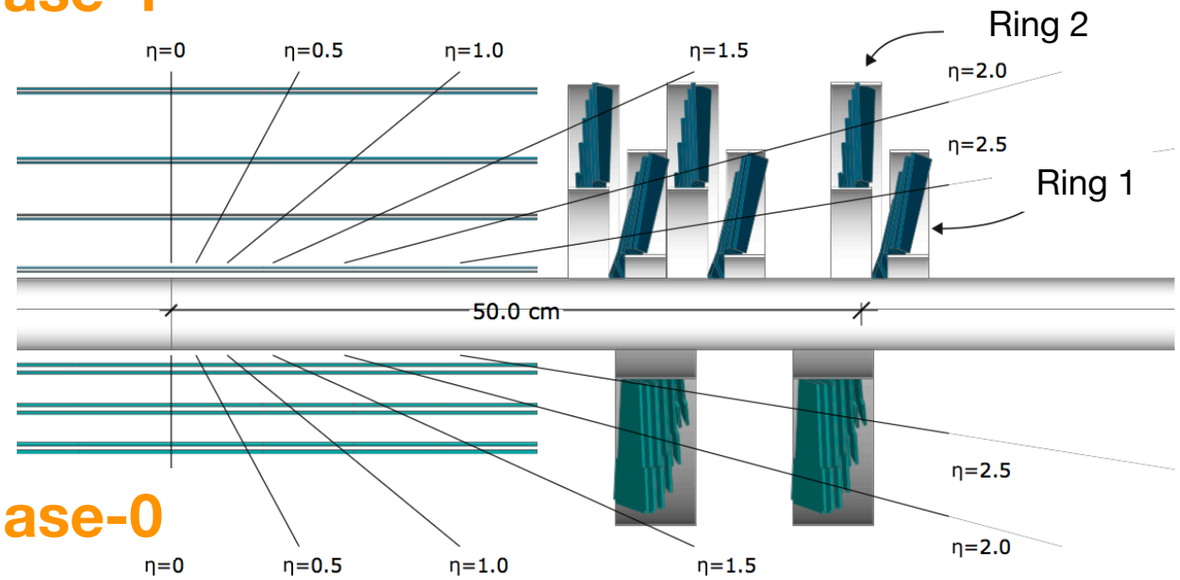
The 28-th International Workshop on Vertex Detectors

Timeline:


Extract, Repair and Reinstall Pixel
LHC Run-2 Starts
Long Shutdown 2
~ LHC Run-3 Starts
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
We are here
Phase-1 Upgrade
End of LHC Run-2
End of Phase-1(?)

Phase-1 Upgrade:

Phase-1



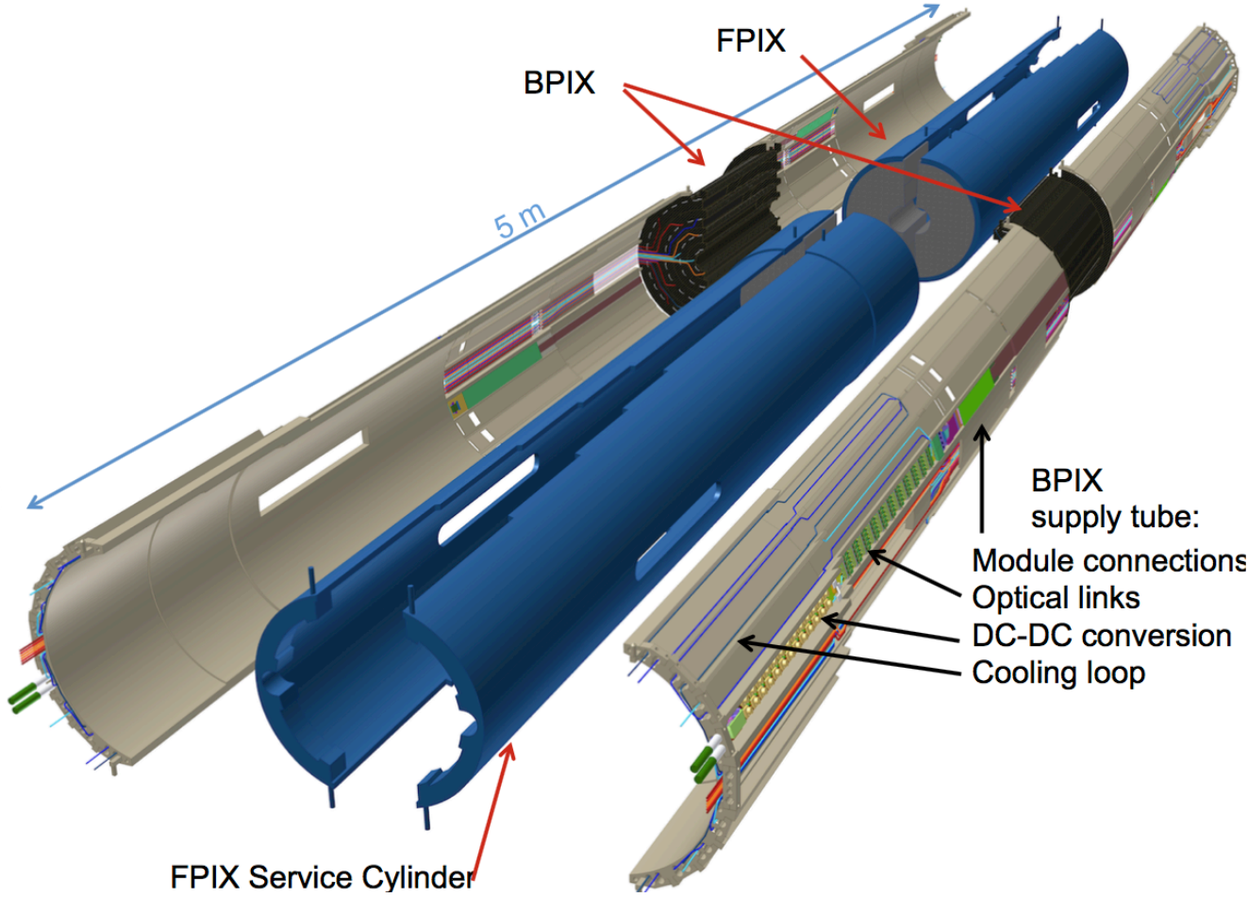
Phase-0

Motivation for upgrade:

- Phase-0 was designed for an instantaneous luminosity of $1x10^{34}$ $cm^{-2}s^{-1}$
- LHC performing beyond expectation, projected instantaneous luminosity for Run-2 $2x10^{34}$ $cm^{-2}s^{-1}$
- Large hit inefficiency due to high data rate

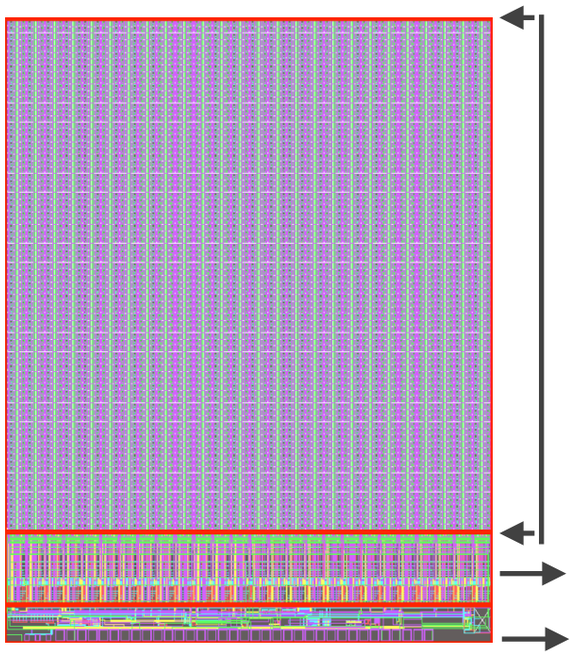
Upgrade features:

- One additional barrel layer and endcap disk
- Layer-1 closer to IP
- Improved Readout Chips
- 1.9 times more readout channels
- Forced to keep same power cables, use DCDC conversion near detector
- Two-phase CO_2 cooling
- uTCA based backend hardware



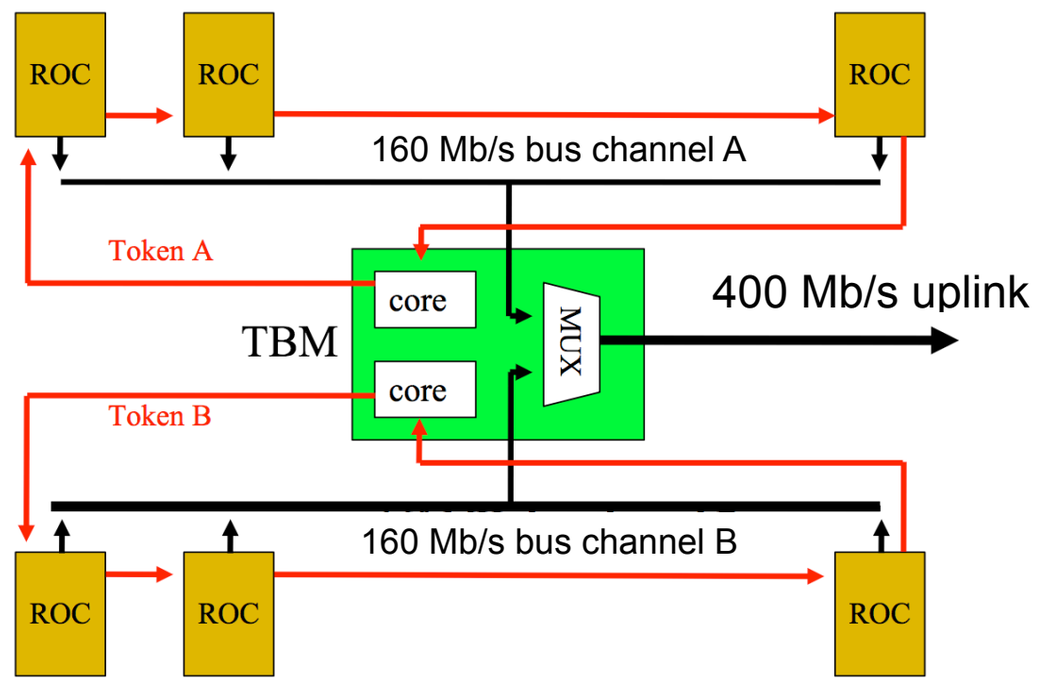
Phase-1 Detector: Front-end

Layout of the read out chip (ROC)



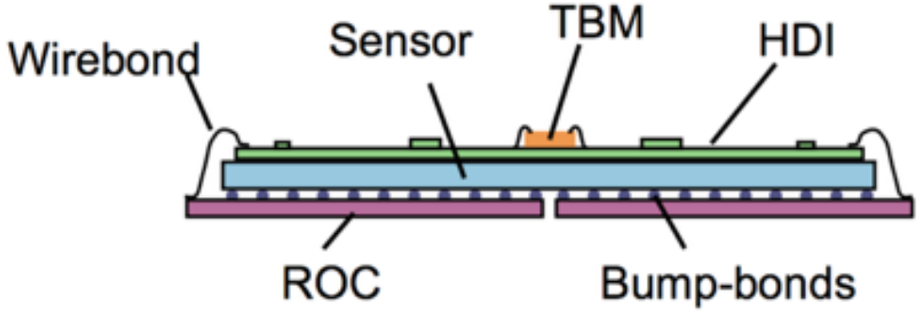
- 8 bit ADC for pulse height
- Increased buffer size for timestamp (24) and data (80)
- On chip digitization, readout at 160 Mbps
- Mainly two flavors of ROC:
  - PROC600 for Layer-1 and psi46dig for rest
  - Data rate: PROC600 - 580 MHz/cm^2, psi46dig - 150 MHz/cm^2
  - Data Drain: PROC600 - dynamic cluster draining, psi46dig - double column drain

Token Bit Manager (TBM) block diagram

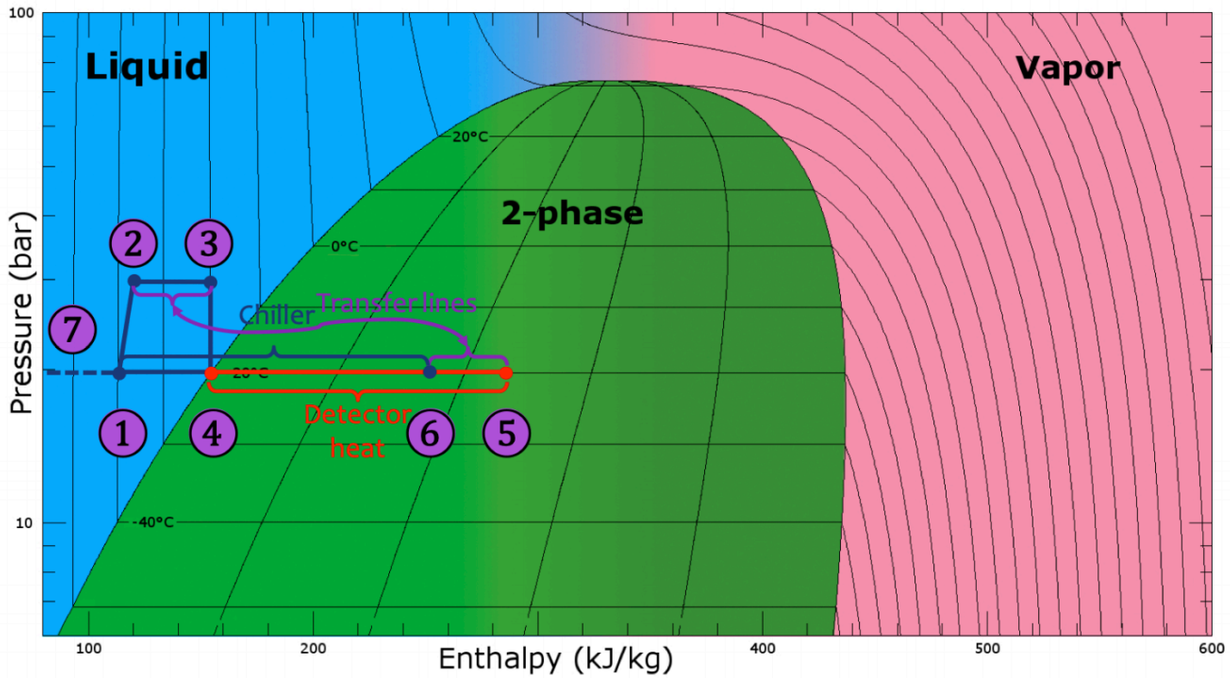


- There is one circuit in TBM that gets latched by SEU and needs power cycling to restore functionality
- Typical SEU rate during 2018: **~ 3/100 pb^{-1}**

Schematic of a typical module

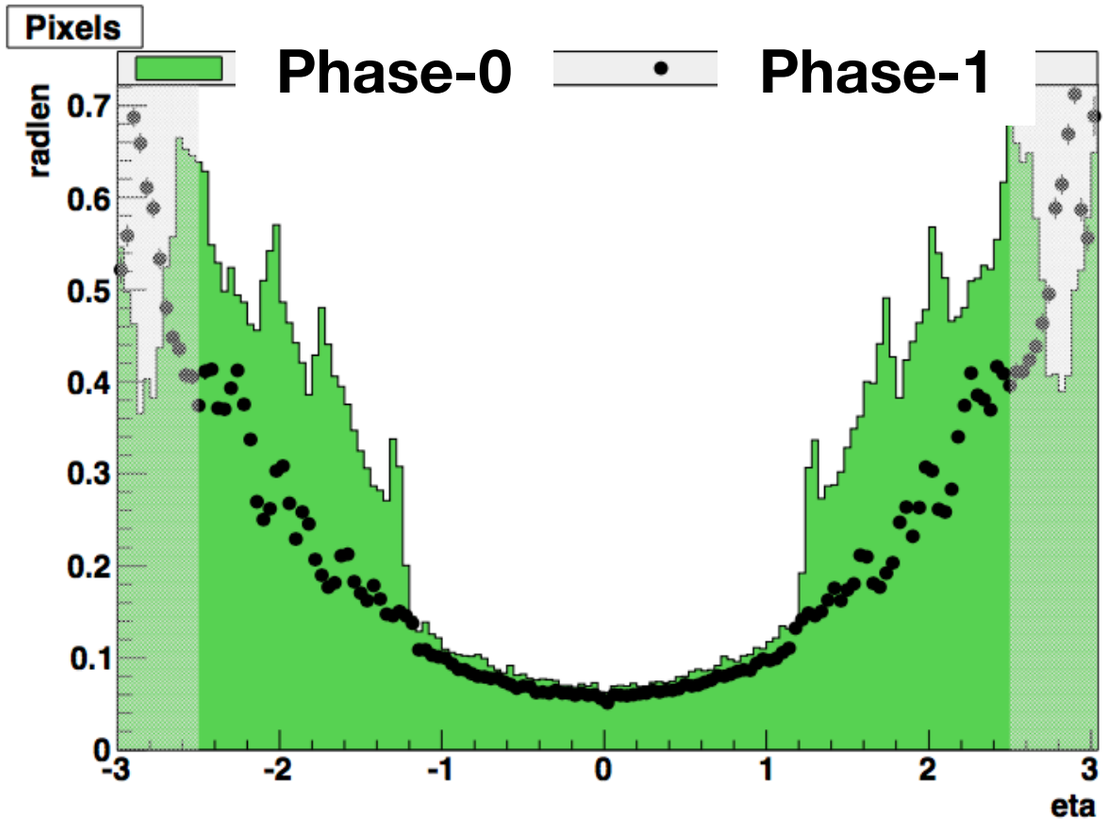


Cooling and Material Budget:

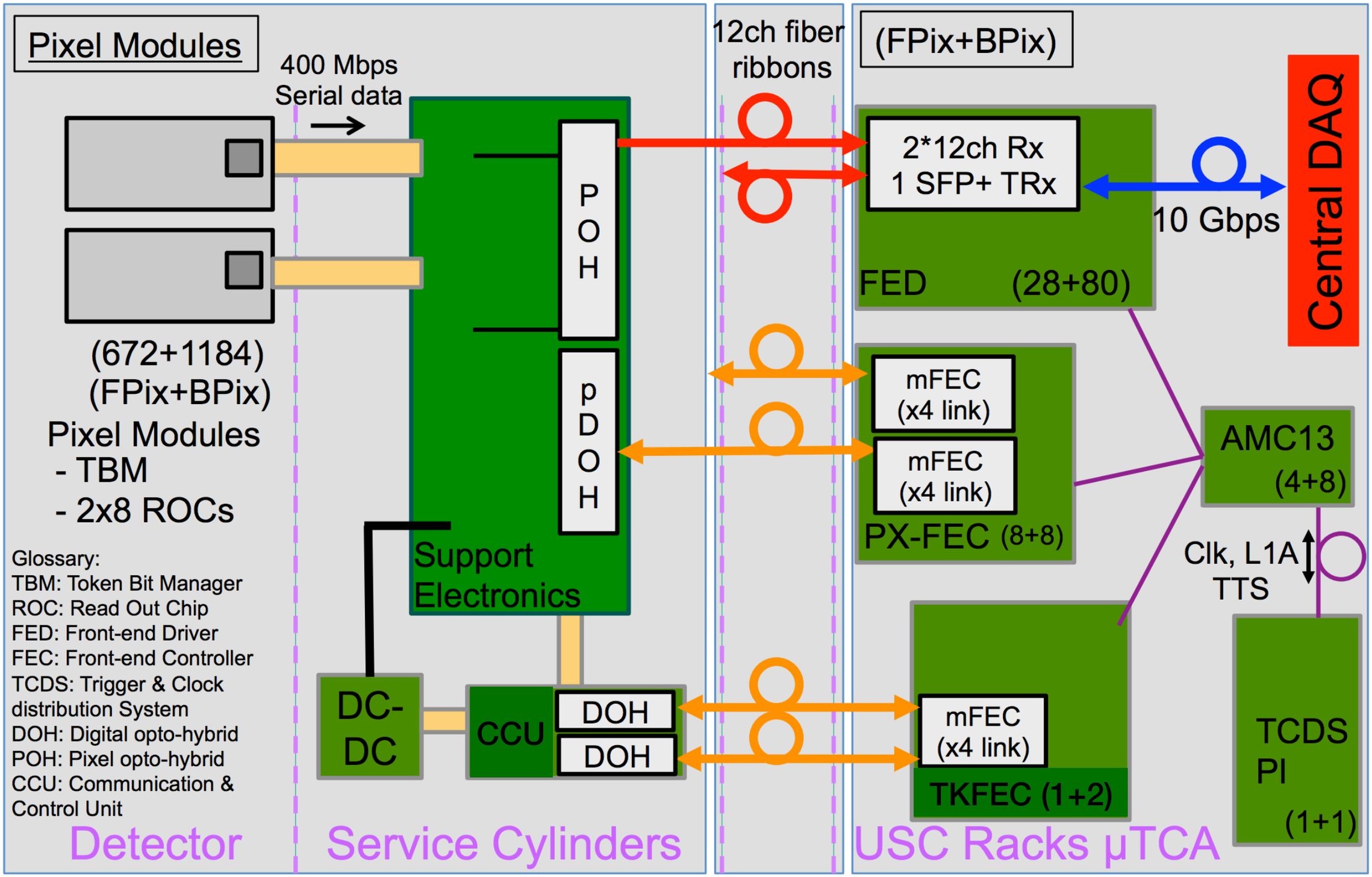


- Two-phase CO_2 cooling instead of mono phase C_6F_{14}
- Set temperature -22°C, possible to go even lower
- Light weight, thinner, stainless steel cooling pipes

- Cooling choice reduced the material budget
- Carbon fiber made support structure
- Auxiliary components moved to higher pseudo-rapidity
- First use of two-phase CO_2 cooling in CMS; Several phase-2 projects will use CO_2 cooling



Phase-1 Detector: DAQ Architecture



Status after 2017:

Mar 2017 → Phase-1 upgrade done, Started data taking with 95.6% active detector

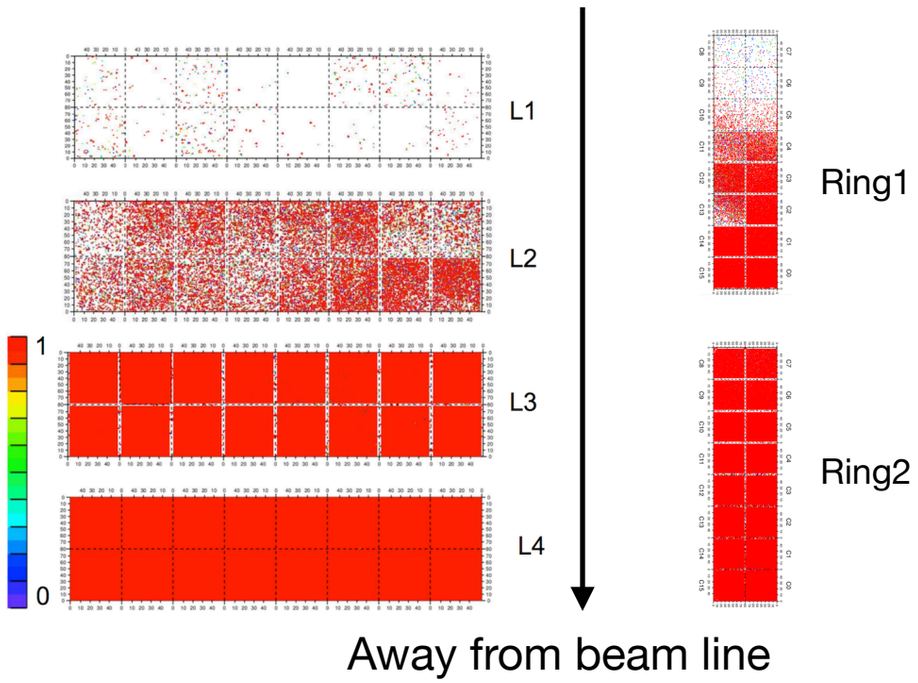
5th Oct 2017 → 1st DCDC Converter Broke

Dec 2017 → 5% converters not working, 11% detector not active

YETS 2017-18 → Detector Extracted, Replaced all DCDC with bigger fuse, problem not yet understood

May 2018 → Problem reproduced at lab (irad, xray), reason known

- DCDC failure during enable/disable cycle of SEU recovery
- Reason of failure was not understood until mid 2018
- Modules with broken DCDC not properly powered
- Bias voltage on, module power off condition damaged modules
- Damage proportional to accumulated radiation and distance from beam line
- 6 (accessible) Layer1 modules replaced during 2017-18 YETS out of total 8 damaged modules in Layer-1



Beginning of 2018: 97.3% Active detector

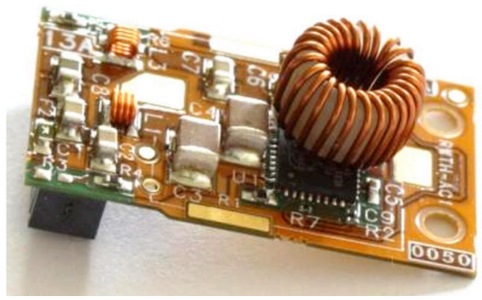
	Tot ROC	Inactive	%Active
L1	1536	56	96.4
L2	3584	224	93.7
L3	5632	88	98.4
L4	8192	48	99.4
Ring1	4224	290	93.1
Ring2	6528	88	98.7

DCDC Converter Failure: Impact on operation in 2018

- Using DCDC converters was an elegant solution for Phase-1 detector powering
- Due to a fault in FEAST chip design it started breaking while in disable state due to charge build up in a circuit when irradiated (> 10kGy)
- Adapted power cycling procedure during 2018 operation to avoid breaking the converters.
- Latest FEAST (2019) chip fixes the problem and will be used in Phase-1 detector replacing the old ones

Impact on operation in 2018:

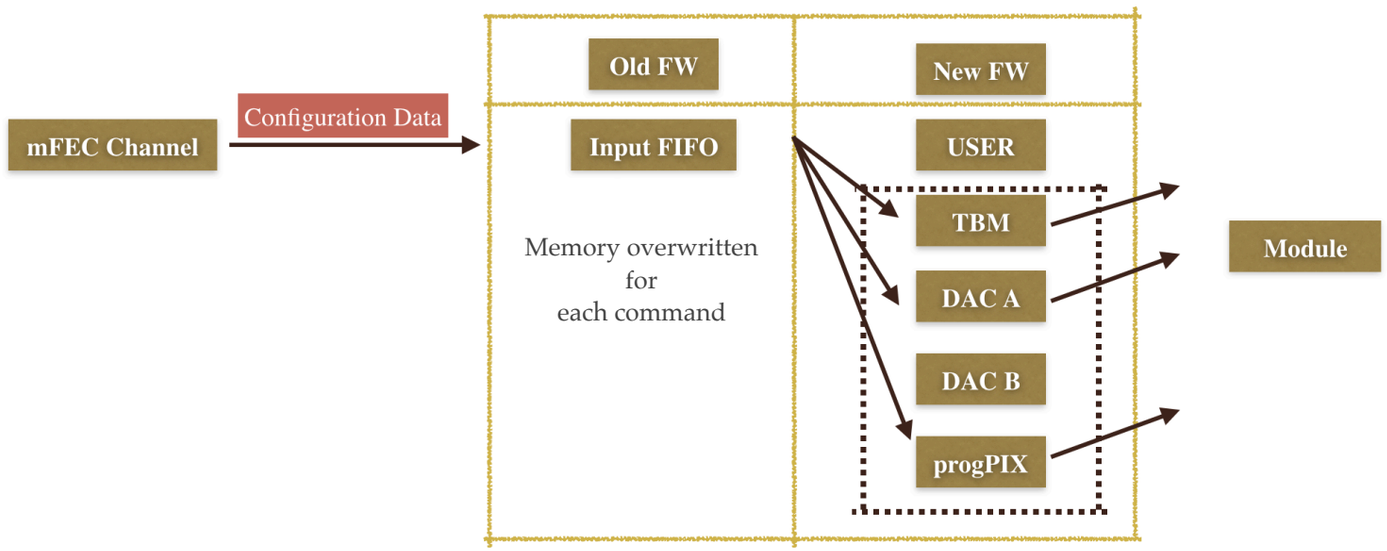
- No power cycle during run, accumulate stuck-TBM and power cycle after the end of the fill
- Kept converters always in enabled state, used CAEN system for power cycling. Operated converters with lower input voltage
- Immediate consequence was high current trips in power groups with higher share of modules
- Raised trip limit, smart programming to reduce start up current in power groups, or in worst case selectively disabled converter to avoid trips



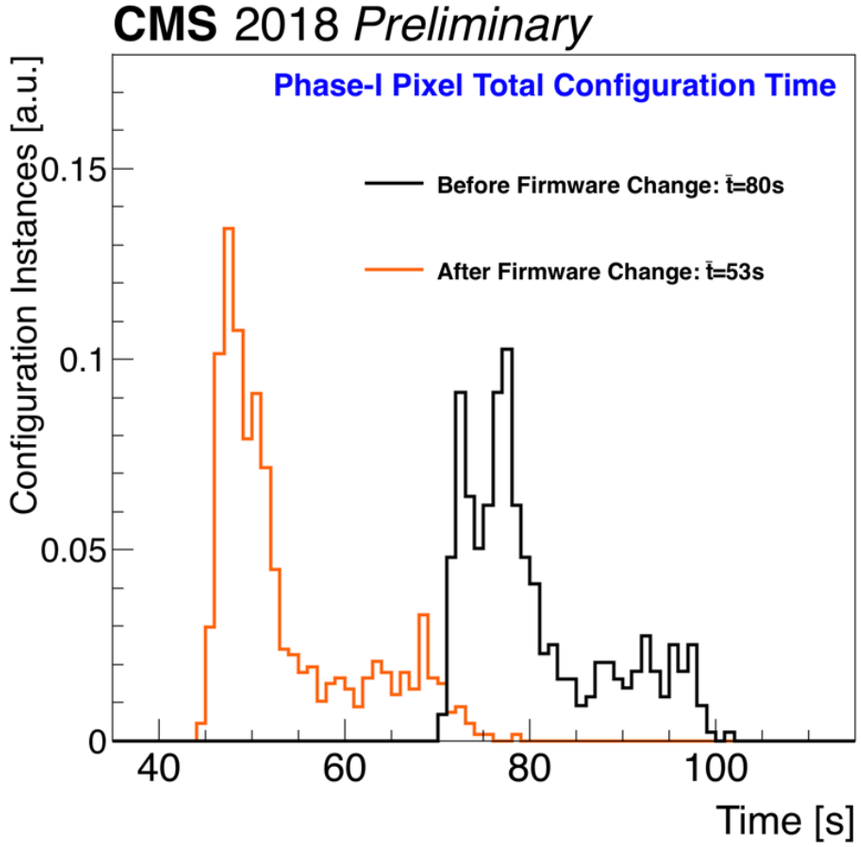
A DCDC converter without the shield on inductor

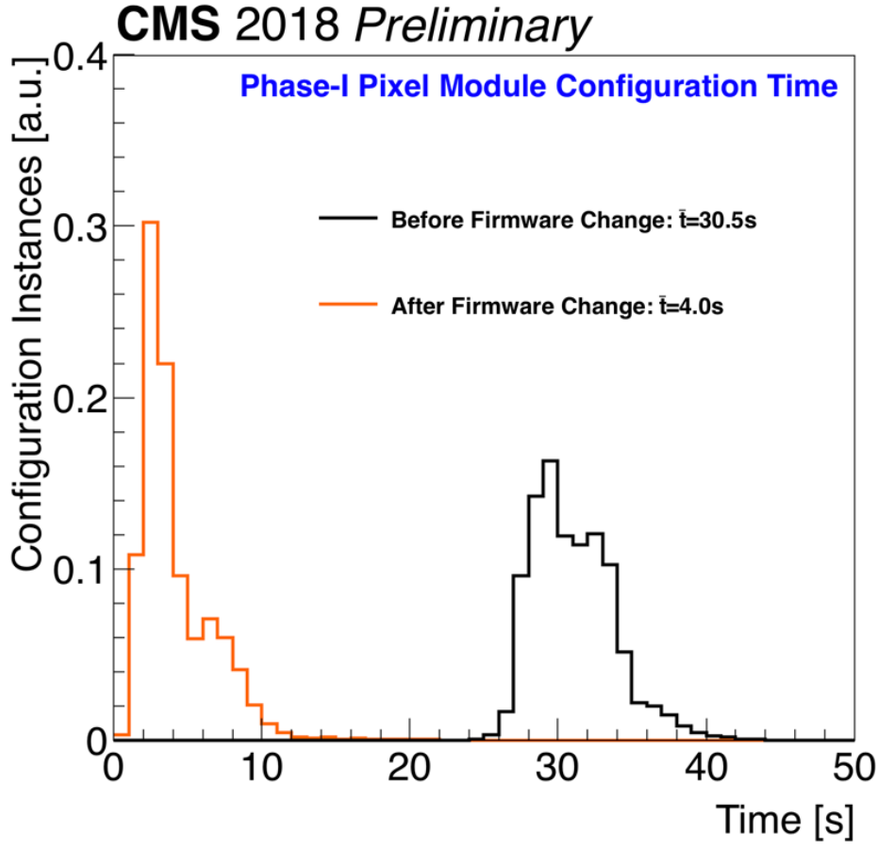
Improvement in 2018 Operation:

- Pixel Frontend Controller programs the modules
- Local DDR memory based firmware for PixelFEC, pre-stored data in segmented memory
- Drastic improvement in module programming time
- Faster calibrations

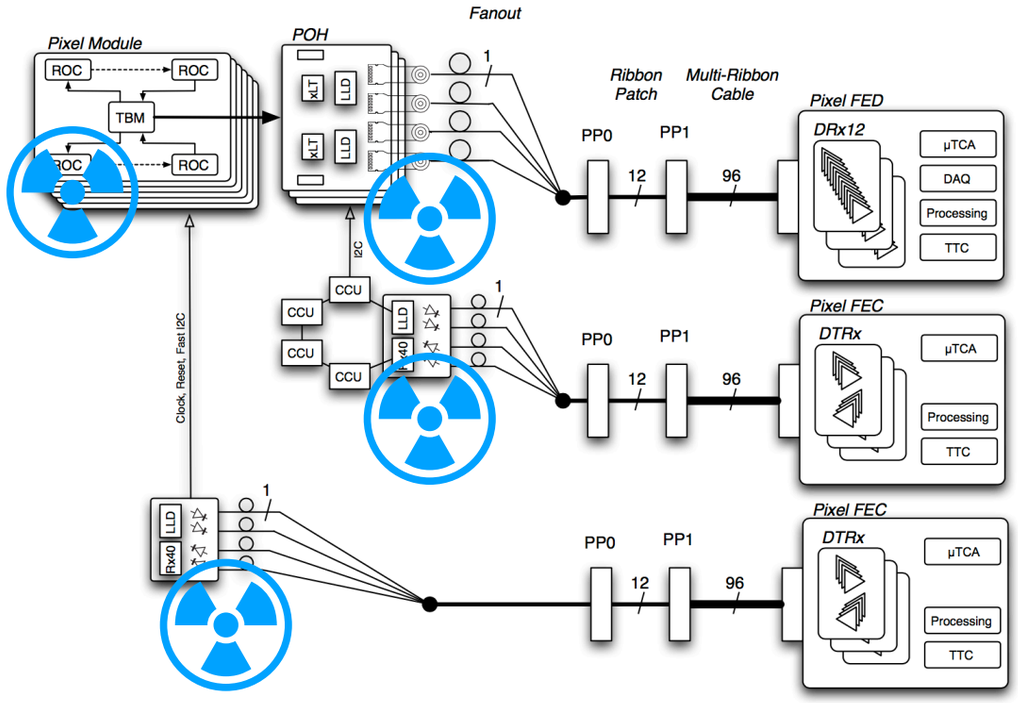


Commands are stored in Segmented memory



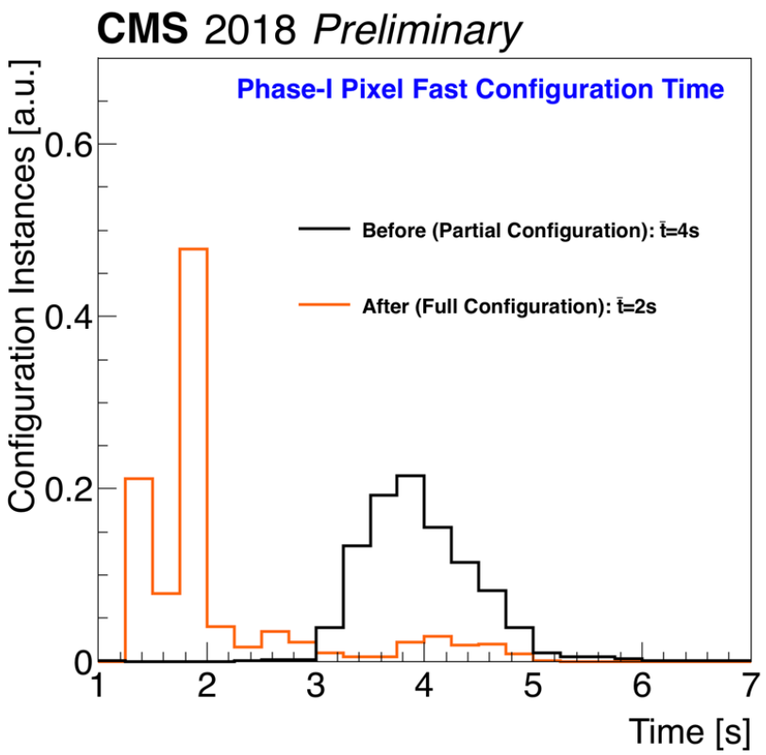


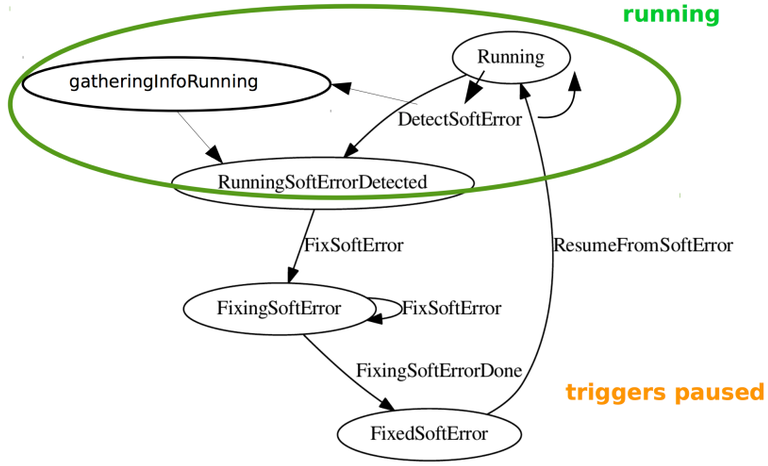
SEU Recovery:



- Pixel detector very close to the interaction point, high rate environment
- Front-end chips, opts-hybrids, CCUs are affected by single event upset
- Refreshing the configuration brings it back to normal, SEU on TBM needs a power-cycling

Automatic Software Scheme:

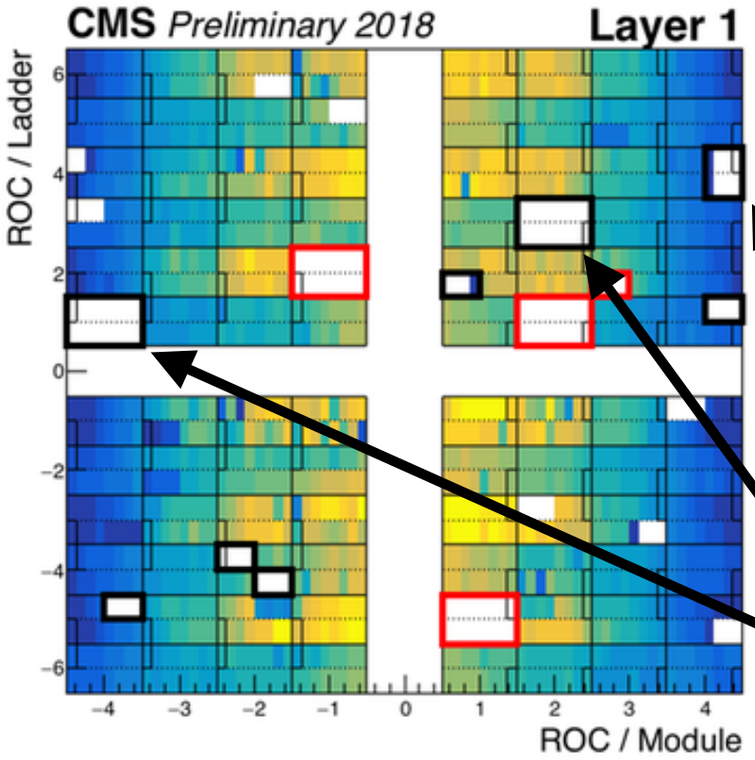


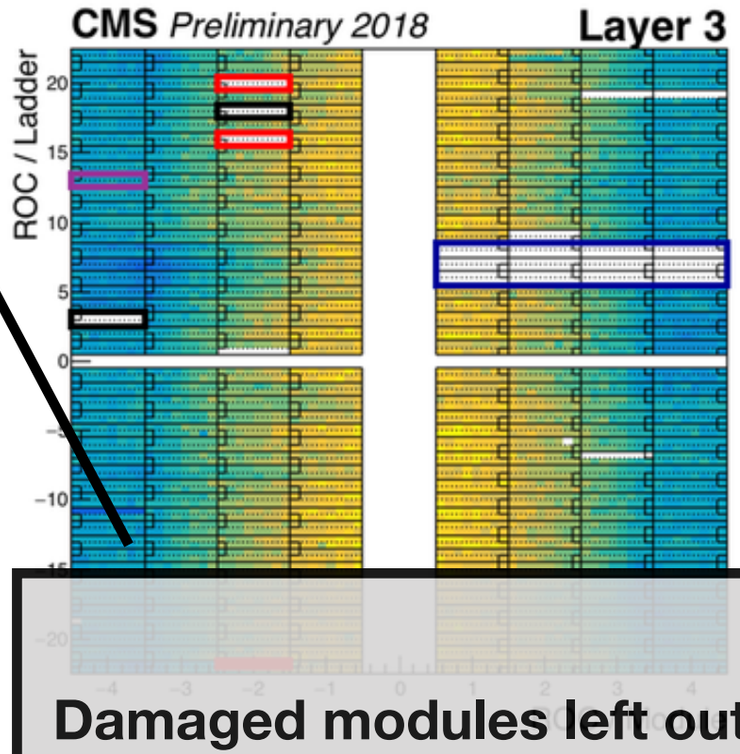


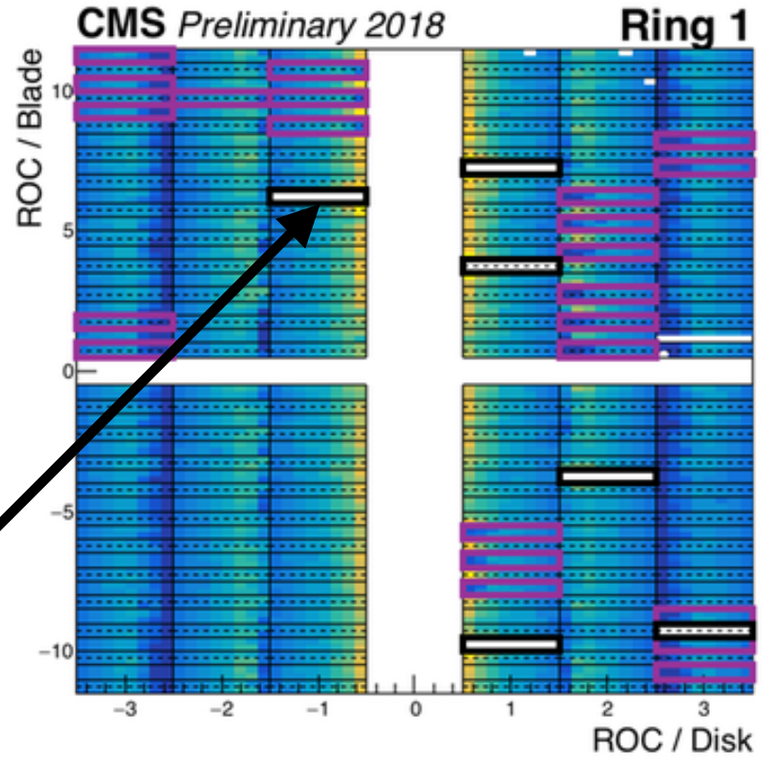
More complete and quicker module configuration during soft error recovery

- **Full Configuration:** Pixel level programming, ~66kB data/module
- **Partial Configuration:** ROC level programming, ~0.5kB data/ module

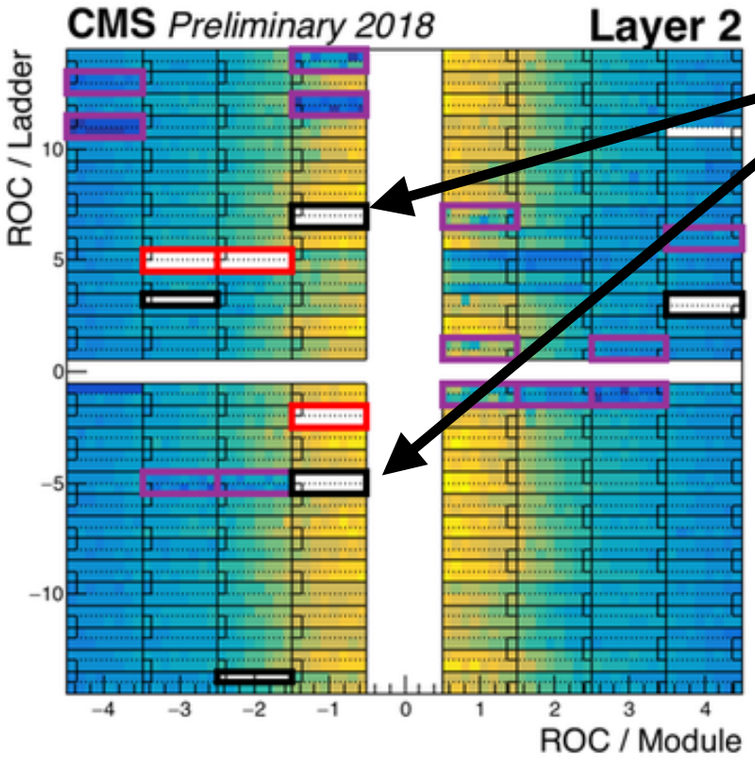
Active Detector: End of 2018

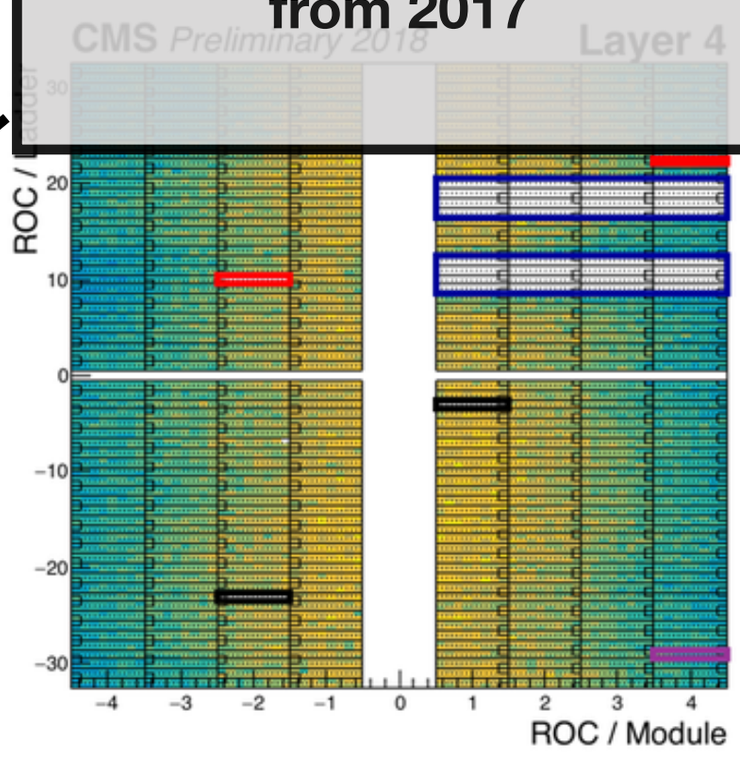


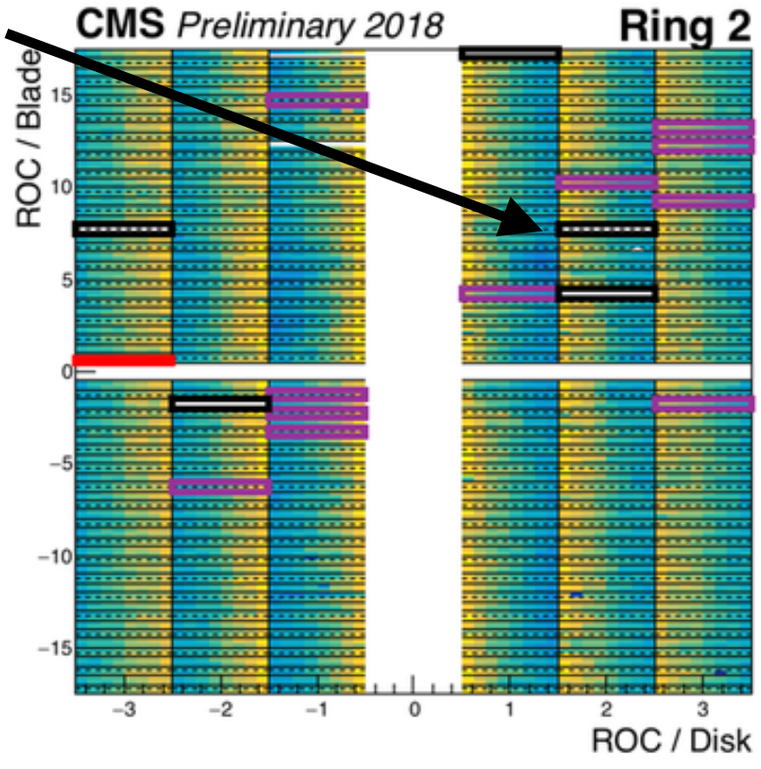




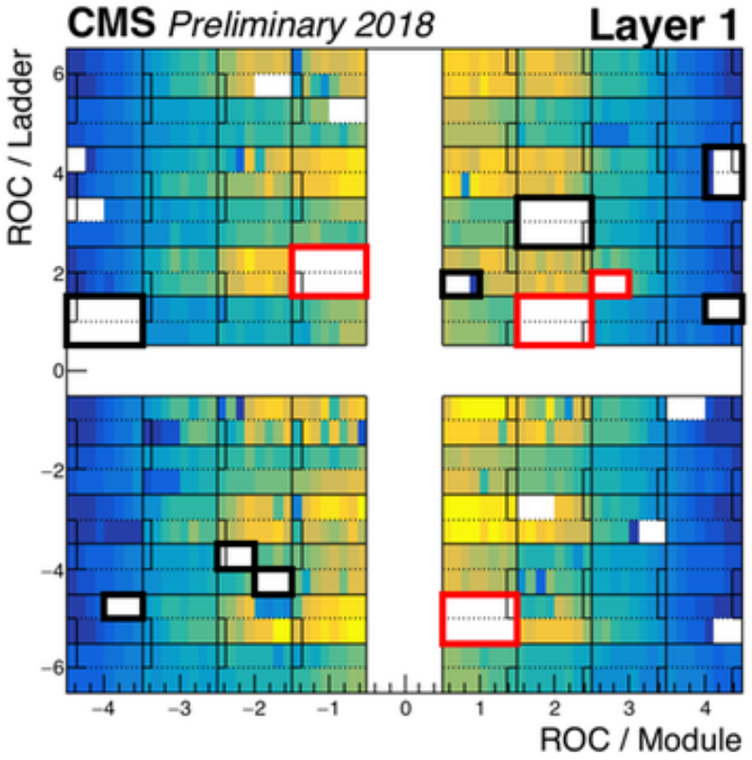
Damaged modules left out from 2017

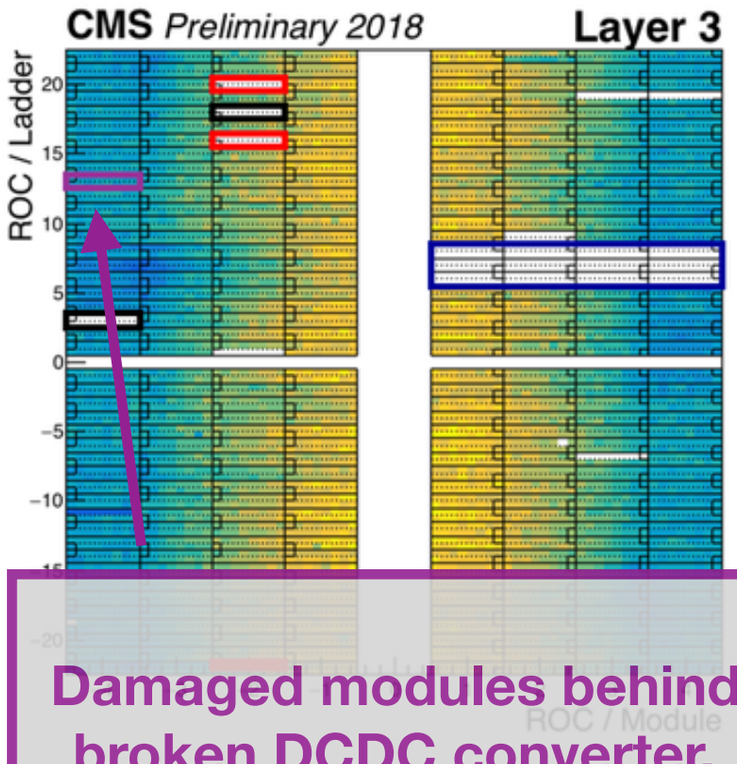


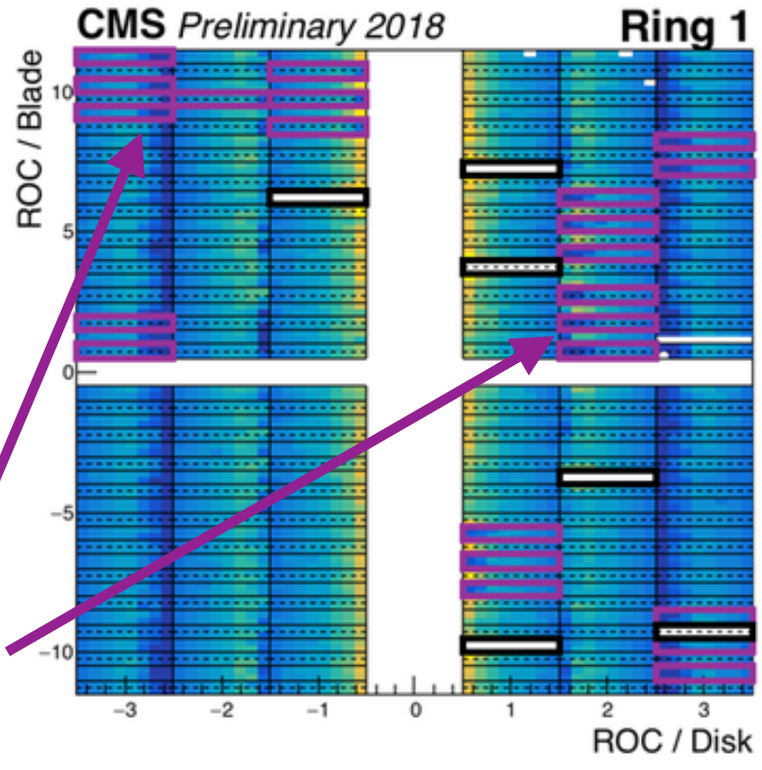




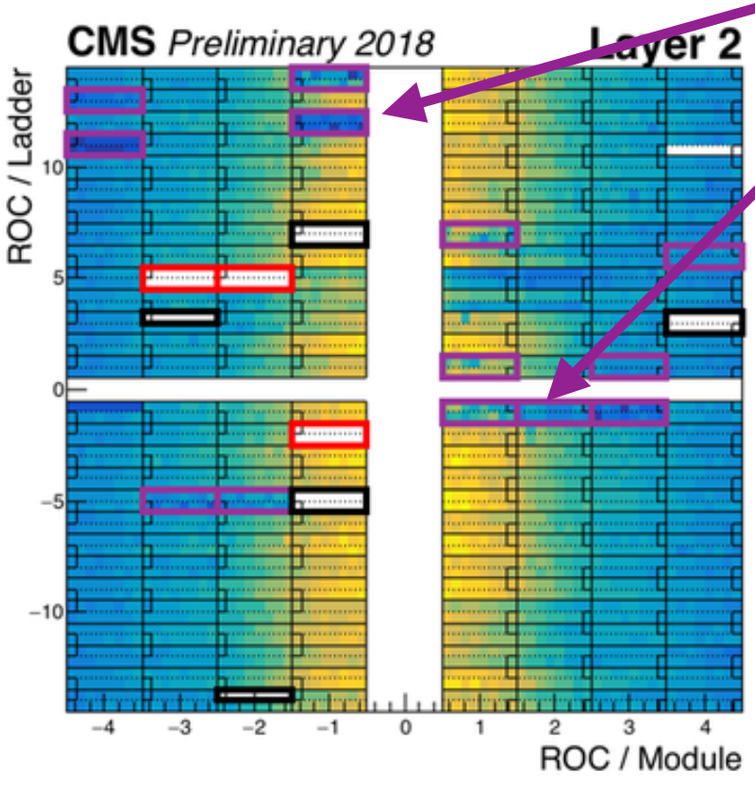
Active Detector: End of 2018

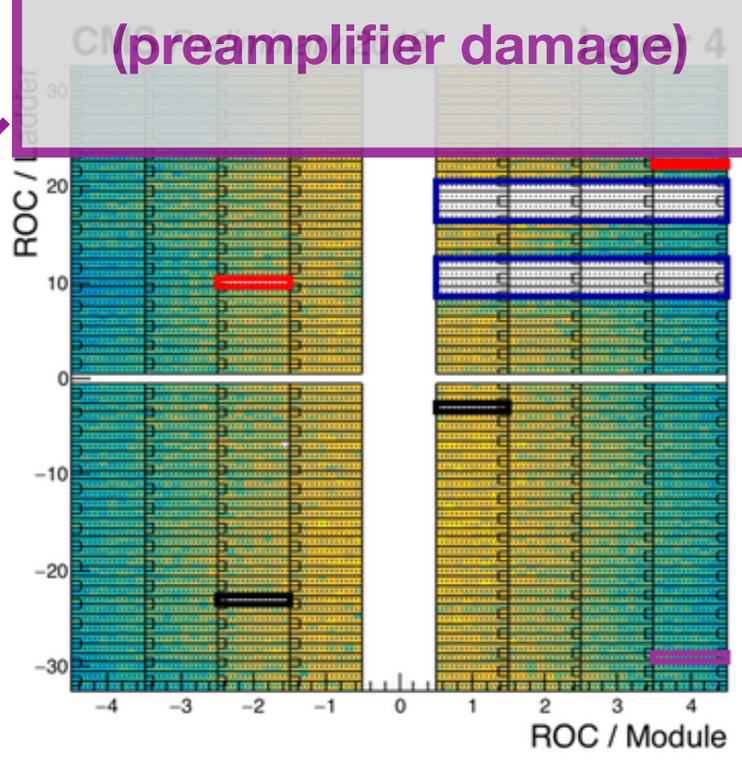


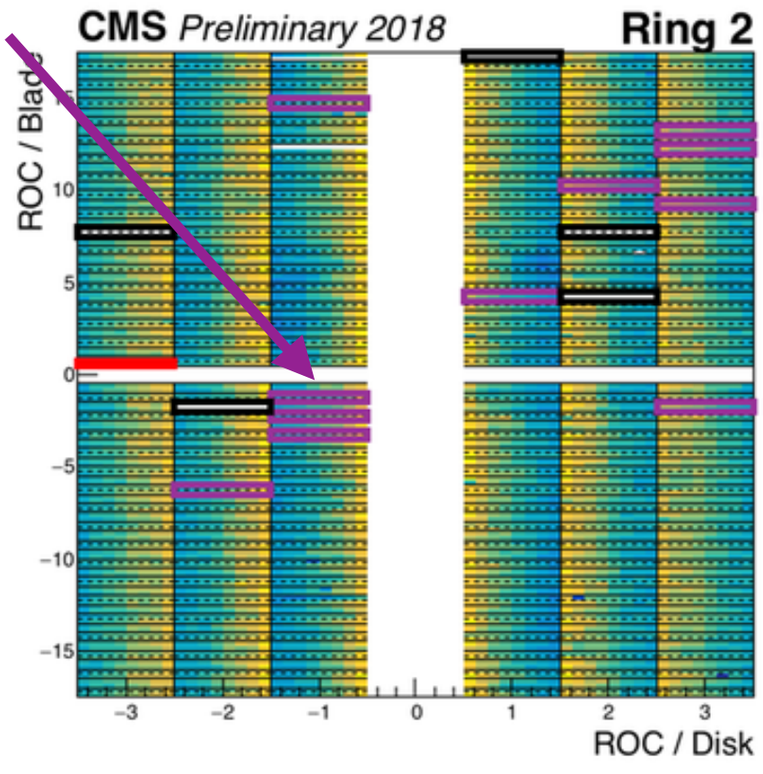




Damaged modules behind broken DCDC converter. (preamplifier damage)







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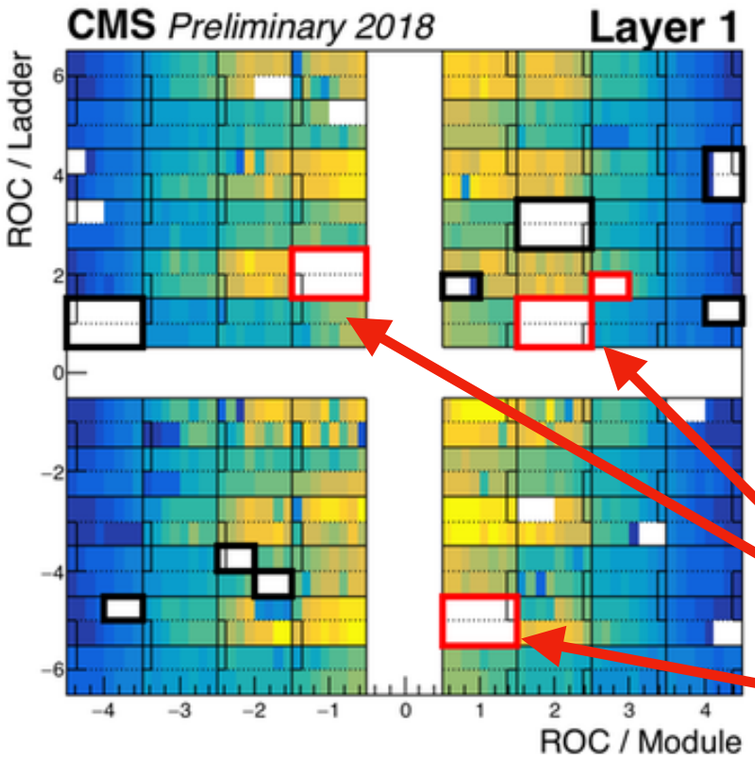
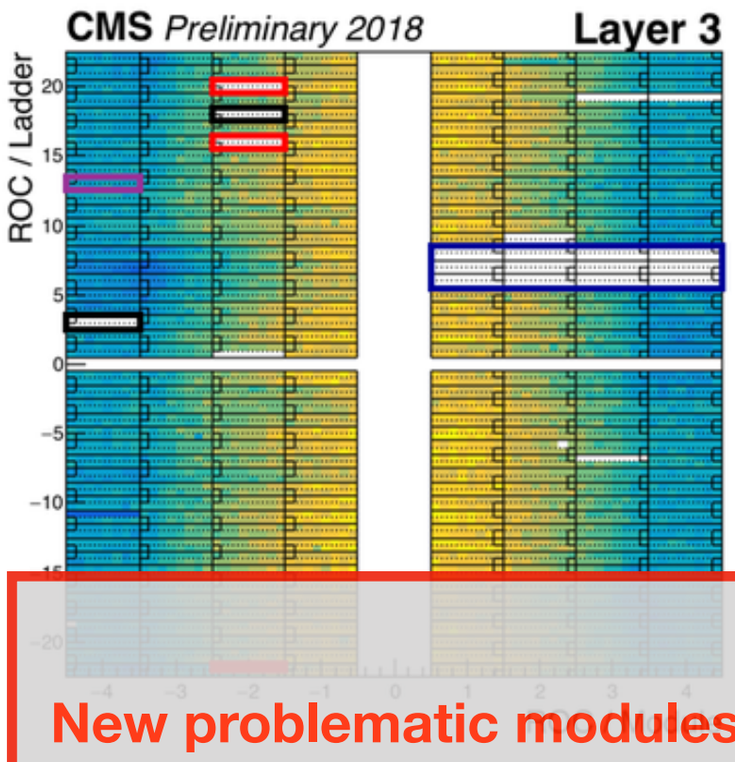
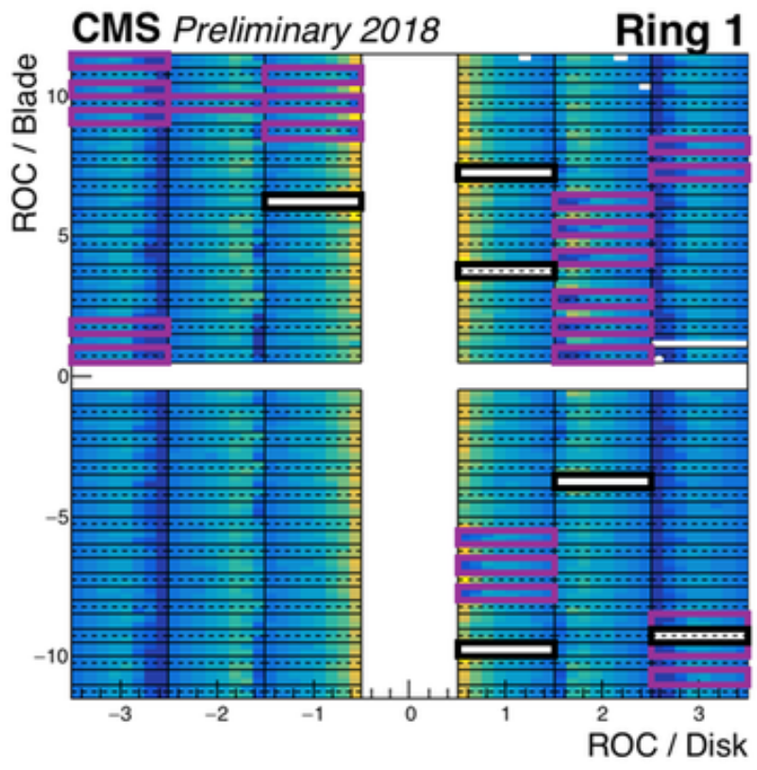
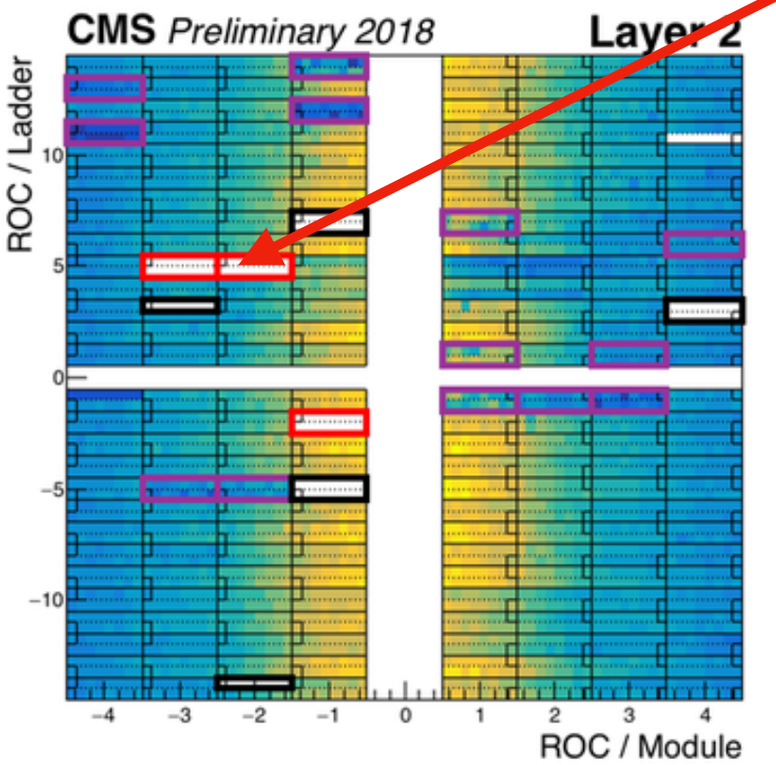
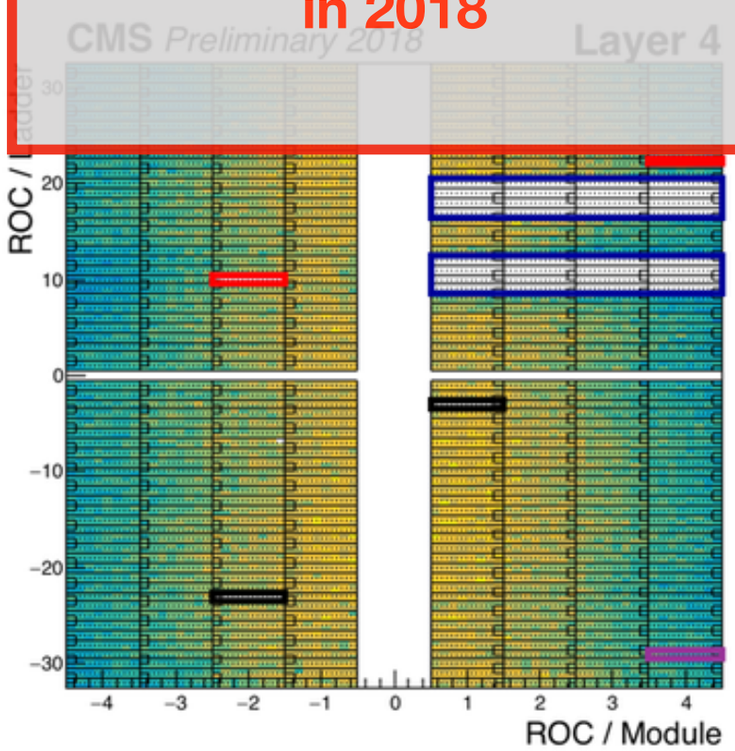


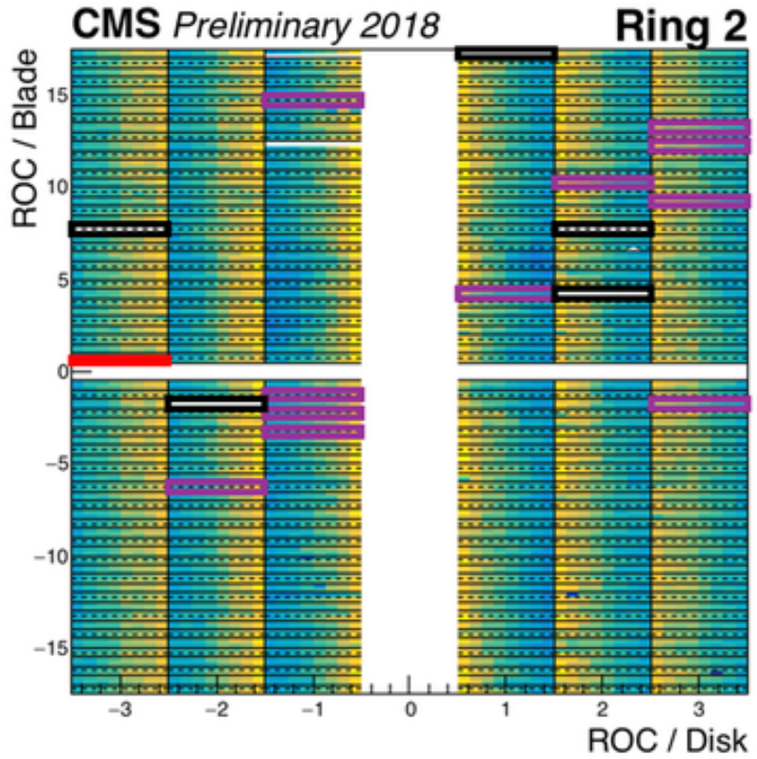




New problematic modules in 2018







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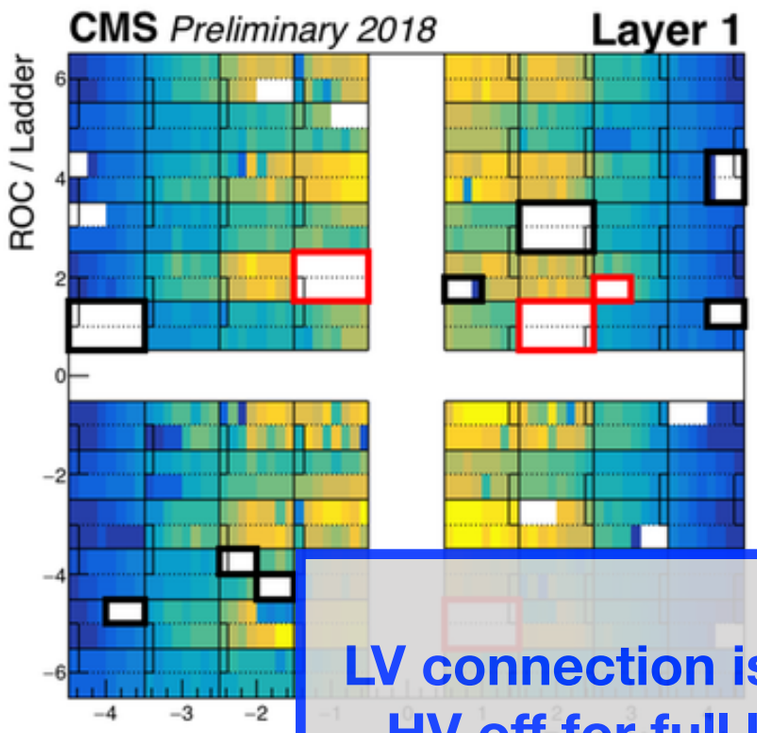
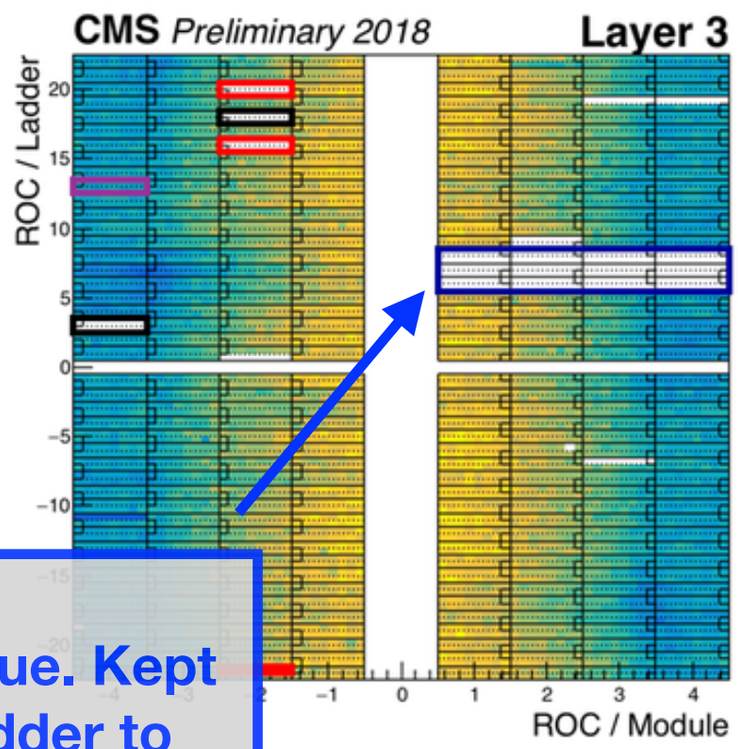
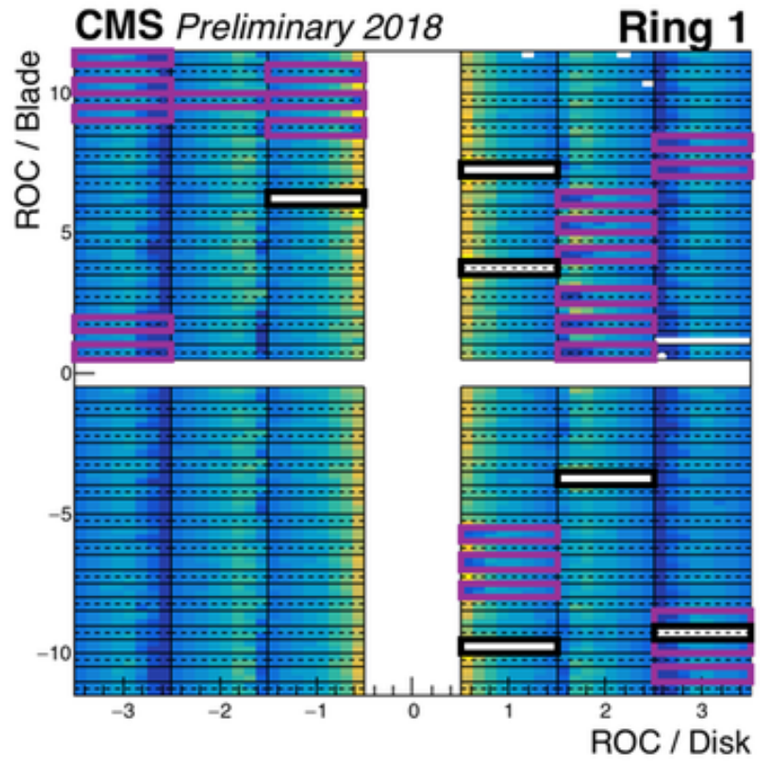
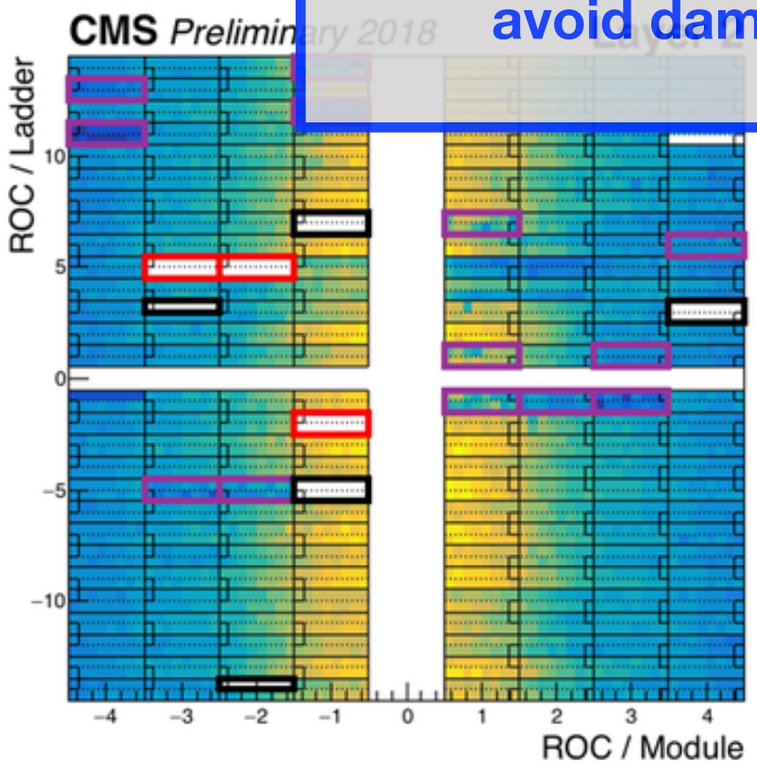
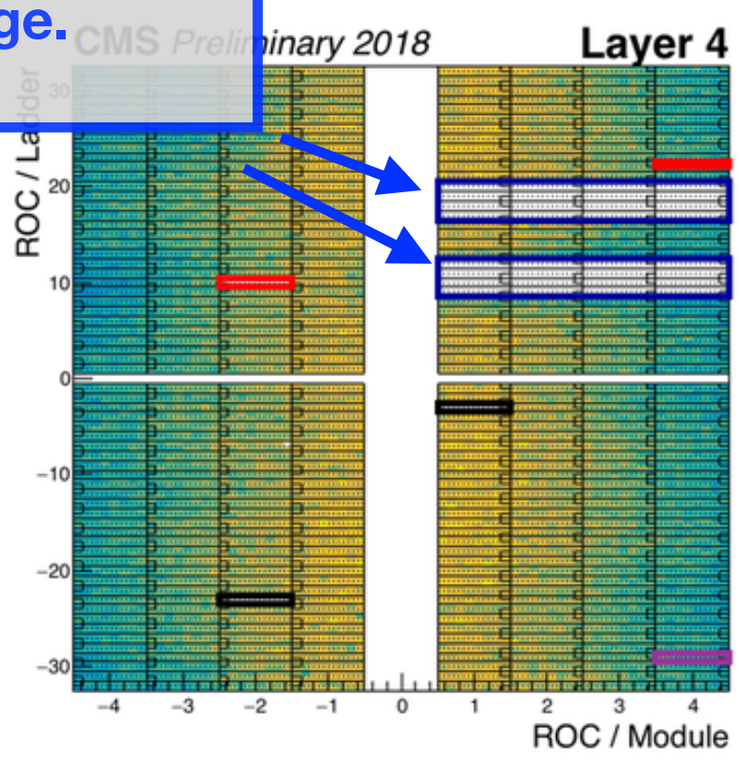


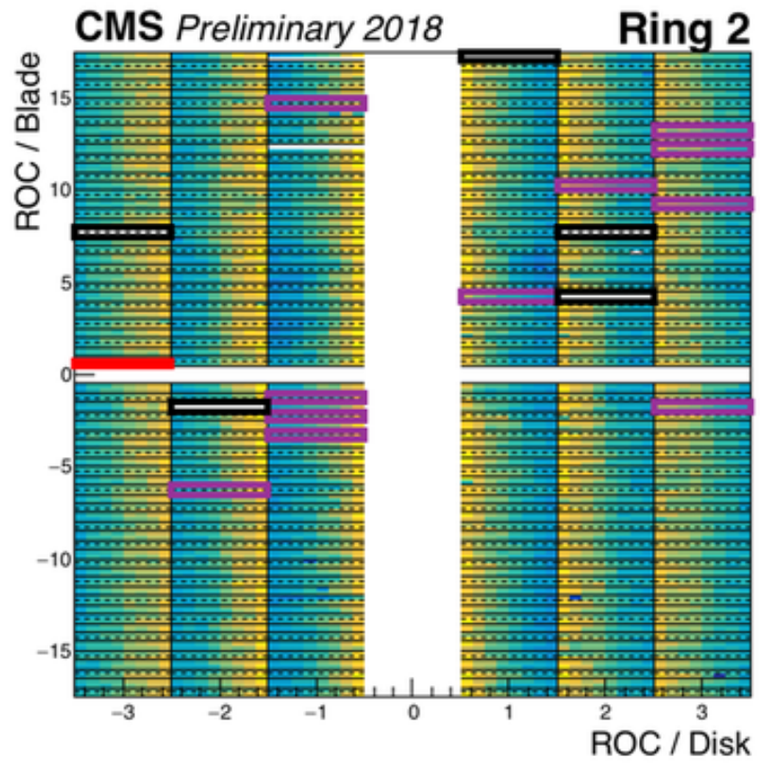




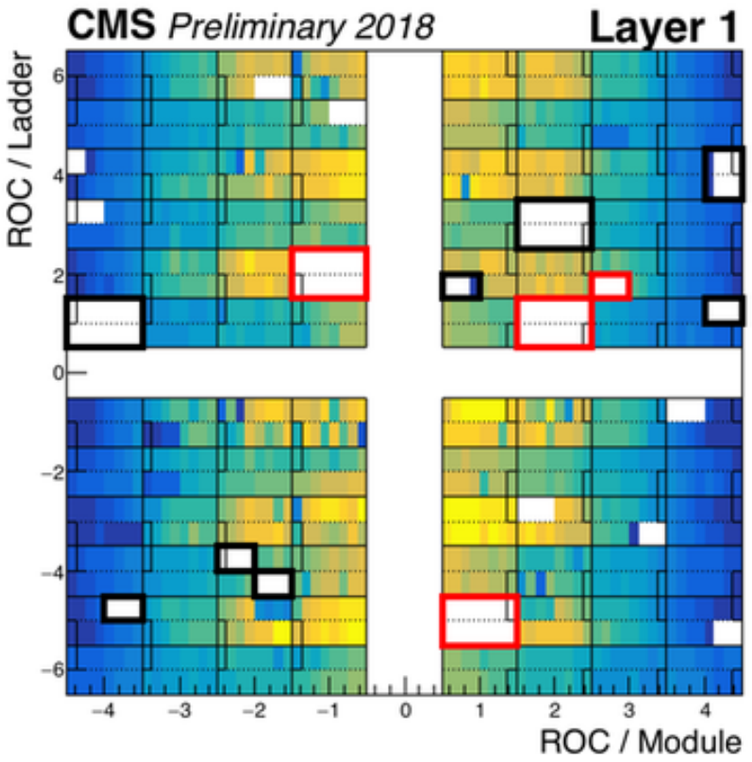
LV connection issue. Kept HV off for full ladder to avoid damage.

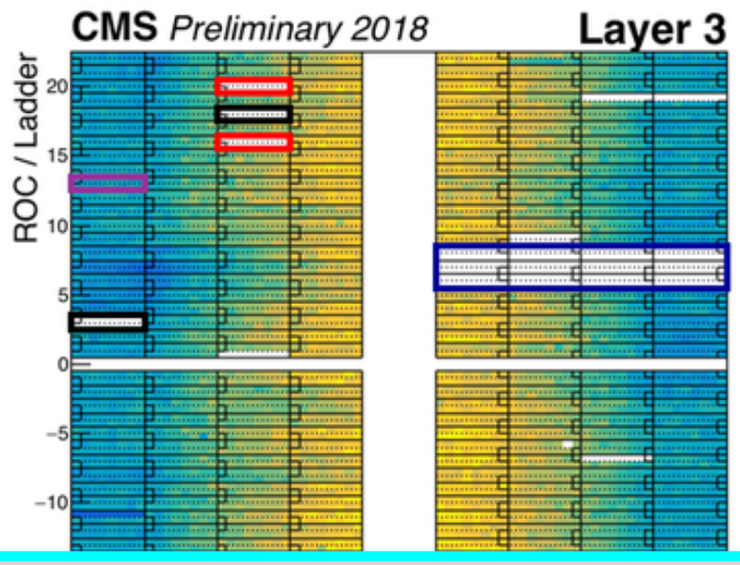


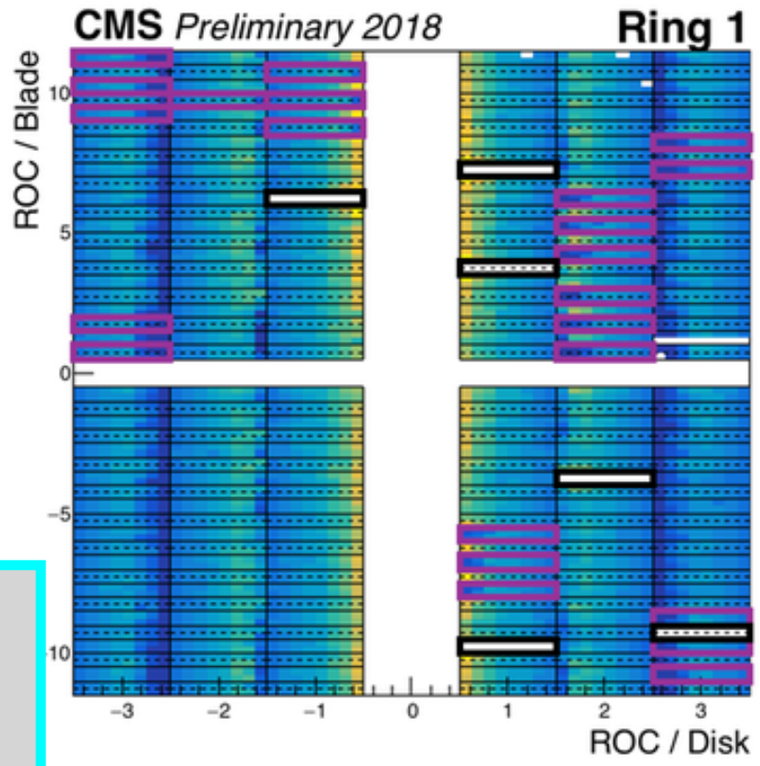




Active Detector: End of 2018

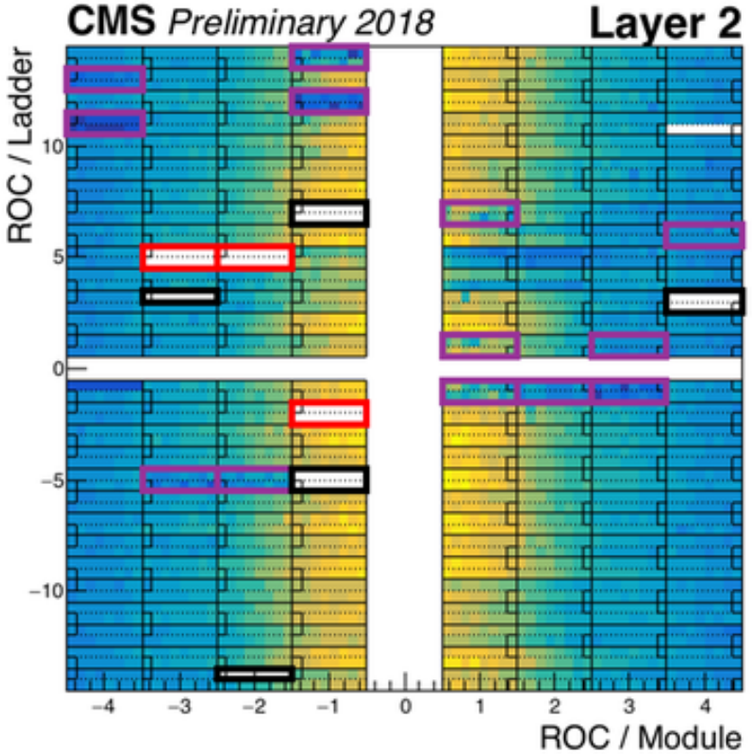


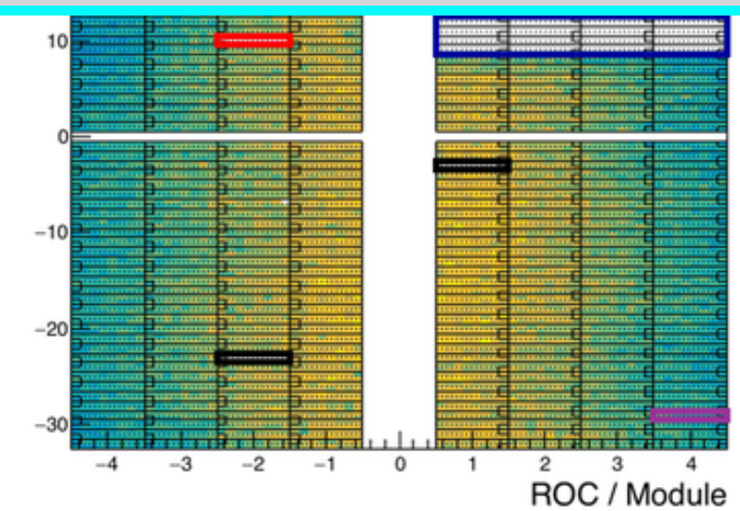


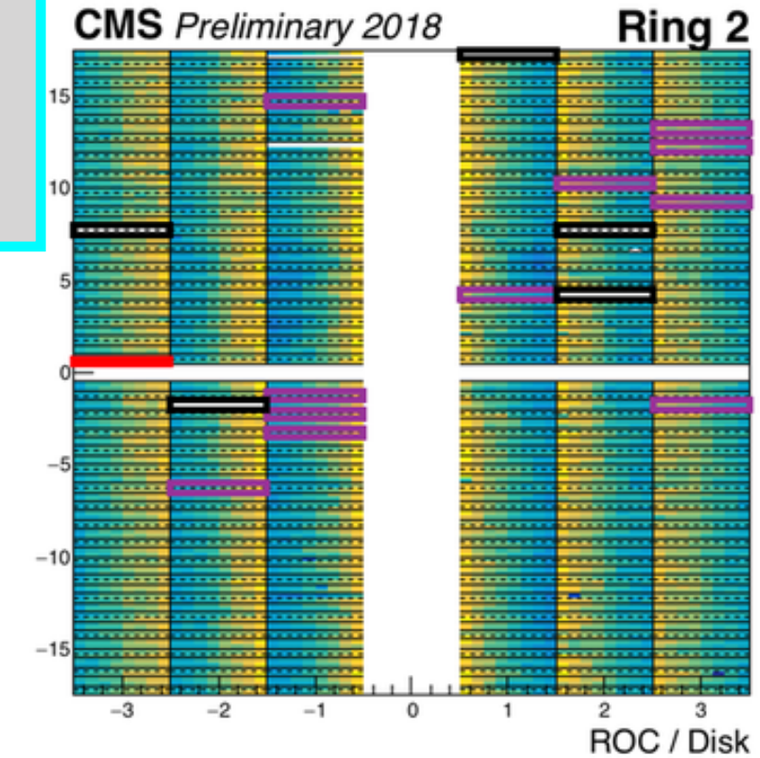


94.3% active detector fraction after the end of 2018 operation

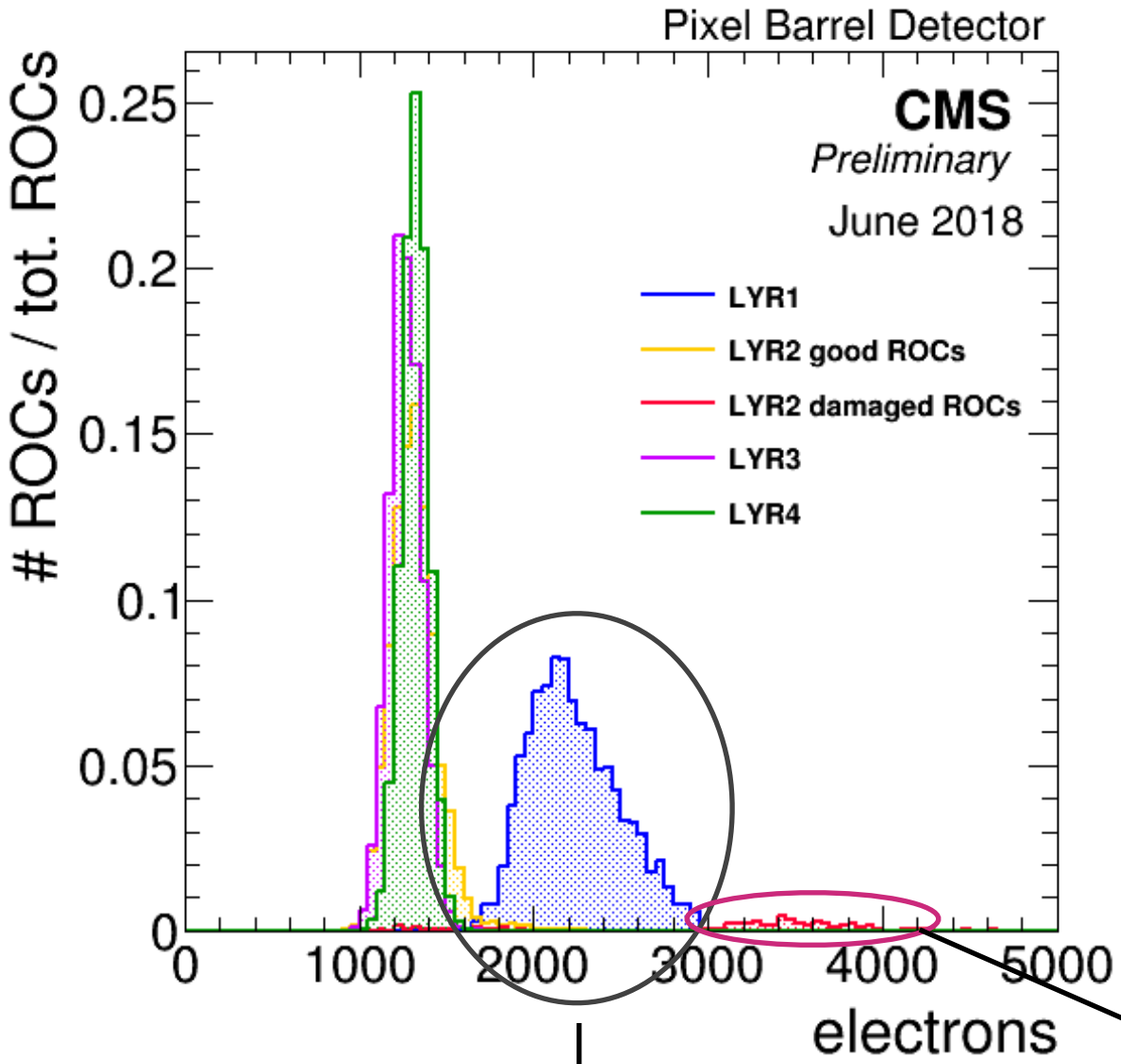
Did not break a single DCDC

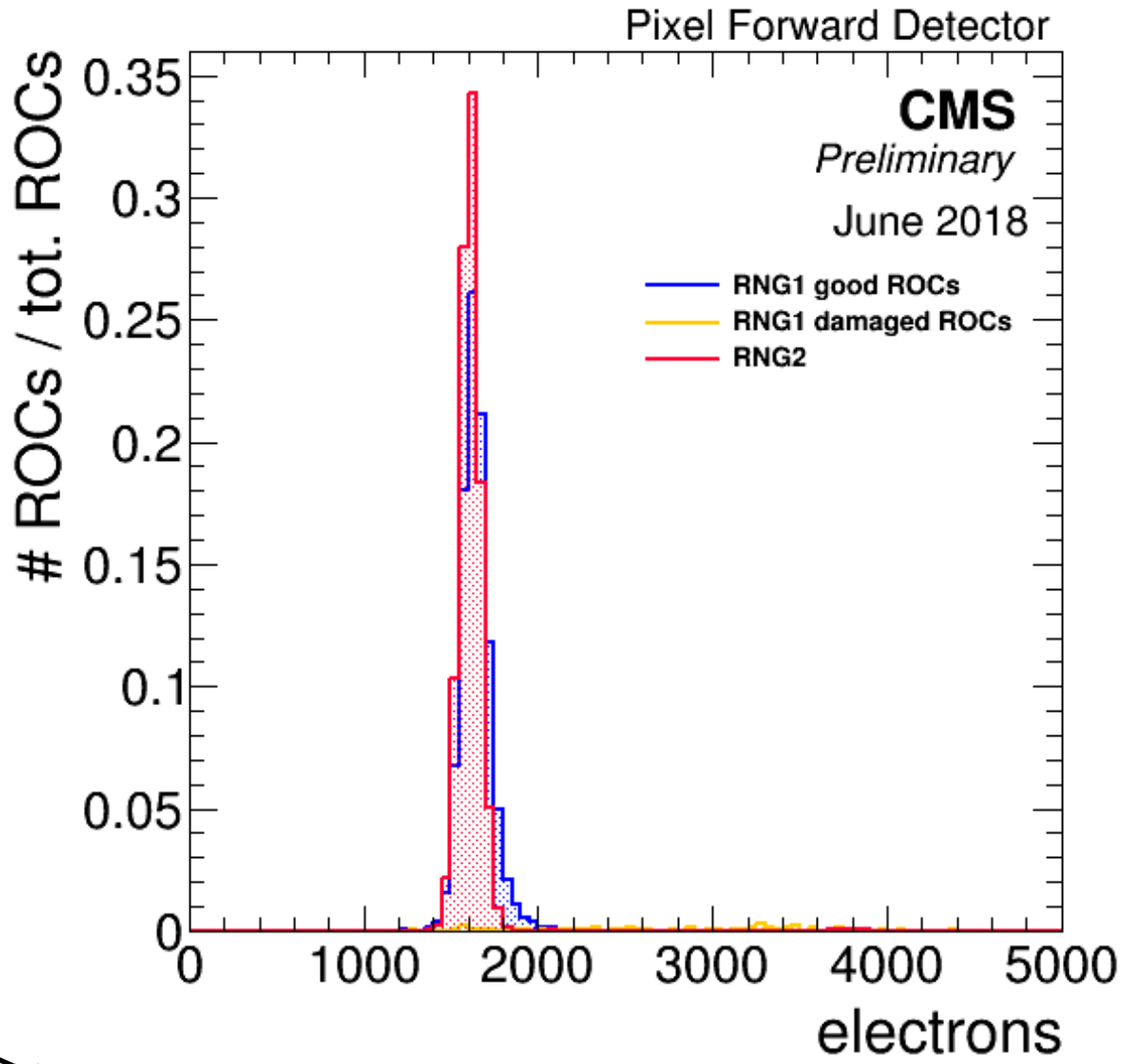






Detector Thresholds:



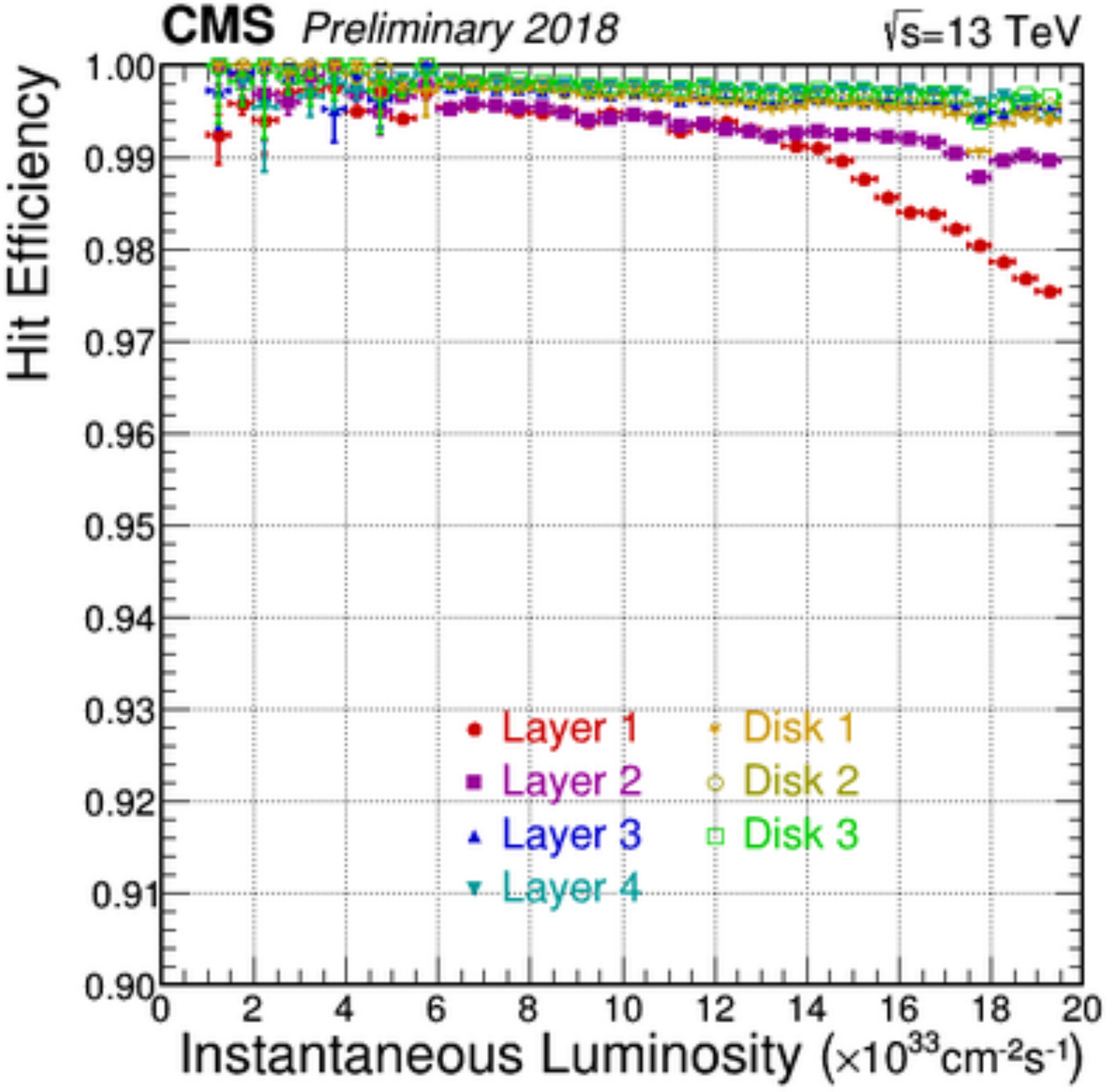


Damaged ROCs because of DCDC issue

- Higher threshold in Layer-1 due to cross talk noise
- Changed programming sequence of the ROC to mitigate the issue, recovers hit efficiency
- Problem is being addressed in new version of PROC600

See Danek's talk after lunch on Layer-1 Issues and Solutions

Hit Efficiency:

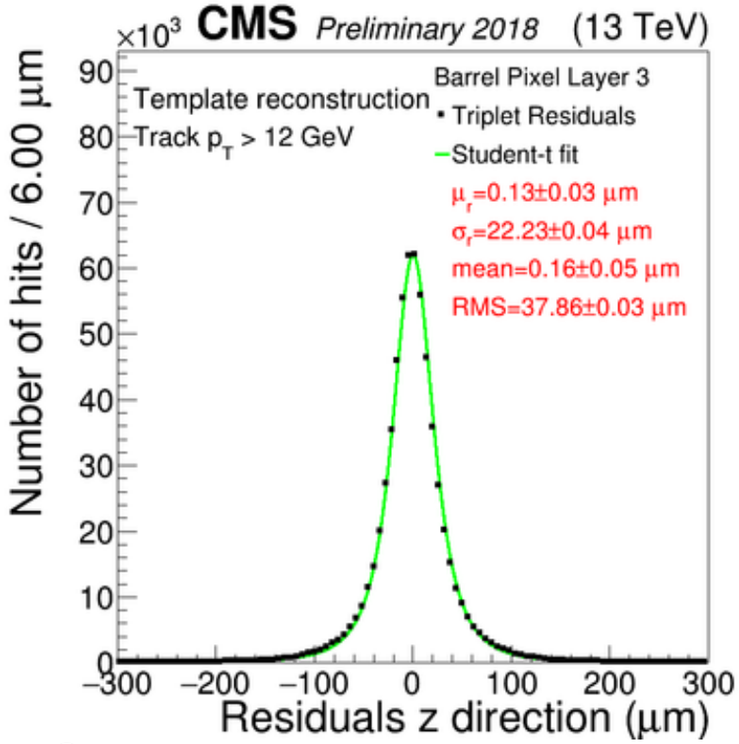


Overall excellent hit efficiency by Phase-1 detector

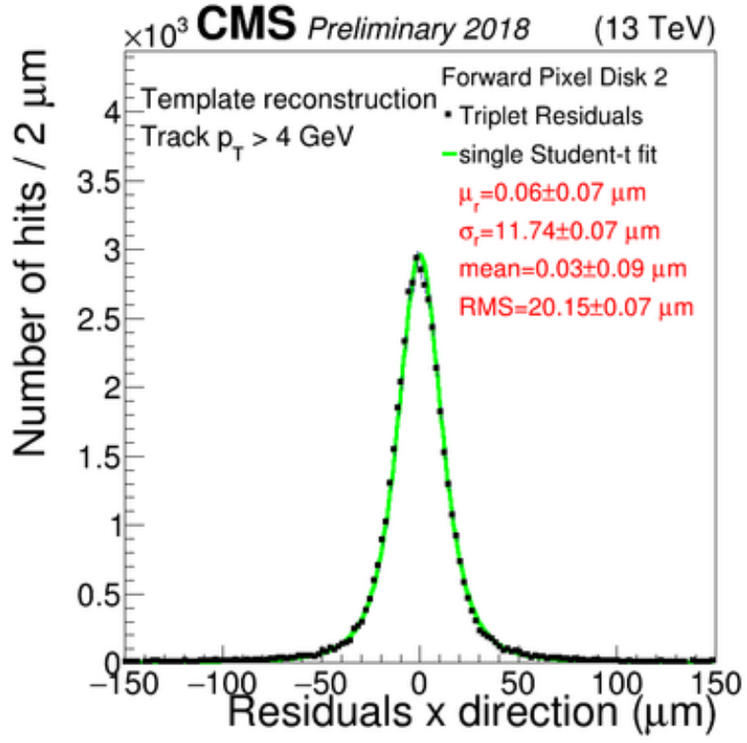
Small Layer-1 inefficiencies in low and high luminosities are understood.
Being addressed in new PROC600.

See Danek's talk after lunch on Layer-1 Issues and Solutions

Precision Tracking, Residuals:



$z : 22\mu m$

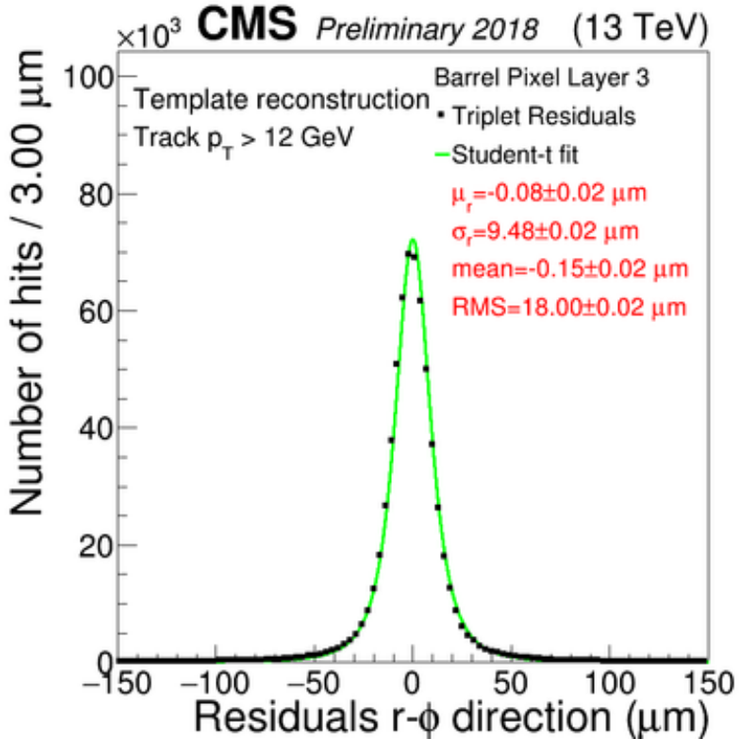


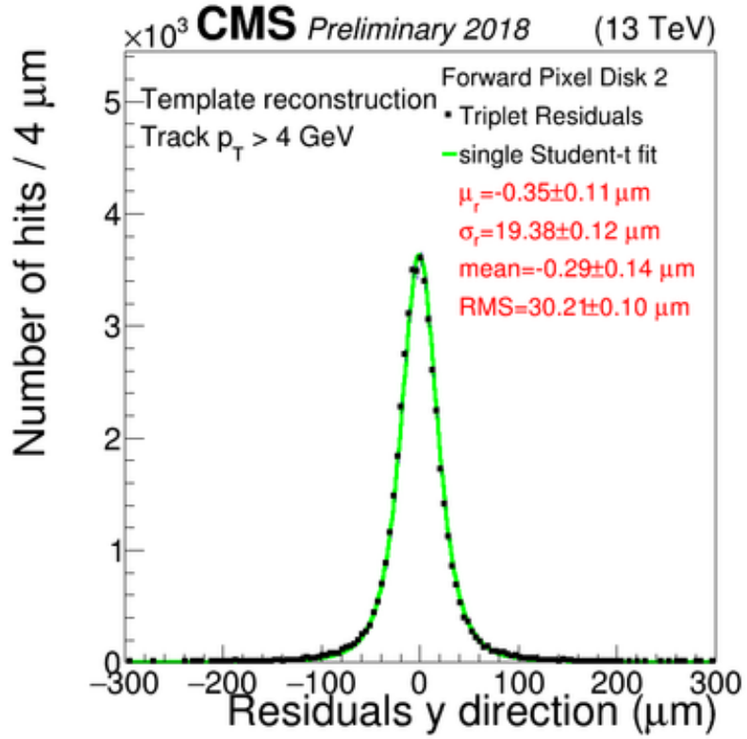
$x : 12\mu m$

Layer-3 **Disk-2**

Excellent hit residuals/resolutions

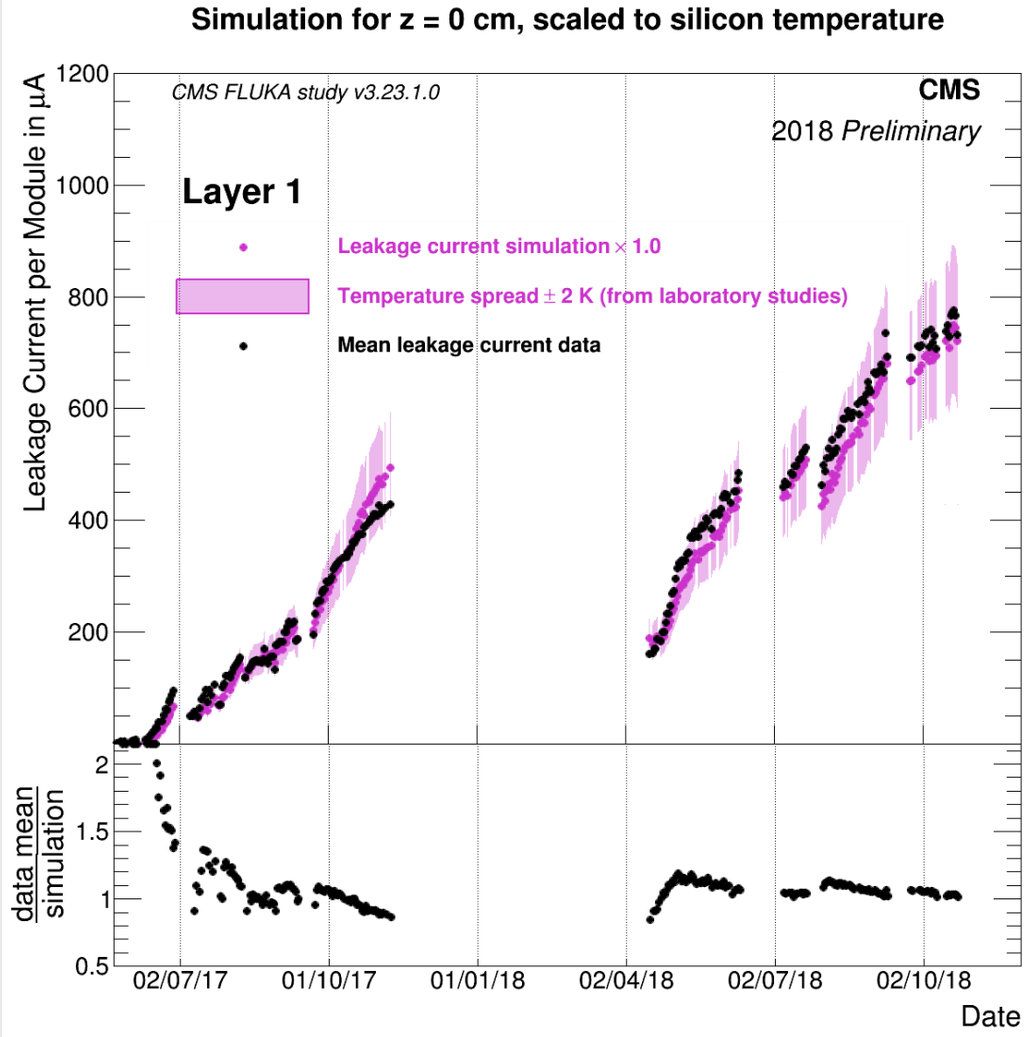
$r\phi : 9.5\mu m$

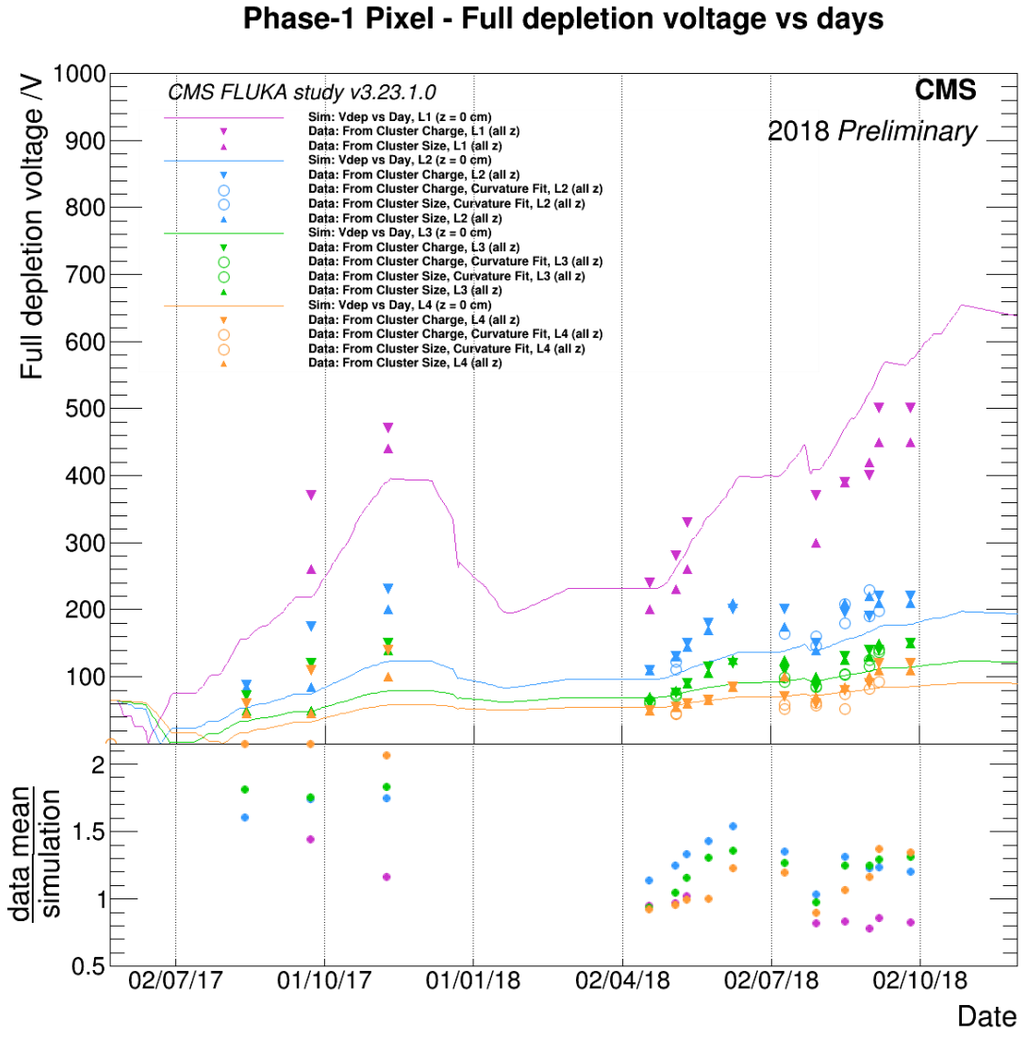




$y : 19\mu m$

Monitoring: Leakage Current and Depletion Voltage



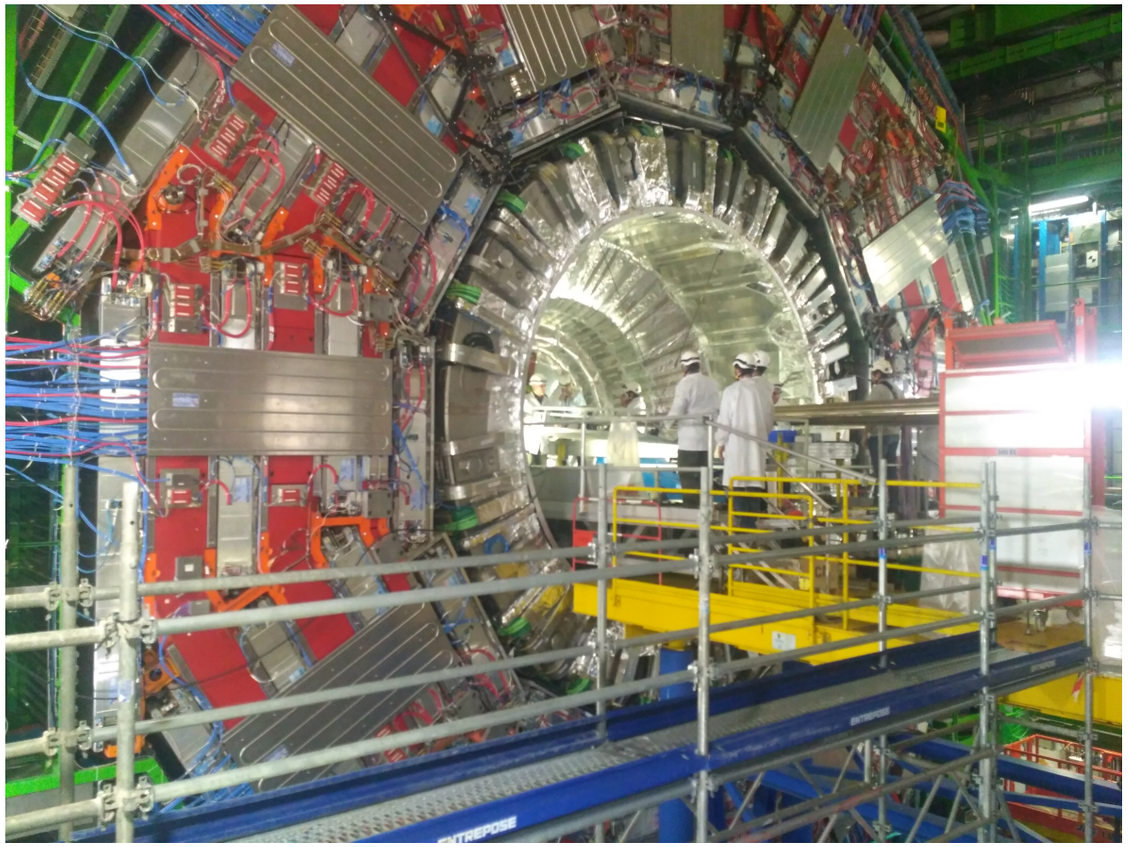


- Prediction of leakage current agrees well with measured values from the detector
- No limitation from power supplies

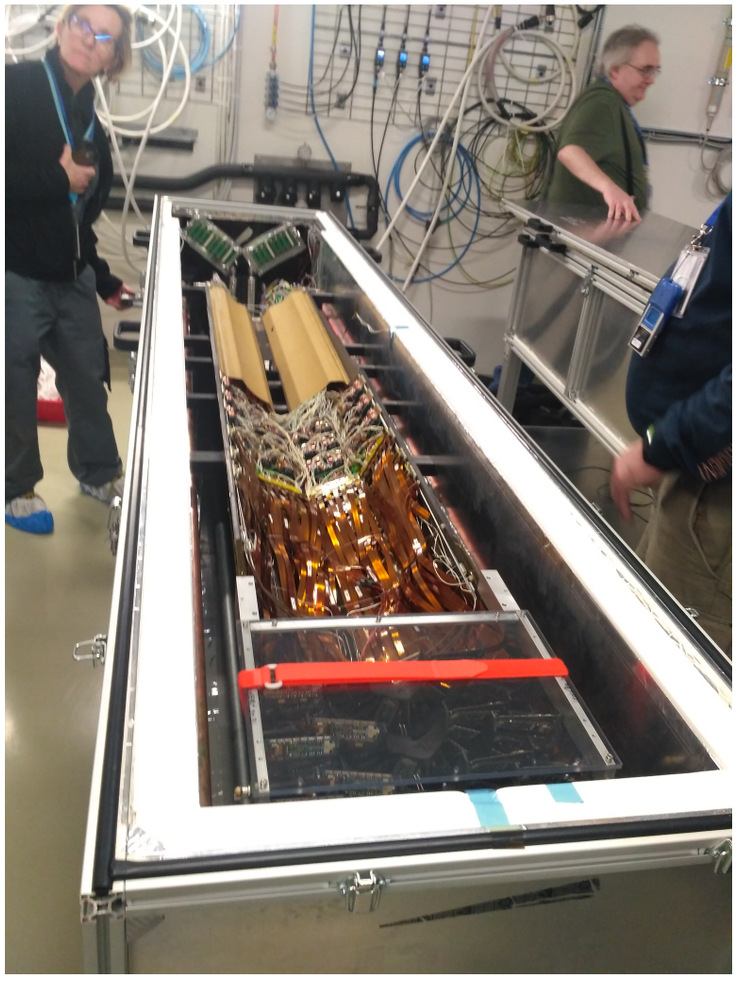
- Hamburg model to simulate the evolution of depletion voltage
- Need ~800V for Layer-1 in Run-3

Long Shutdown-2 Activities/Plan

Detector in Cleanroom:



- Detector was extracted from experimental cavern in January, 2019



- Detector kept inside cold box in cleanroom
- Module temperatures ~ 0-2 degC, to protect the silicon sensor

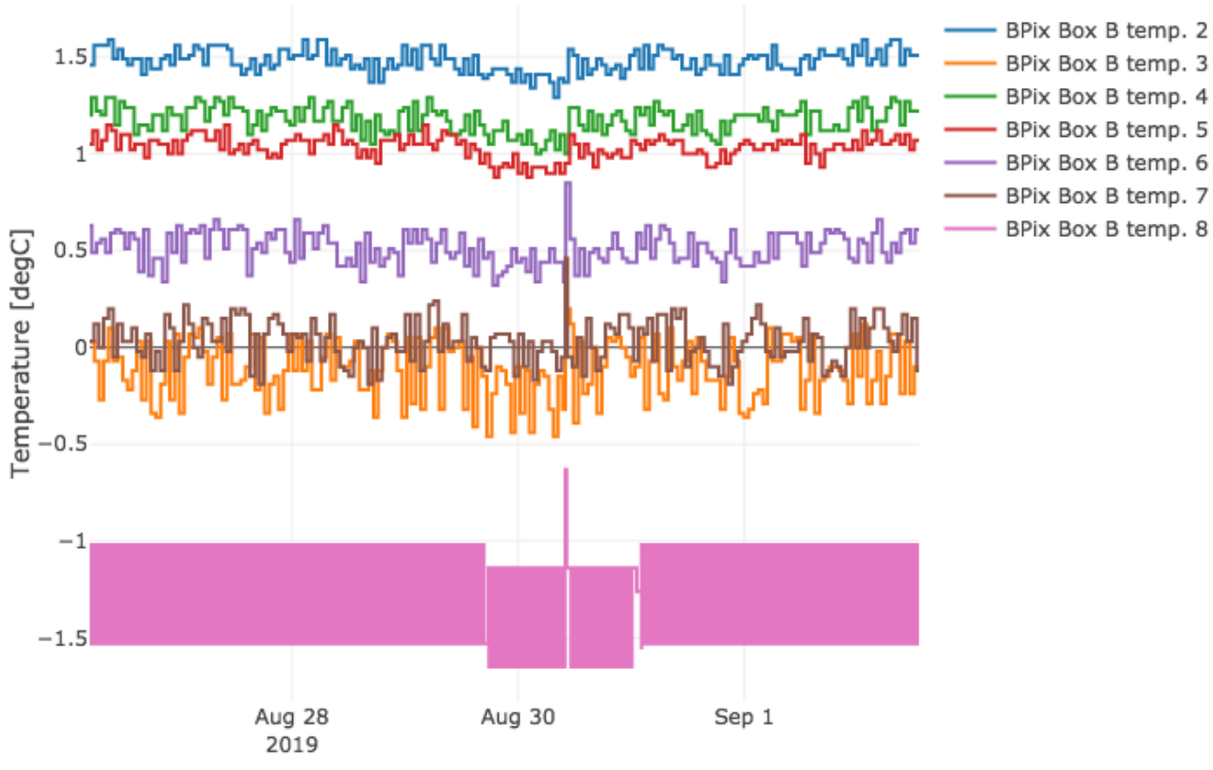
Detector Refurbishment:

- Layer-1 will be fully replaced with improved Readout Chip (PROC600v4)
- This will fix most of the problems as observed during previous operation
- Also include new TBM, fixing the latching issue
- Replace DCDC damaged modules in Layer-2
- Fix module power connection problems
- Upgrade power supplies to deliver 800V, 15 mA
- Modify FPix power board to improve the granularity of HV distribution
- Replace all DCDC converters with the latest version of the FEAST chip

DAQ Software and Monitoring Improvements:

- Restructuring DAQ software to make it easier to develop and maintain
- New UI and more added monitoring
- Introduce fast signal based reconfiguration of frontend registers in regular interval to recover from SEU
- Calibration code developments and speed up with new DDR based FEC firmware
- Pixel FEC and FED firmware developments
- New pixel online monitoring system: centralized information, possible to correlate variables, friendly user interface

Cold box temperatures



New PixelMonitoring System

Summary:

- Successful commissioning and operation of the detector during 2018
- No major issues encountered
- 94.3% active detector by the end of 2018 operation, excellent position resolution and hit efficiency
- It was an operational achievement not to break a single DCDC in 2018
- PixelDAQ also performed exceptionally, only 5% of the total downtime due to pixel
- LS2 refurbishment works are running on schedule
- New Layer-1 and other refurbishment will ensure an excellent detector until the end of Run-3