- VERTEX 2019 -

# Design of the CMS MTD Endcap Timing Layer

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on behalf of the CMS Collaboration

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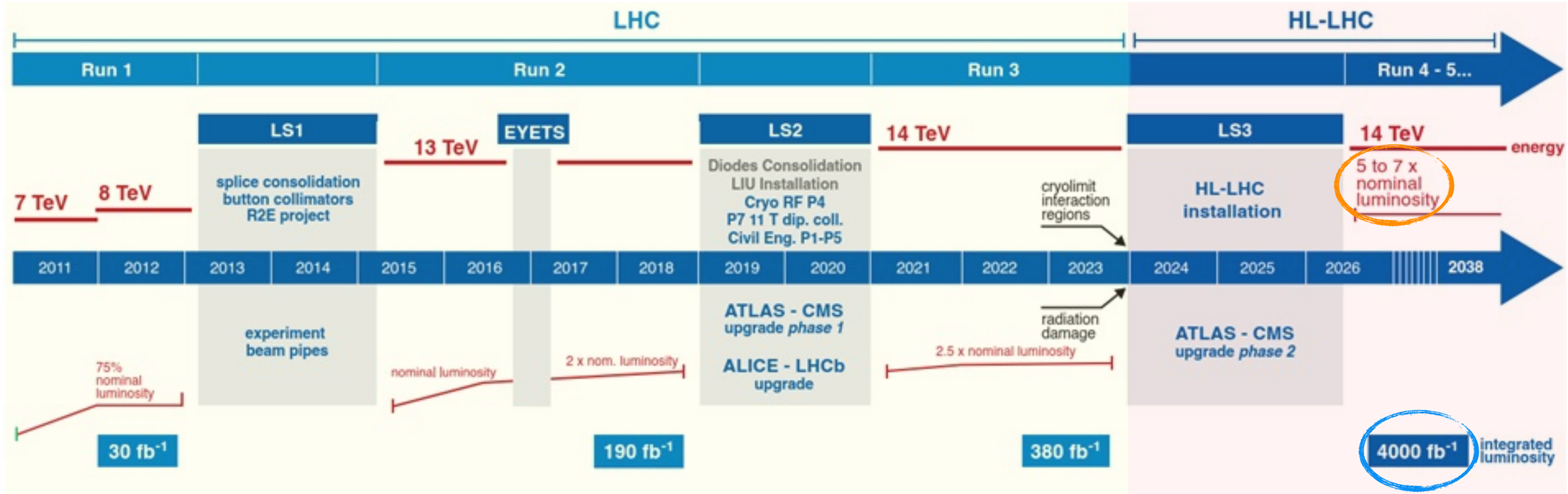
# The HL-LHC challenge




Factor ~5 increase in instantaneous luminosity ⟹

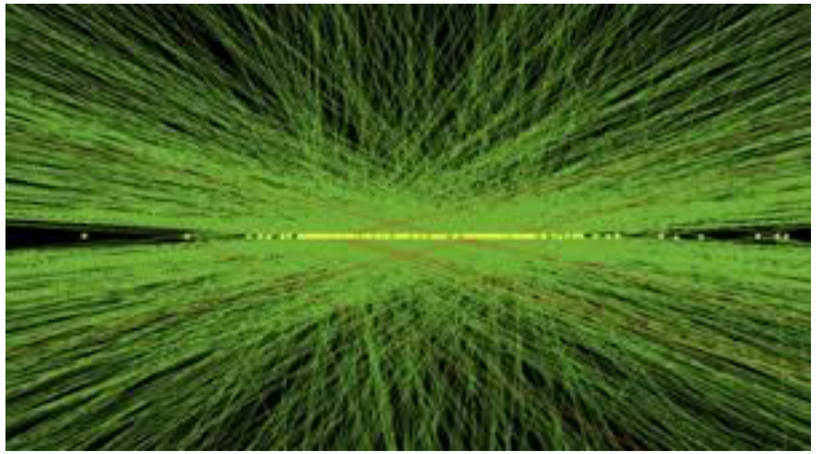
- high hit rate;
- high level of event superposition (pileup)

Factor ~10 increase in integrated luminosity ⟹

- high radiation dose

# Vertex reconstruction vs. pileup

$\mu$ = 200

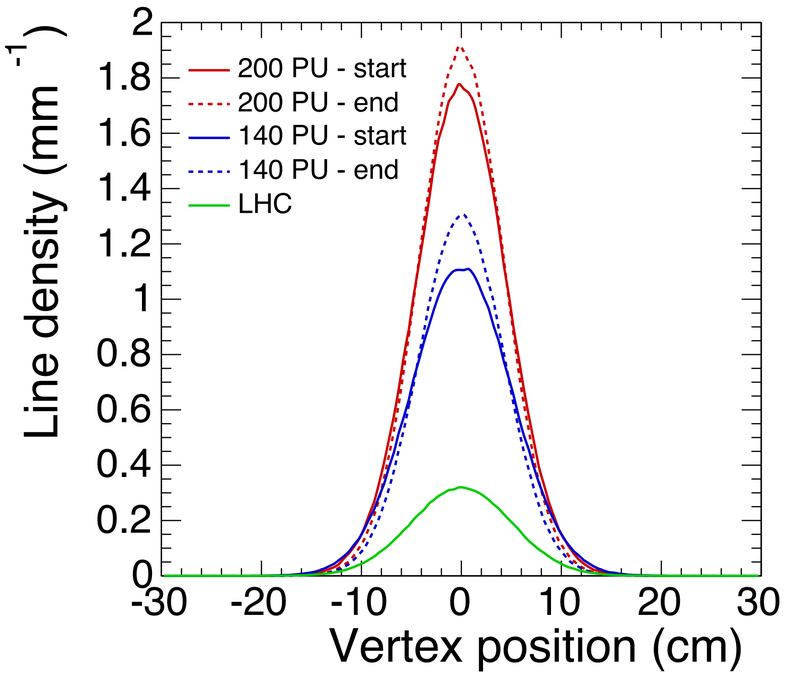


In CMS, pileup mitigation by *Particle Flow* technique

- jets built from all reconstructed tracks in identified vertices
- statistical-based correction of neutral contribution

Expected pileup at HL-LHC up to $\mu$ ~180-200 (vertices/ bunch crossing)

- current level: $\mu$ ~50

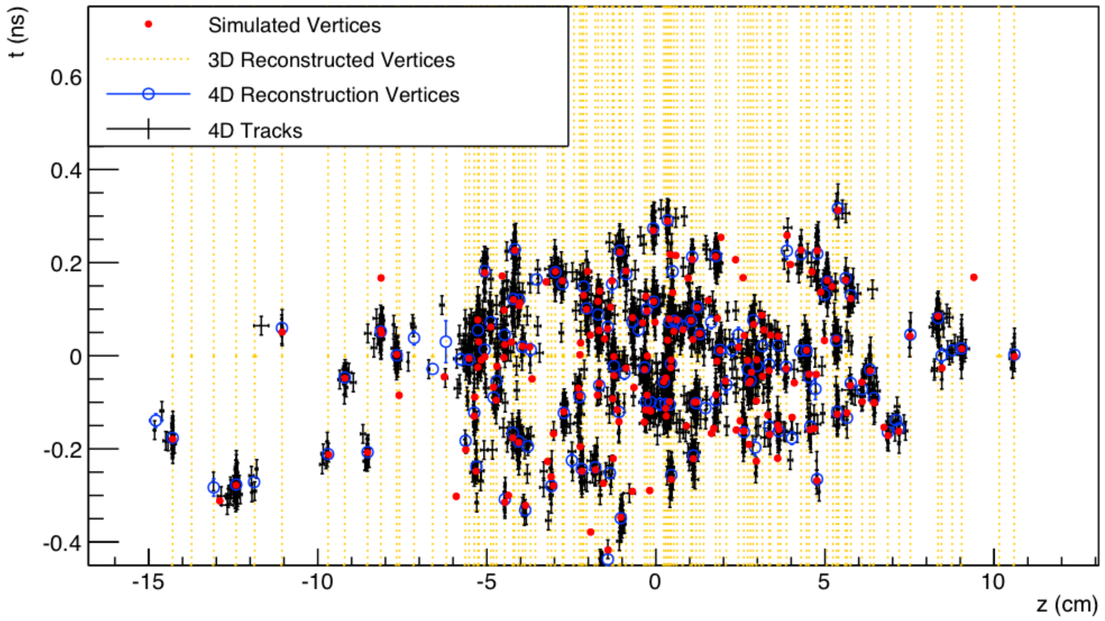



Optimal $\Delta z$ window for efficient vertex identification: ~1 mm

At HL-LHC, vertex density 0.3 mm$^{-1}$ → 1.2 - 1.9 mm$^{-1}$

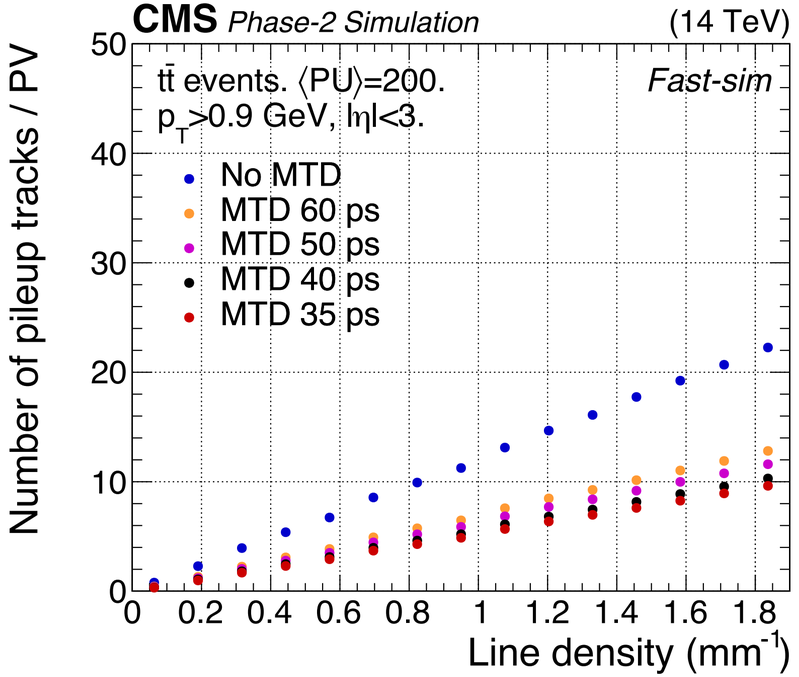
- improved resolution of upgraded inner tracker cannot compensate highest expected levels of pileup
- inefficiency for isolated objects
- worse resolution for jets and missing $p_T$

# Resolving vertices in time




Proton bunch structure
⟹ RMS time spread of vertices ~180-200 ps,
~uncorrelated with spatial distribution

If vertex time resolved at 30-40 ps level
⟹ residual pileup back at $\mu$ = 40-60




Simulations show significant reduction in pileup contribution to primary vertex when time information is added

# A MIP Timing Detector for CMS

MTD concept: thin timing layer outside tracking volume

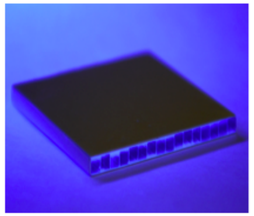
- Barrel (BTL): scintillating crystals (LYSO) + SiPM readout
- Endcaps (ETL): silicon detectors with gain layer (LGAD)

Required time resolution: 30-40 ps initially, degrading with radiation damage to 50-60 ps

Technical Design Report recently approved [CMS-TDR-020]

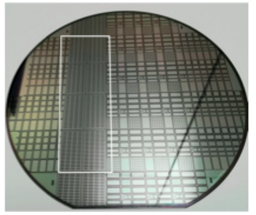
**BTL: LYSO bars + SiPM readout:**

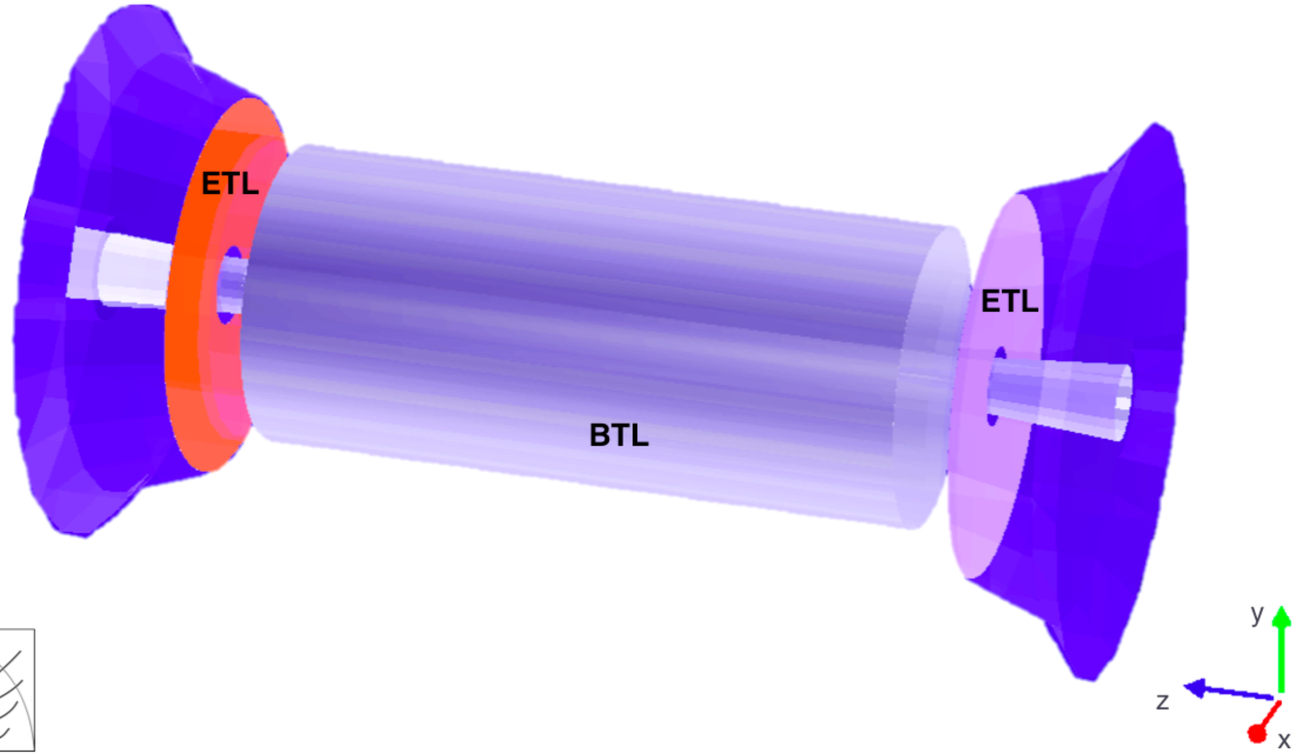
- TK / ECAL interface: $|\eta| < 1.45$
- Inner radius: 1148 mm (40 mm thick)
- Length: ±2.6 m along z
- Surface ~38 $m^2$; 332k channels
- Fluence at 4 $ab^{-1}$: $2x10^{14}$ $n_{eq}/cm^2$



**ETL: Si with internal gain (LGAD):**

- On the CE nose: $1.6 < |\eta| < 3.0$
- Radius: 315 < R < 1200 mm
- Position in z: ±3.0 m (45 mm thick)
- Surface ~14 $m^2$; ~8.5M channels
- Fluence at 4 $ab^{-1}$: up to $2x10^{15}$ $n_{eq}/cm^2$





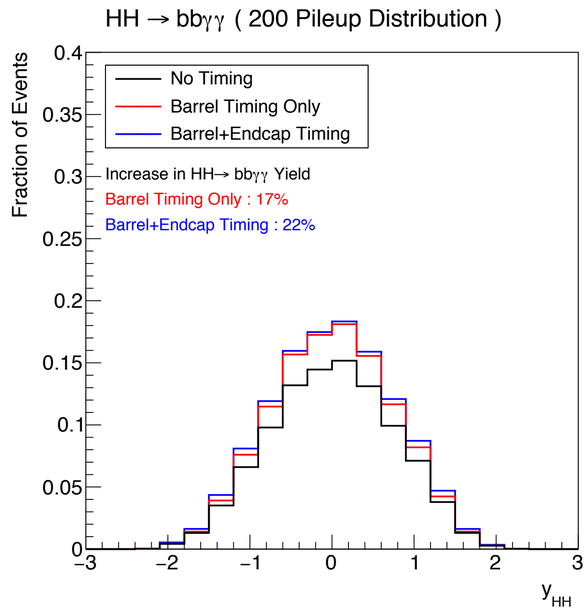

A vertex detector (in time domain) at 3 m from the interaction point!

# Impact on reconstruction

Several areas benefit from improved reconstruction efficiency and $p_T$ resolution:

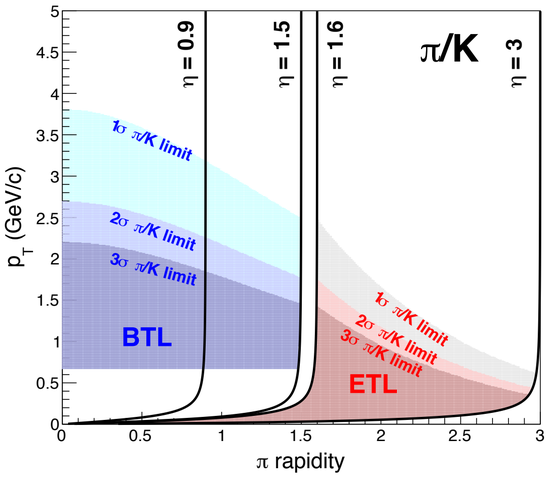
- b tagging;
- $p_T^{miss}$ resolution;
- multi-lepton signatures

Overall, performance comparable to Phase-1 CMS detector at current LHC conditions

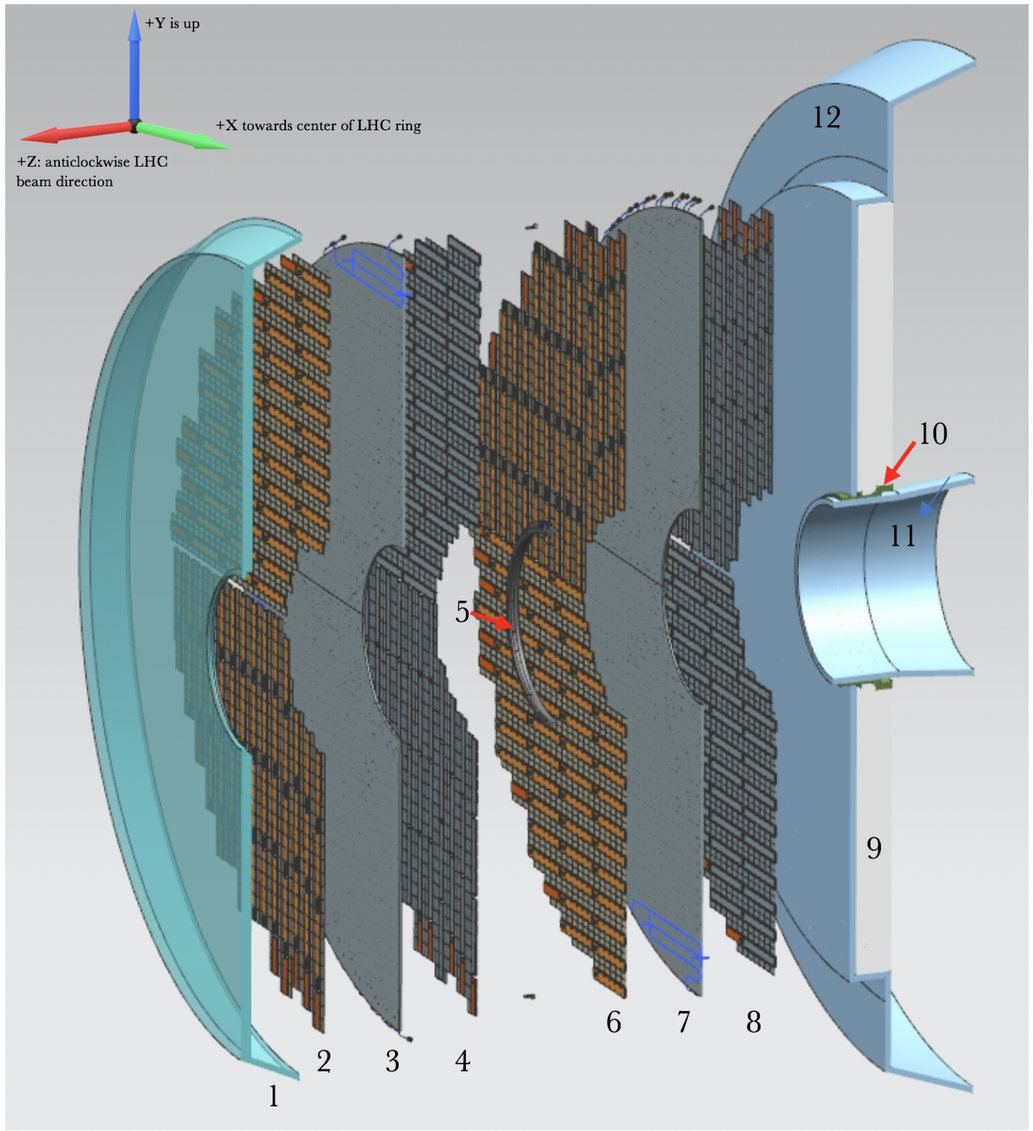



Enhanced capabilities:

- charged particle ID (time of flight) up to $p_T$ ~ few GeV;
- timing of secondary vertices $\Longrightarrow \beta$ of long lived particles



# The Endcap Timing Layer




1: ETL Thermal Screen
2: Disk 1, Face 1
3: Disk 1 Support Plate
4: Disk 1, Face 2
5: ETL Mounting Bracket
6: Disk 2, Face 1
7: Disk 2 Support Plate
8: Disk 2, Face 2
9: HGCal Neutron Moderator
10: ETL Support Cone
11: Support cone insulation
12: HGCal Thermal Screen

Two disks of LGAD sensors per side

- two measurements needed for target time resolution
- double-sided sensor layers for large geometrical acceptance (85%/disk)

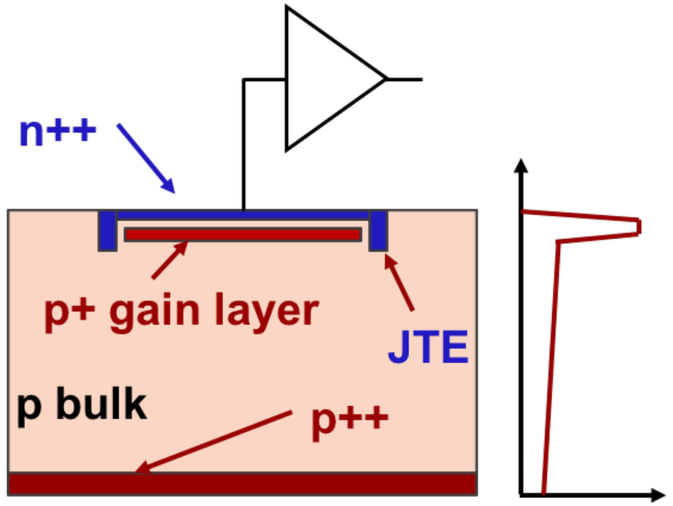
Coverage: $315 < r < 1200$ mm $\Longrightarrow$ $1.6 < |\eta| < 3.0$

- 7.9 m$^2$ total sensor area per side

For $\mathscr{L}_{\text{int}} = 3000$ fb$^{-1}$, expected fluence ranges from $1.5 \times 10^{14}$ $n_{eq}$/cm$^2$ to $1.6 \times 10^{15}$ $n_{eq}$/cm$^2$ at high $|\eta|$

Designed to be removable in case of needed maintenance/repairs during technical stops

# Silicon sensors




Ultra Fast Silicon Detector  E field

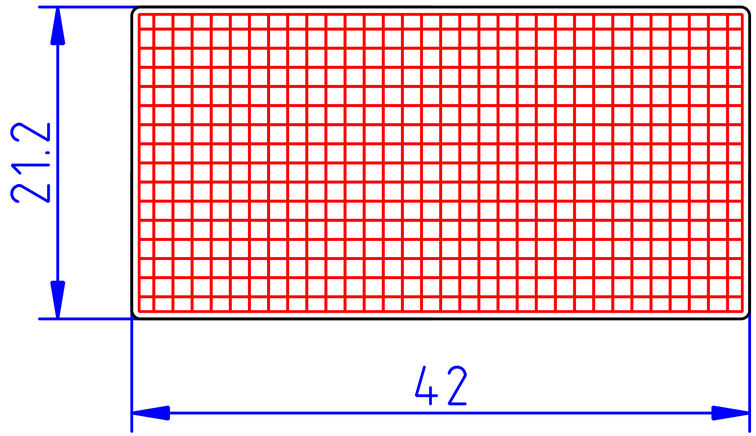
Ultra-Fast Silicon Detectors (UFSD): planar silicon sensors based on Low-Gain Avalanche Detector (LGAD) technology

- charge multiplication for $E \gtrsim 300$ kV/cm
- gain layer through p-type implant
- signal gain: ~10-30
- Junction Termination Extension (JTE) to avoid breakdown
- vendors: CNM, FBK, HBK

Sensor requirements:

- small pad capacitance ⟹ pad size ~few mm$^2$;
- large production yield ⟹ limited size sensors

⟹ ETL sensor
- size: 21.2 × 42 mm$^2$
- pads: 1.3 × 1.3 mm$^2$ (16 × 32 array)



# Radiation hardness

Radiation damage on silicon sensors:

- decrease in charge collection efficiency;
- increase in leakage current;

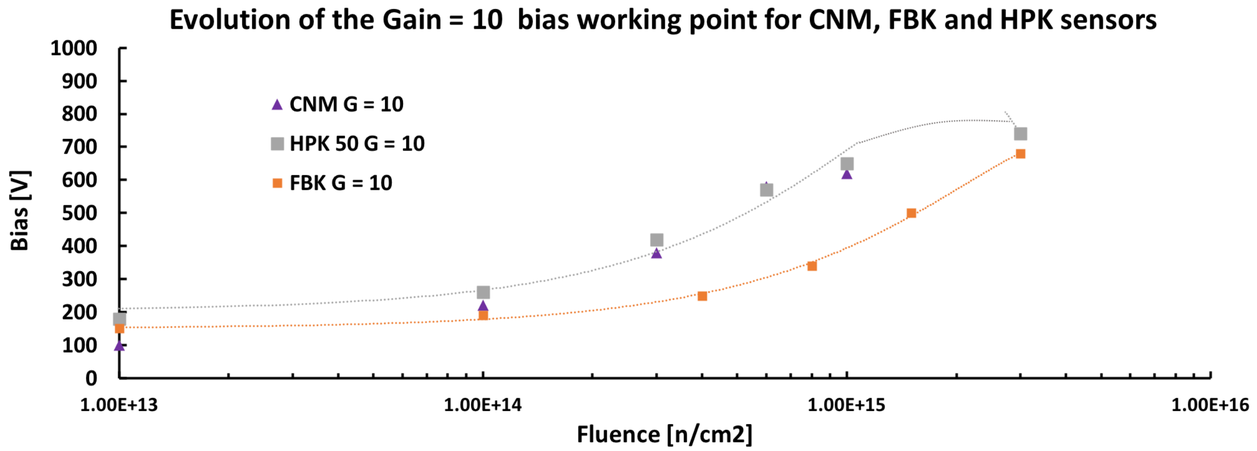
} ⟹ thin sensor: 50 μm active thickness

- change of doping profile

Several irradiation campaigns conducted

Different doping profiles and ion implants tested in gain layer

- a moderate level of carbon implant is beneficial in slowing down removal of initial acceptors




The loss in gain for radiation damage is compensated by gradually increasing the bias voltage

- ⟹ very different bias evolution in time for low $|\eta|$ and high $|\eta|$ regions

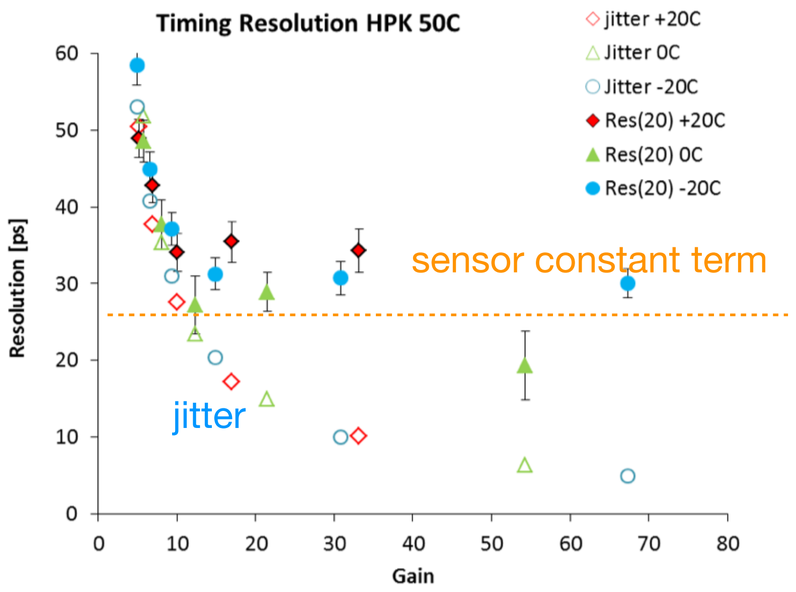
# Time resolution

Main contributions to time resolution in UFSD:

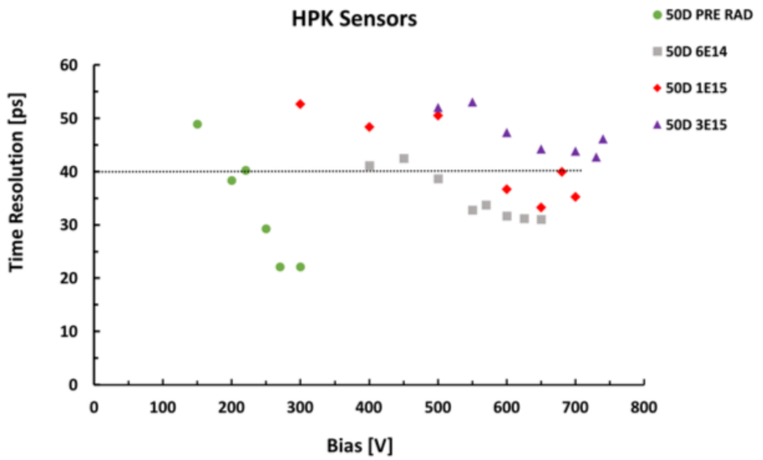
- jitter ($\sigma_{jitter}$) from readout electronics: decreases for higher gain
- Landau noise ($\sigma_{Landau}$) from non-uniformity in ionisation process: ~constant with gain

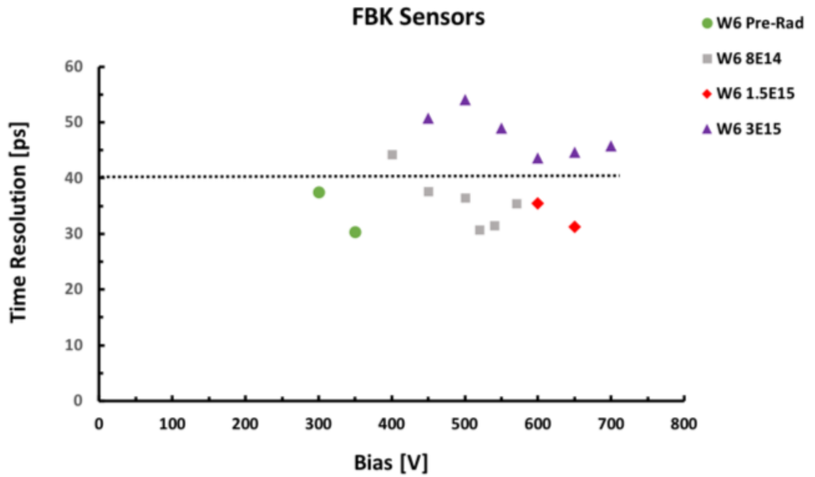
Shot noise due to leakage current is kept low by operating sensors at low *T* (~–30° C)

Timing performance evaluated with dedicated very low noise electronics



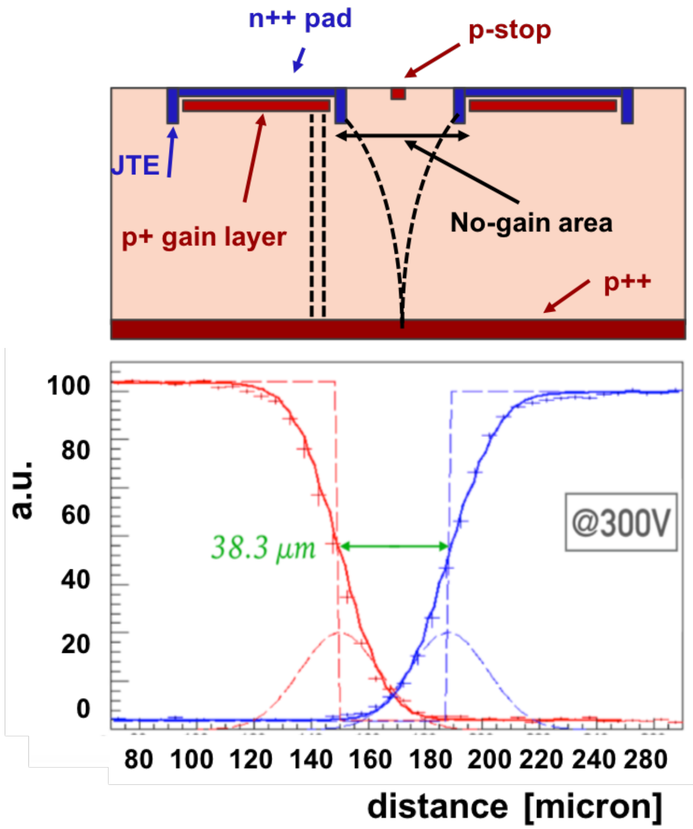

Rept.Prog.Phys. 81 (2018) 2, 026101




Sensor time resolution of 30-40 ps can be achieved up to $1.5 \times 10^{15}$ $n_{eq}/cm^2$

# Fill factor and efficiency




Because of JTE, a no-gain area is present between pads

- Measured with laser test bench and on test beam
- Several designs with various interpad distance tested
- No-gain gap of 50 μm achievable

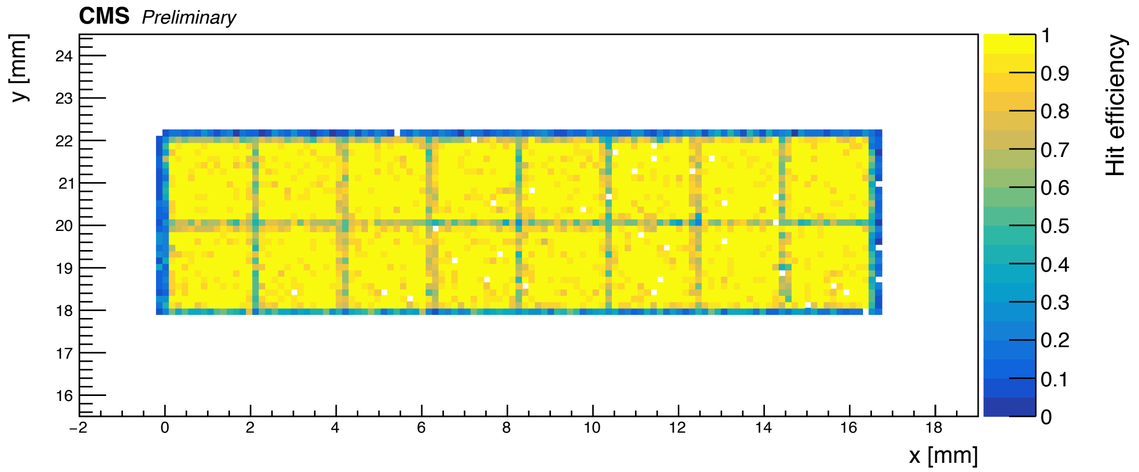
Geometrical inefficiency also at sensor edges

- in current designs, 300-500 μm

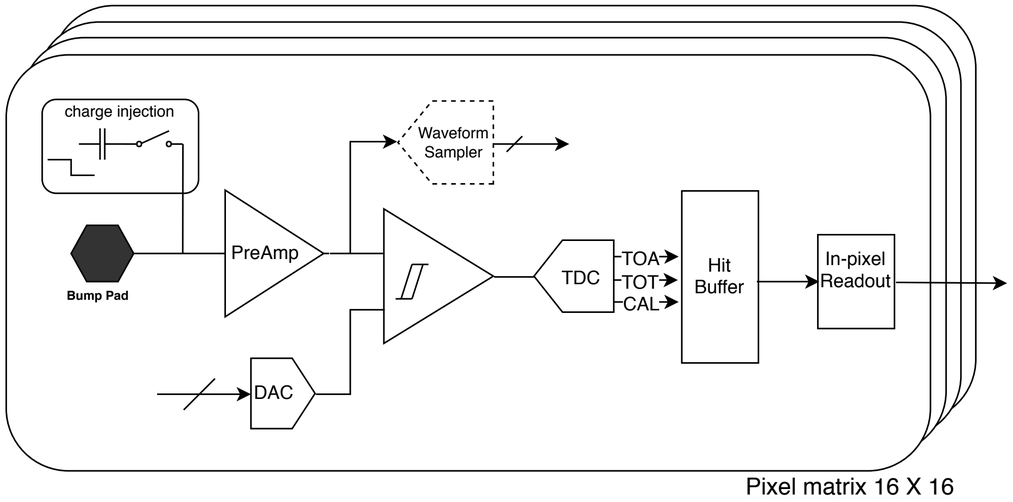
Resulting fill factor: ~90%

Uniform efficiency > 99% observed at test beam

- preserved after 6.4 × $10^{14}$ $n_{eq}/cm^2$ irradiation



# Front-end electronics



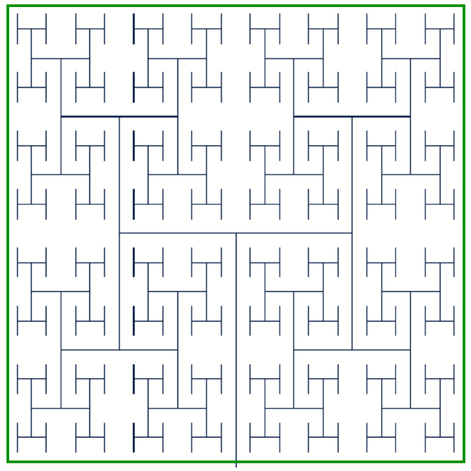

Readout ASIC: ETROC

- 16 × 16 pad array ⟹ 2 chips per sensor (bump-bonded)
- Performs signal pre-amplification, discrimination and time digitisation
- 65 nm technology

Target time resolution (mainly jitter from preamplifier and discriminator): < 40 ps

- ⟹ total time resolution per hit: 50 ps

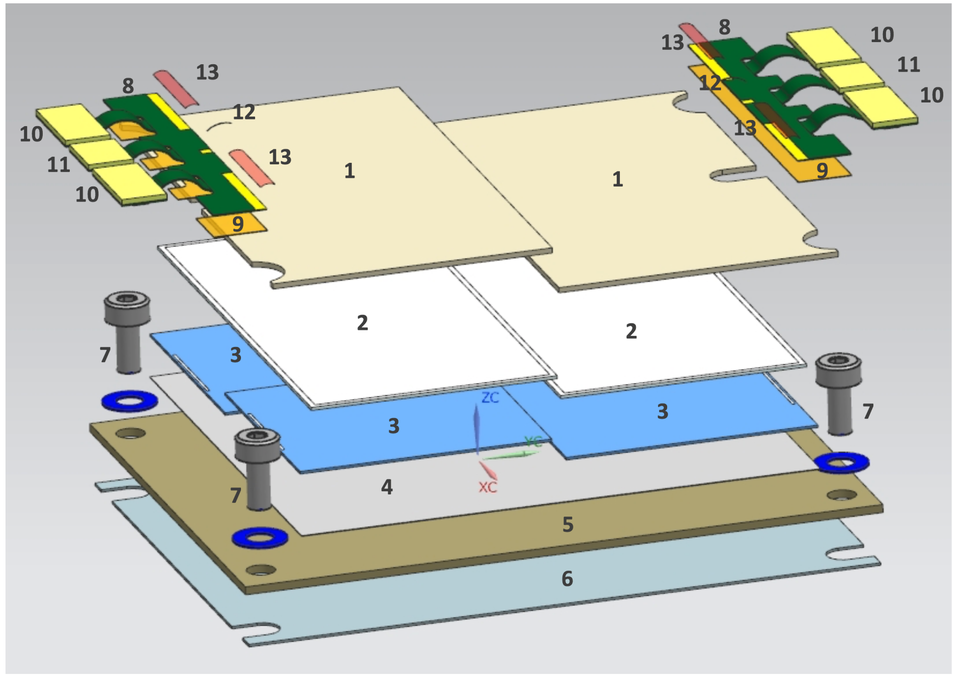
Precision clock distribution network (320 MHz)



Time determination based on fixed threshold with leading-edge + time-over-threshold measurement

Waveform sampling capability on a limited subsample of pads

# ETL modules

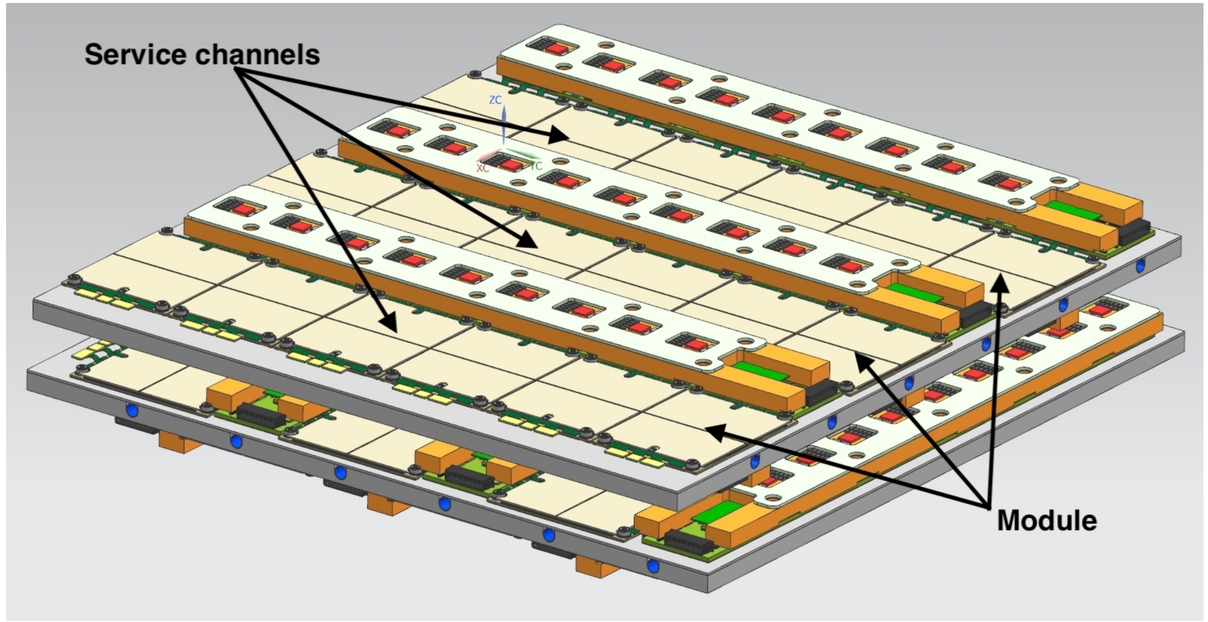



1: AlN module cover
2: LGAD sensor
3: ETL ASIC
4: Mounting film
5: AlN carrier
6: Mounting film
7: Mounting screw
8: Front-end hybrid
9: Adhesive film
10: Readout connector
11: High voltage connector
12: LGAD bias voltage wirebond
13: ETROC wirebonds

"Building blocks" of disks

- Subassembly: sensor + 2 ETROCs
- Two-sensor / one-sensor modules
- AIN baseplate for cooling

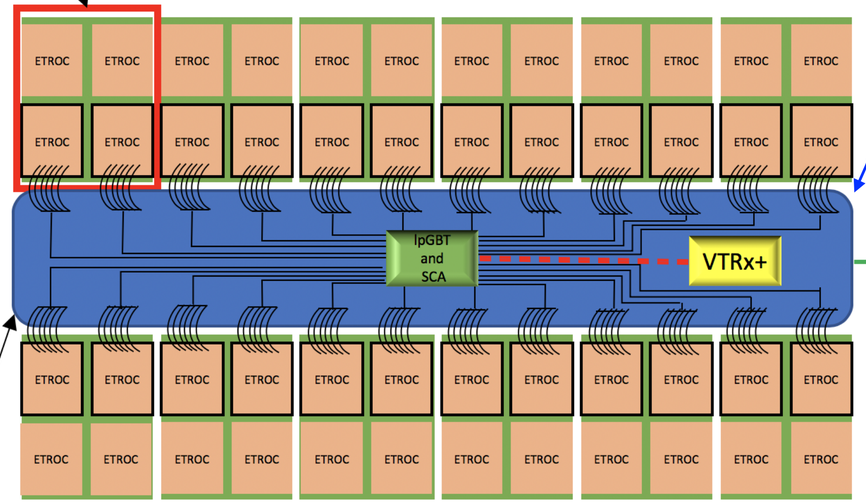
Staggered module and service lines on opposite sides of disk



# Data acquisition

Half size (12 ETROCs) in high occupancy regions

ETL Module: 42x42 mm$^2$
LGAD sensor: 21x42 mm$^2$
ETROC: 21x21 mm$^2$ each




Service Hybrid serving 24 ETROCs
ETROCs read out by this hybrid are outlined in black

Underground Experimental Cavern (UXC)

Underground Service Cavern (USC)

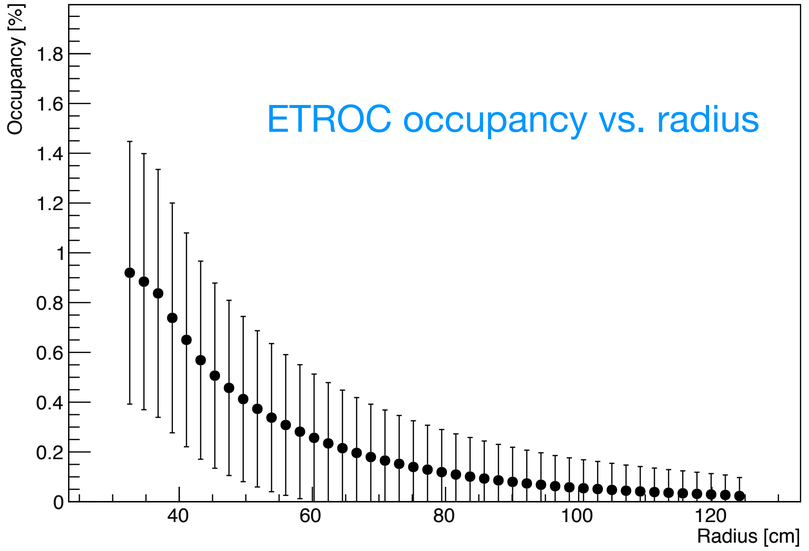
Optical fibers:
LHC clock,
fast controls,
slow controls,
data

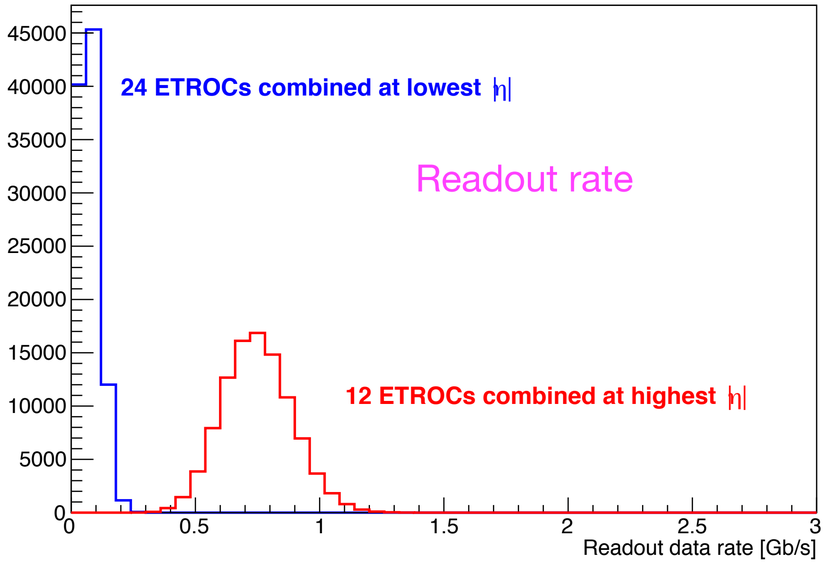
DTH board

DAQ board

bidirectional links

Max L1 trigger latency: 12.8 μs



# Outlook

The MIP Timing Detector is the youngest of CMS detectors proposed for Phase 2

- Technical Design Report just approved

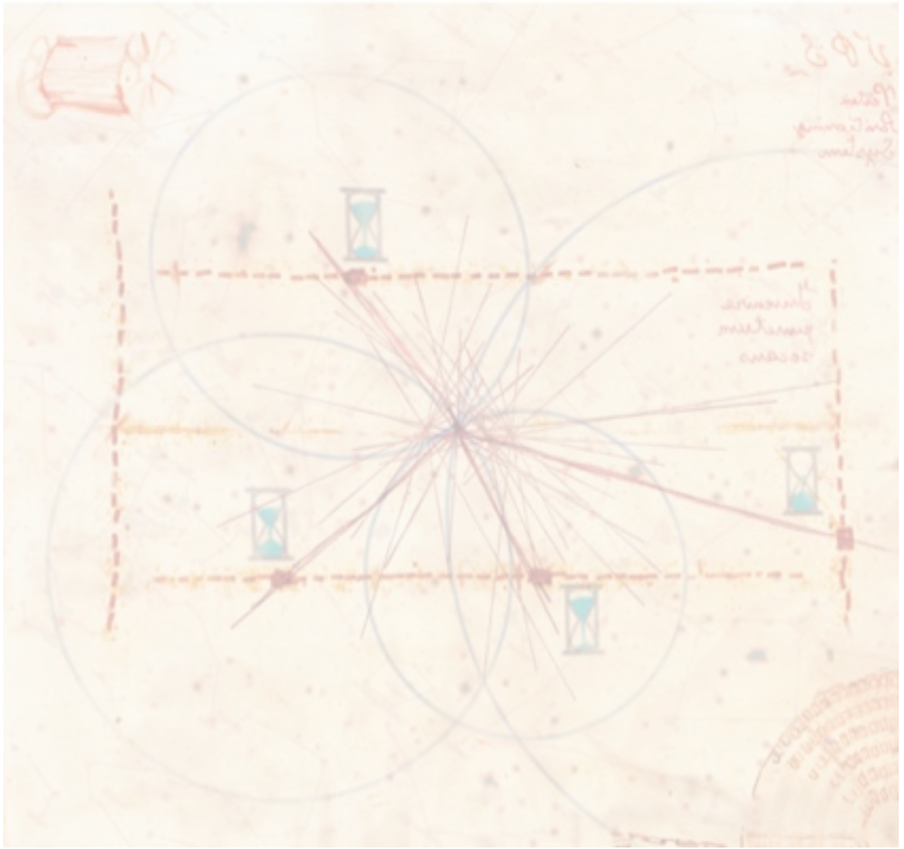
Unprecedented size and scope for a timing detector

- instrumental in overcoming pileup levels at HL-LHC
- ETL is the first large-scale application of UFSD technology

Essential ETL timeline:

- Sensor design choice: Q3 2021
- ETROC final design: Q4 2022
- Start of module assembly: Q4 2023
- Start of module integration: Q2 2024
- Installation in CMS: Q2 2025

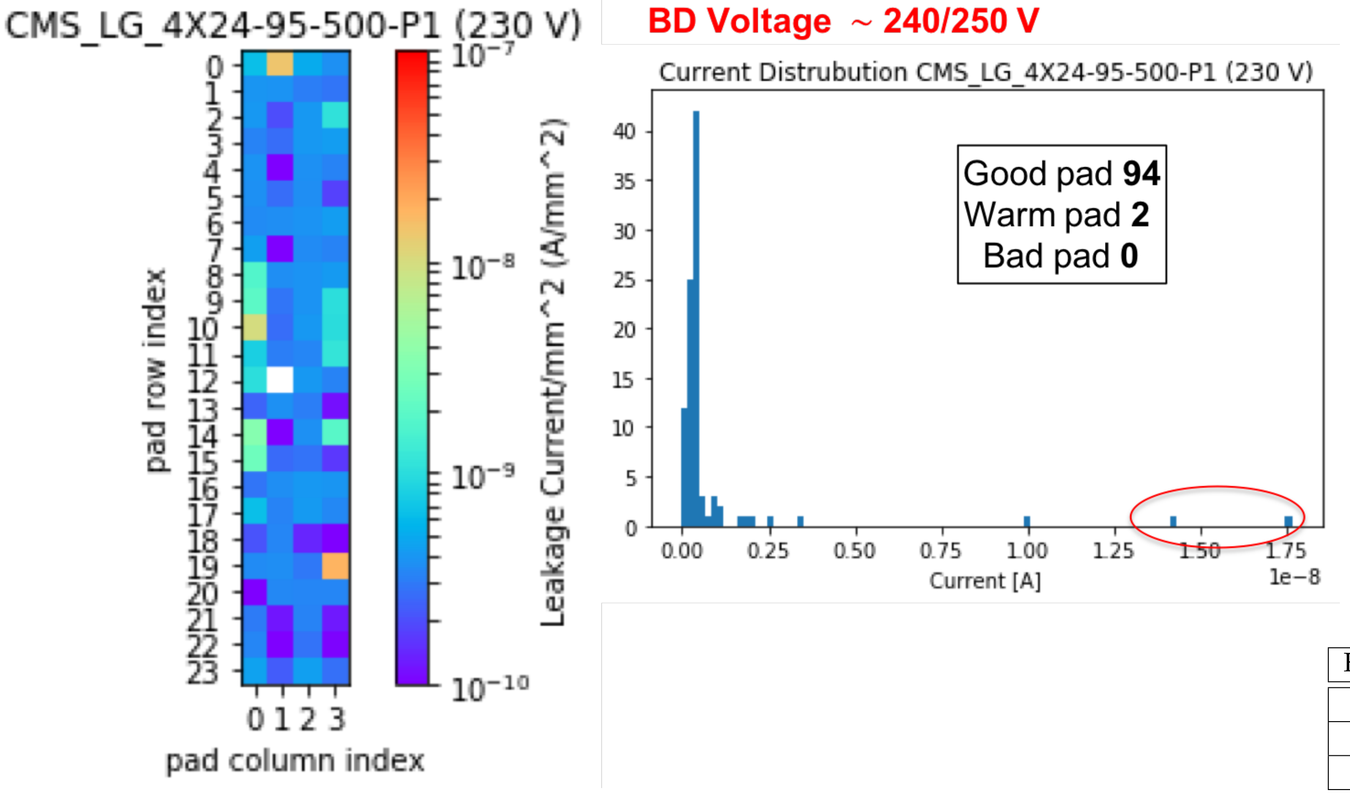
# Additional Material



# Gain uniformity

Gain uniformity indirectly evaluated by measuring leakage current in pads

Leakage current in sensor pads

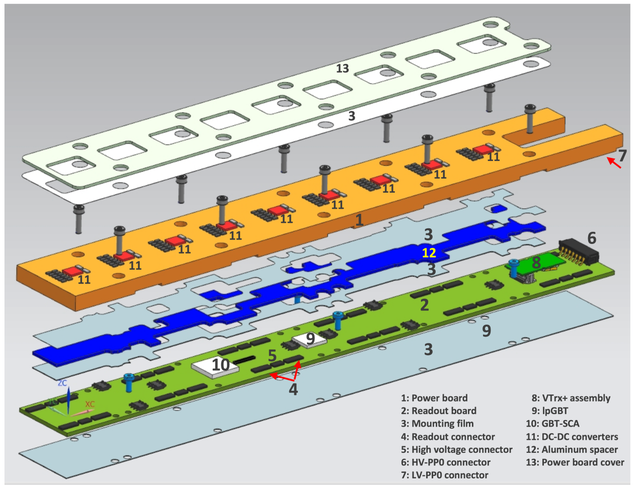


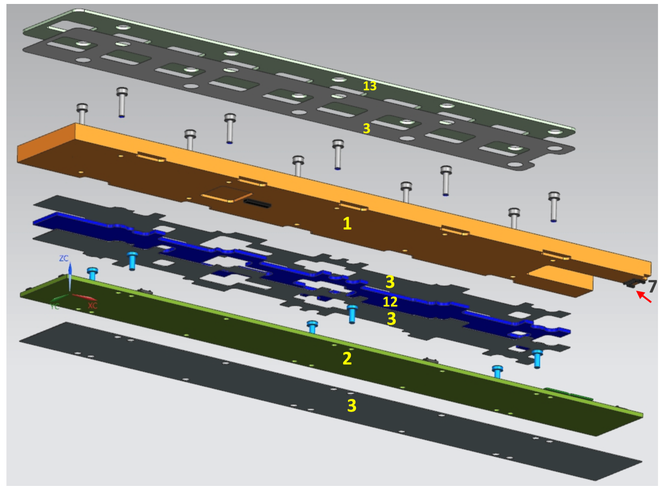

Leakage current in 6” wafer

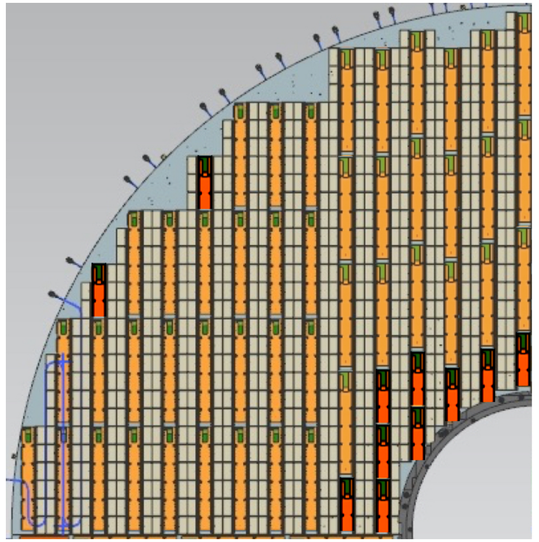
| Foundries | Sensor type | # Sensors tested | # Warm pads | # Bad pads | Comments |
|---|---|---|---|---|---|
| FBK | 4 × 24 pads | 152 | 14 (0.1%) | 0 | bias = 100 V |
| FBK | 5x5 pads | 23 | 4 (0.7%) | 0 | bias = 300 V |
| HPK | 4 × 24 pads | 15 | 20 (1.3%) | 0 | bias = 250 V |

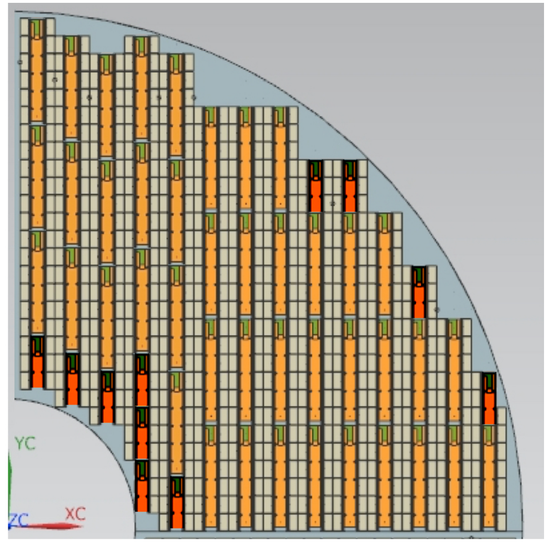
Pads not connected to ground show a decrease in breakdown voltage, which can be significant (up to 250 V). Effect being addressed with vendors.

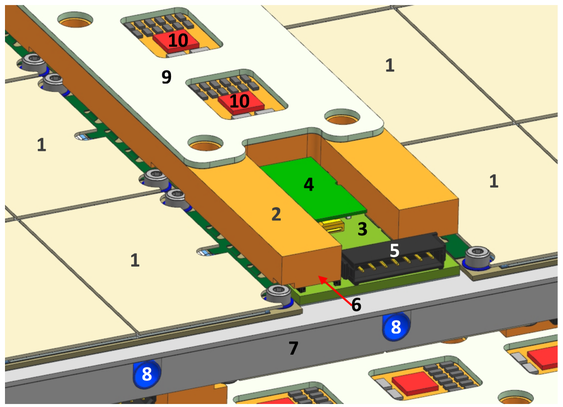
# ETL module layout



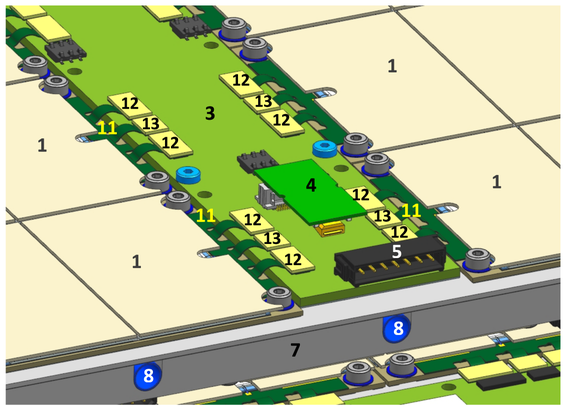



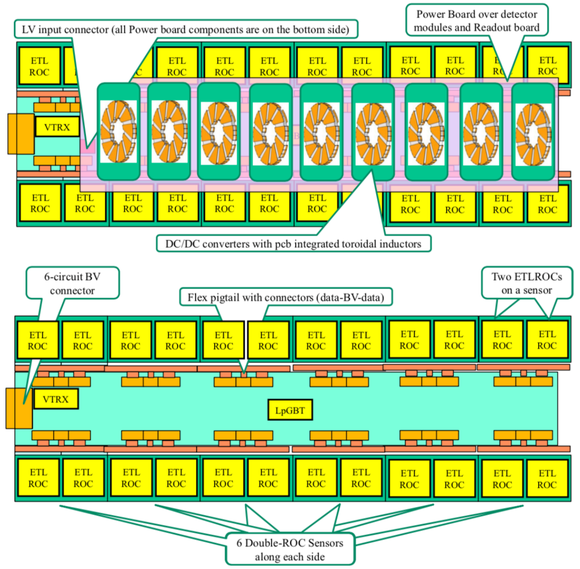




1: AlN module cover
2: Power board
3: Readout board
4: VTRx+
5: HV-PP0 connector
6: LV-PP0 connector
7: Support disk
8: $CO_2$ cooling tube
9: Power board cover
10: DC-DC converters





# Cooling

ETL modules will be cooled by means of two-phase $CO_2$ system

- Distribution through pipes running inside the Al support plate
- Nominal operating point: –35 °C
  (max –25 °C from simulation)