VERTEX 2019

Recent results on 3D Si Sensor and Electronics developments for future Vertex Detectors

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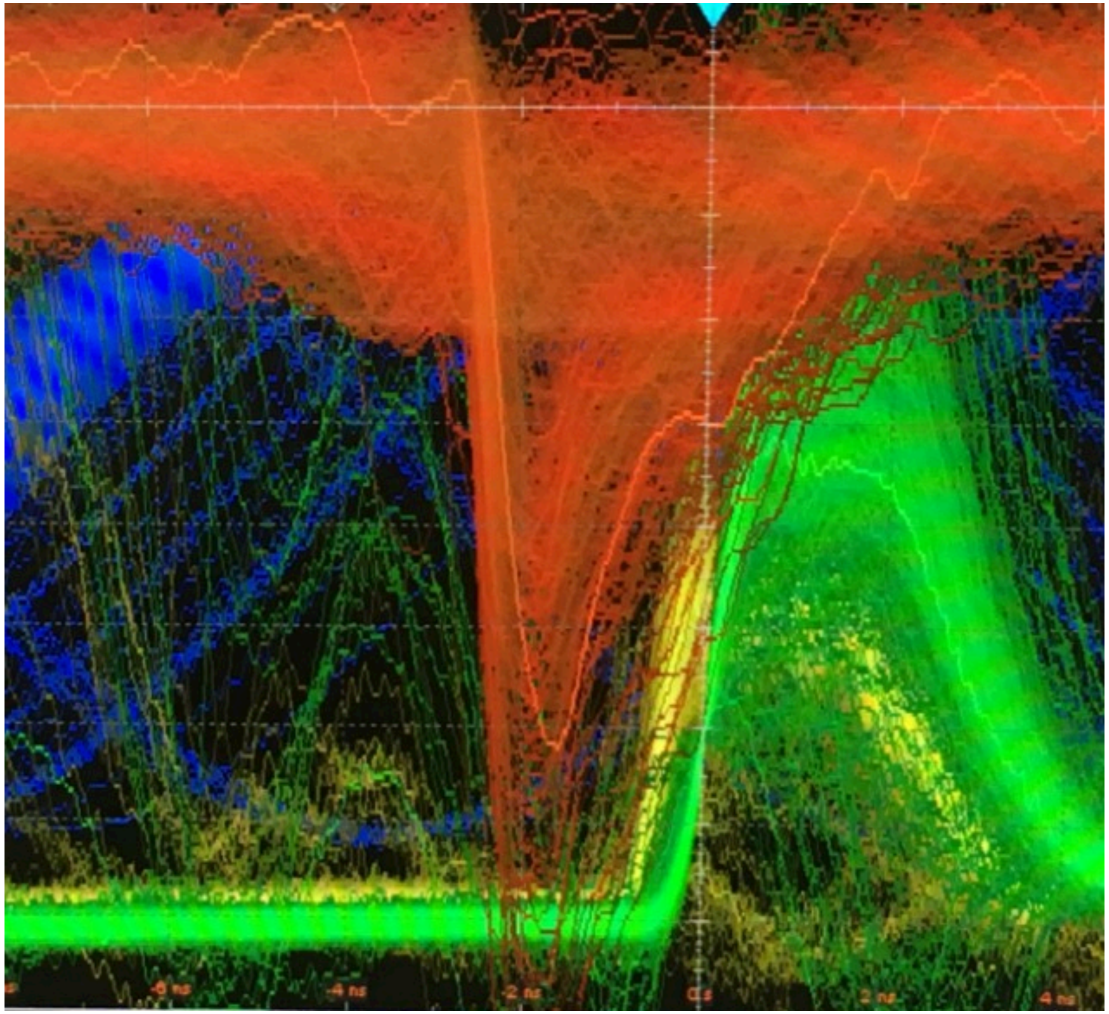
TimeSPOT

TIME and SPace real-time Operating Tracker



Structure, organization and objectives of TimeSPOT

TIME and SPace real-time Operating Tracker

Main target:

Develop and realize a demonstrator consisting of a complete yet simplified tracking system, integrating about 100-1000 read-out channels (pixels), satisfying the following characteristics:

- Space resolution: O (10 μm)
- Radiation hardness: > 10^{16} 1 MeV n_{eq}/ cm^2 (sensors) and > 1 Grad (electronics)
- Time resolution: ≤ 50 ps per pixel (target ≈ 30 ps)
- Real time track reconstruction algorithms and fast read-out (data throughput > 1 TB/s)

Activities are organized in 6 work packages: P.I.: A. Lai Cagliari

1. 3D silicon sensors: development and characterization (GF. Dalla Betta Trento)
2. 3D diamond sensors: development and characterization (S. Sciortino Perugia)
3. Design and test of pixel front-end (V. Liberali Milano)
4. Design and implementation of real-time tracking algorithms (N. Neri Milano)
5. Design and implementation of high speed readout boards (A. Gabrielli Bologna)
6. System integration and tests (A. Cardini Cagliari)

Sezioni INFN: Bologna, Cagliari, Genova, Ferrara, Firenze, Milano (+Bergamo), Padova, Perugia, Torino, TIFPA. ≈ 60 heads, ~ 20 FTE. People from LHCb, ATLAS, CMS + others

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Special Credits
For this talk

TIME and SPace real-time Operating Tracker

Main subject:

Preparation and making of 3D-Si lab and under-beam tests

L. Anderlini, A. Bizzeti, A. Cardini, M. Ferrero, G. Forcolin, M. Garau, A. Lai, A. Lampis, A. Loi, C. Lucarelli, R. Mendicino, S. Minutoli, R. Mulargia, M. Obertino, E. Robutti, S. Vecchi

Some short updates:

28-nm CMOS design

L. Piccolo, A. Rivetti, S. Cadeddu, L. Casu, A. Lai, M. Barbaro, C. Napoli, S. Sonedda, L. Frontini , V. Liberali, A. Stabile, S. Ruhollah Shojaii

In addition, we would like to acknowiedge with great gratitude:

- PSI team for valuable technical support during test beam activities
- Rohde&Schwartz Bern for a 1 week free availability of a 100 k€ 8 GHz BW scope

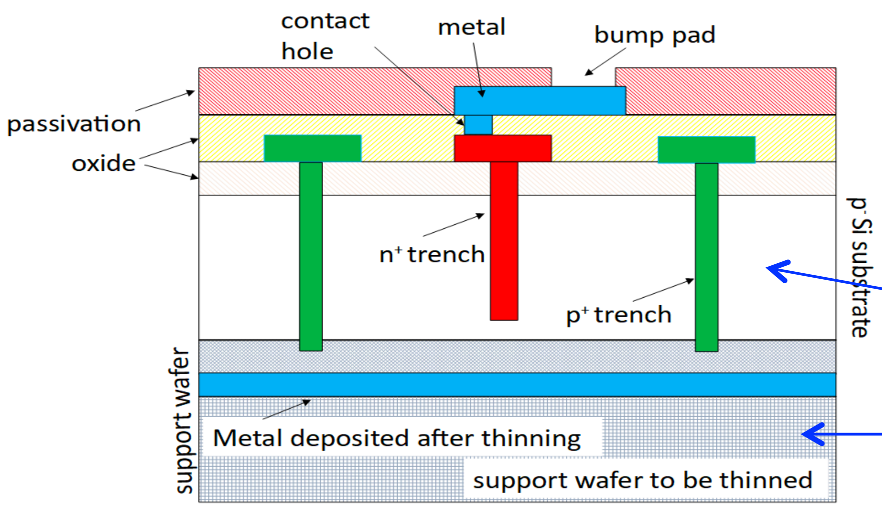
PAUL SCHERRER INSTITUT

3D Trench geometry and Pixel characteristics

Electric field map

Column geometry (e.g. ATLAS IBL)

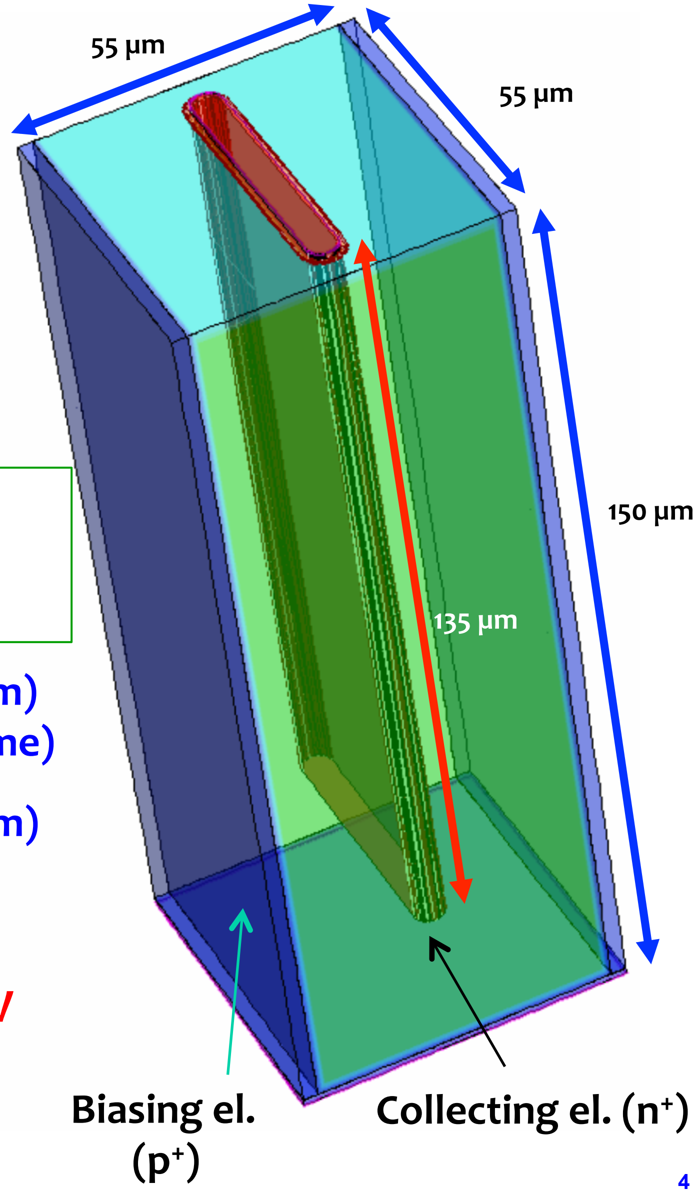
Trench geometry (TIMESPOT)



Single-Side production method

HR Si (~ 5kΩ cm) (sensitive volume)

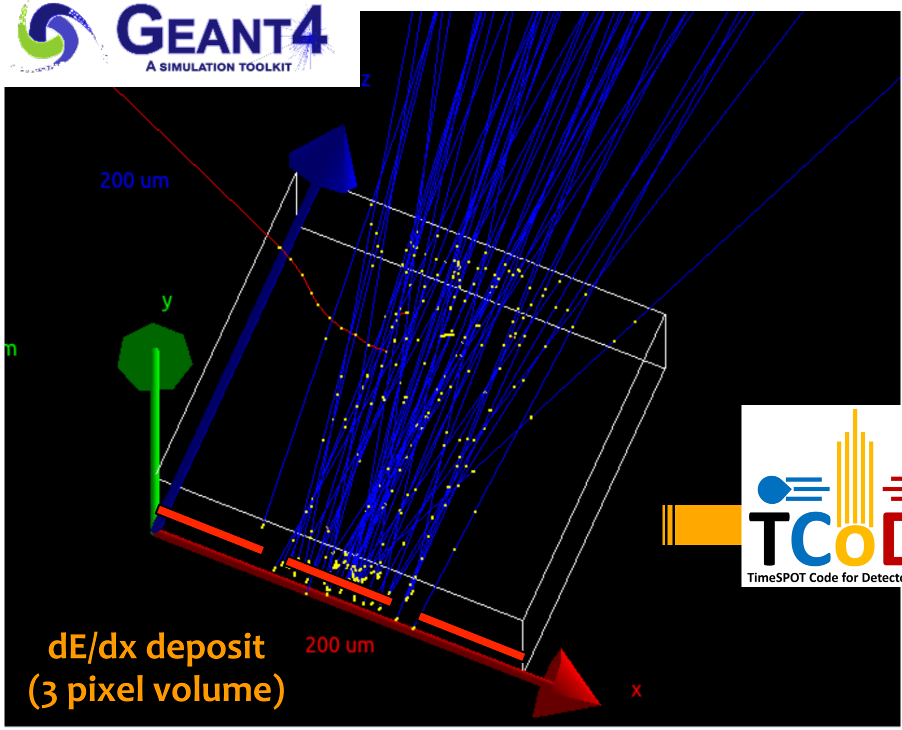
LR Si (<Ω cm)

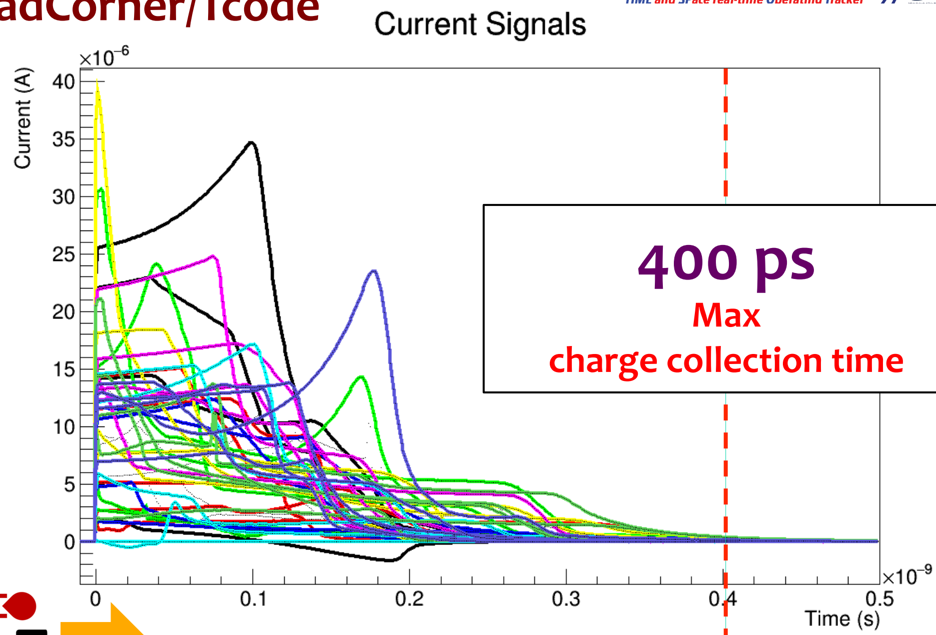


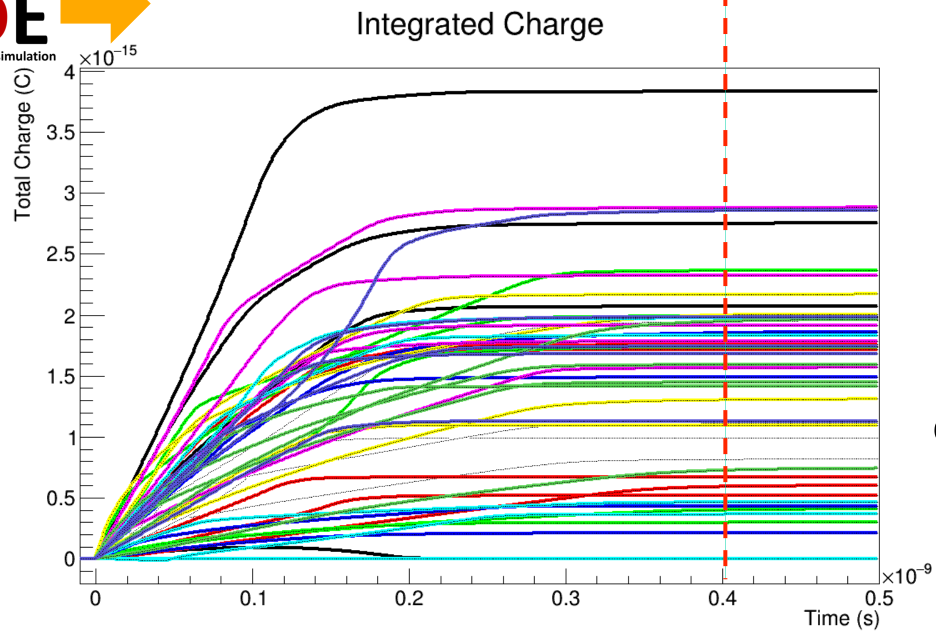
- Total charge deposit for MIP ≈ 2 fC
- Full depletion @ few Volts, Velocity saturation @ > 30 V
- Pixel capacitance (from simulation) ~140 fF
- 55x55 μm²: TIMEPIX family-compatible pitch

Signals: full-3D model. "Statistics"

https://github.com/MultithreadCorner/Tcode







50 tracks

Induced current signals calculated by TCODE

(input to F/E electronics model)

1h40' in ST (Intel®Xeon®CPU X5450 – 10 GB RAM)

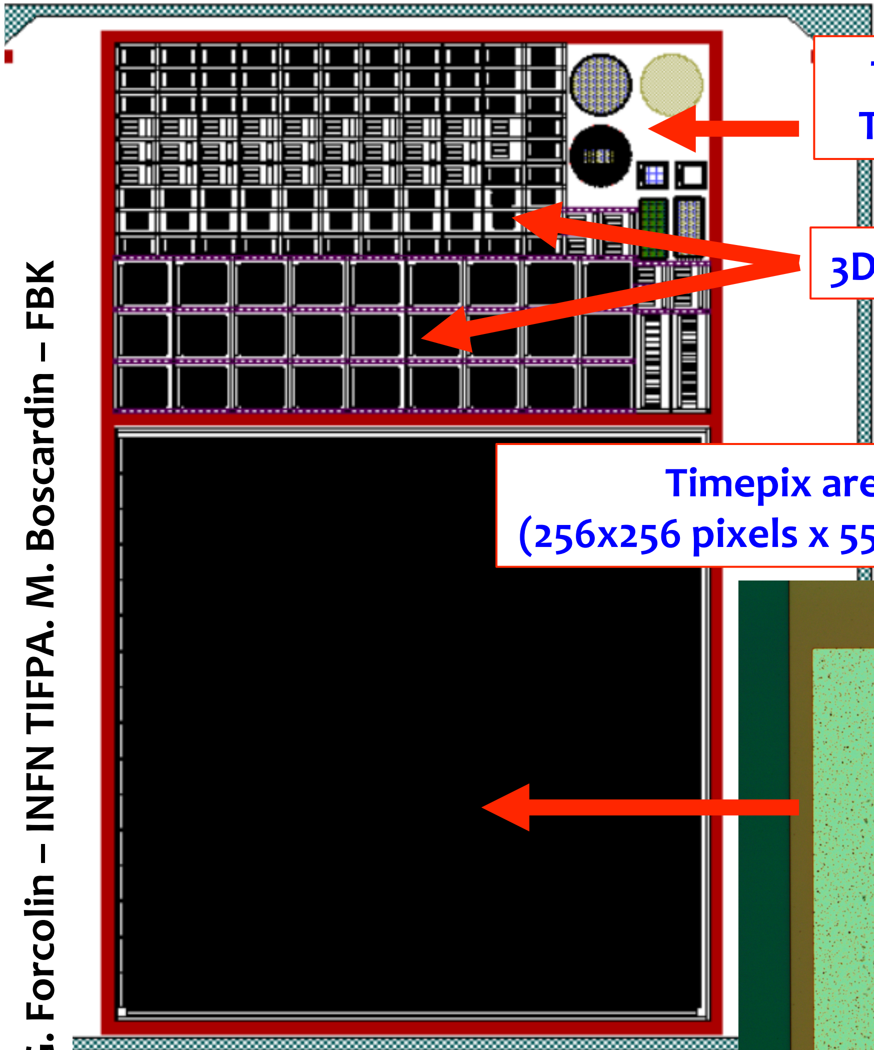
1'40" on a gaming laptop in MT

2-3 months on TCAD (estimate)

A. Contu, A. Loi – INFN Cagliari

1st 3D-trench batch: ~15 June 2019

G. Forcolin – INFN TIFPA. M. Boscardin – FBK

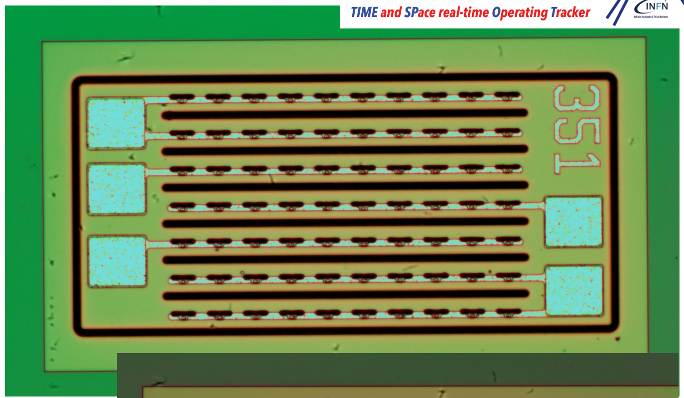


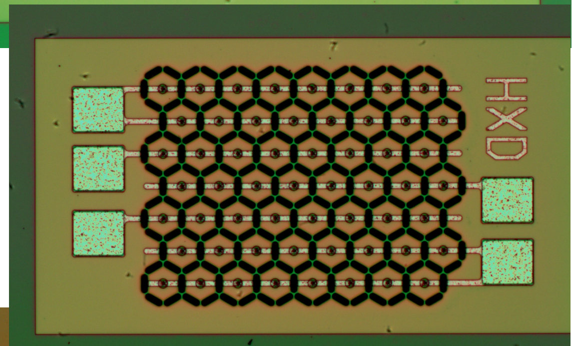
Technological Test Structures

3D Test Structures

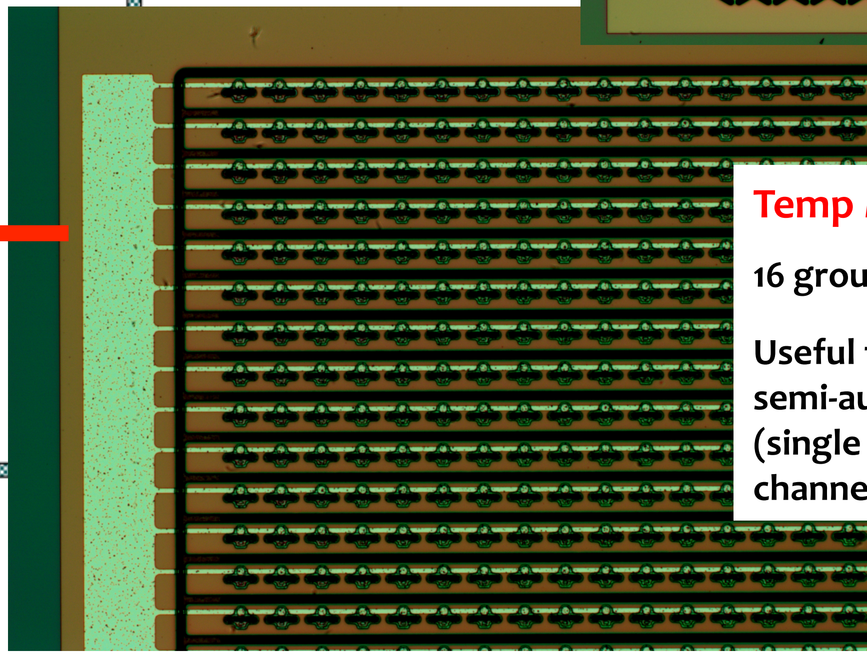
Timepix area (256x256 pixels x 55 μm pitch)

11 of such structures x 10 wafers





Diodes, Strips …

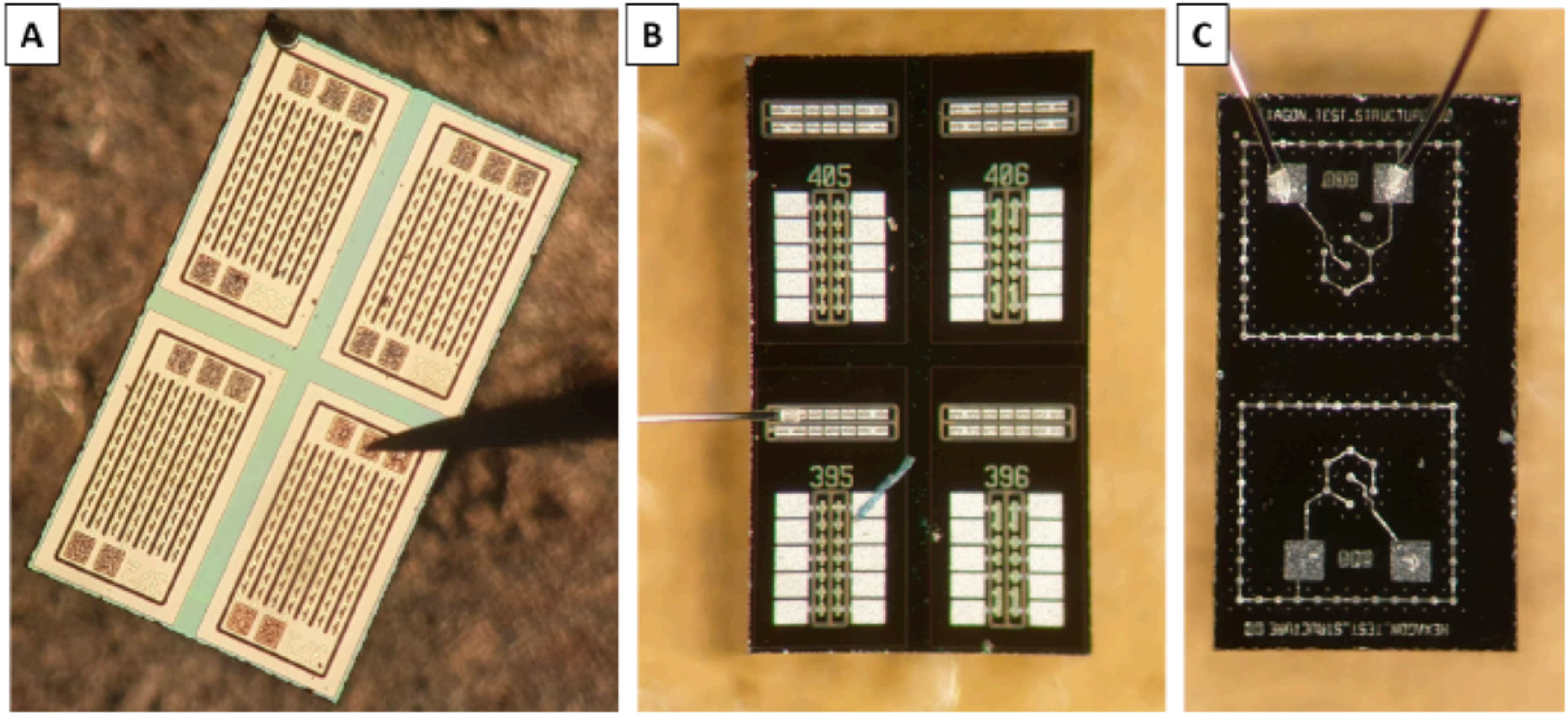


Temp Metal:

16 groups of 16 rows each

Useful for automatic and semi-automatic I-V tests (single probe for several channels)

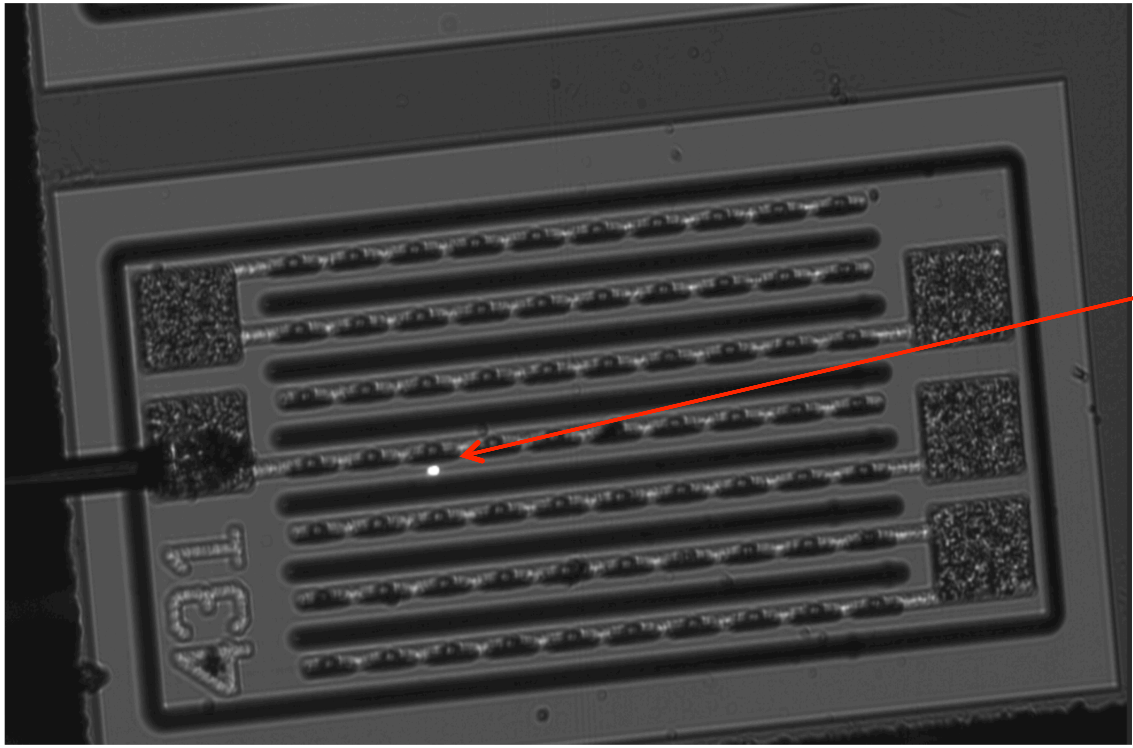
3D structures under test
In lab & under-beam measurements



(A) Pixel-strip (10 pixels connected on the same read-out pad); **(B)** Single and double pixel; **(C)** Hexagonal (column) pixel device, based on FBK 3D Double Side Technology.
Devices are connected to electronics by wire bonding (Al, 25 μm diameter, ~ 5 mm length)

TCT on test structures

Measurements on 1st batch in laboratory



Pixel strip device: 10 pixels connected on the same read-out pad.
Total capacitance ≈ 1.5 pF + bonding

Test setup:

1030 nm pulsed LASER
200 fs native jitter
8 ps on scope ("setup" jitter)
Repetition rate from single pulse to 40 MHz

Cylindical spot 5 μm diameter
MIP-like deposit shape

MIP (~2 fC) deposit amount estimated by means of Charge amplifier, adjustable by optical filtering

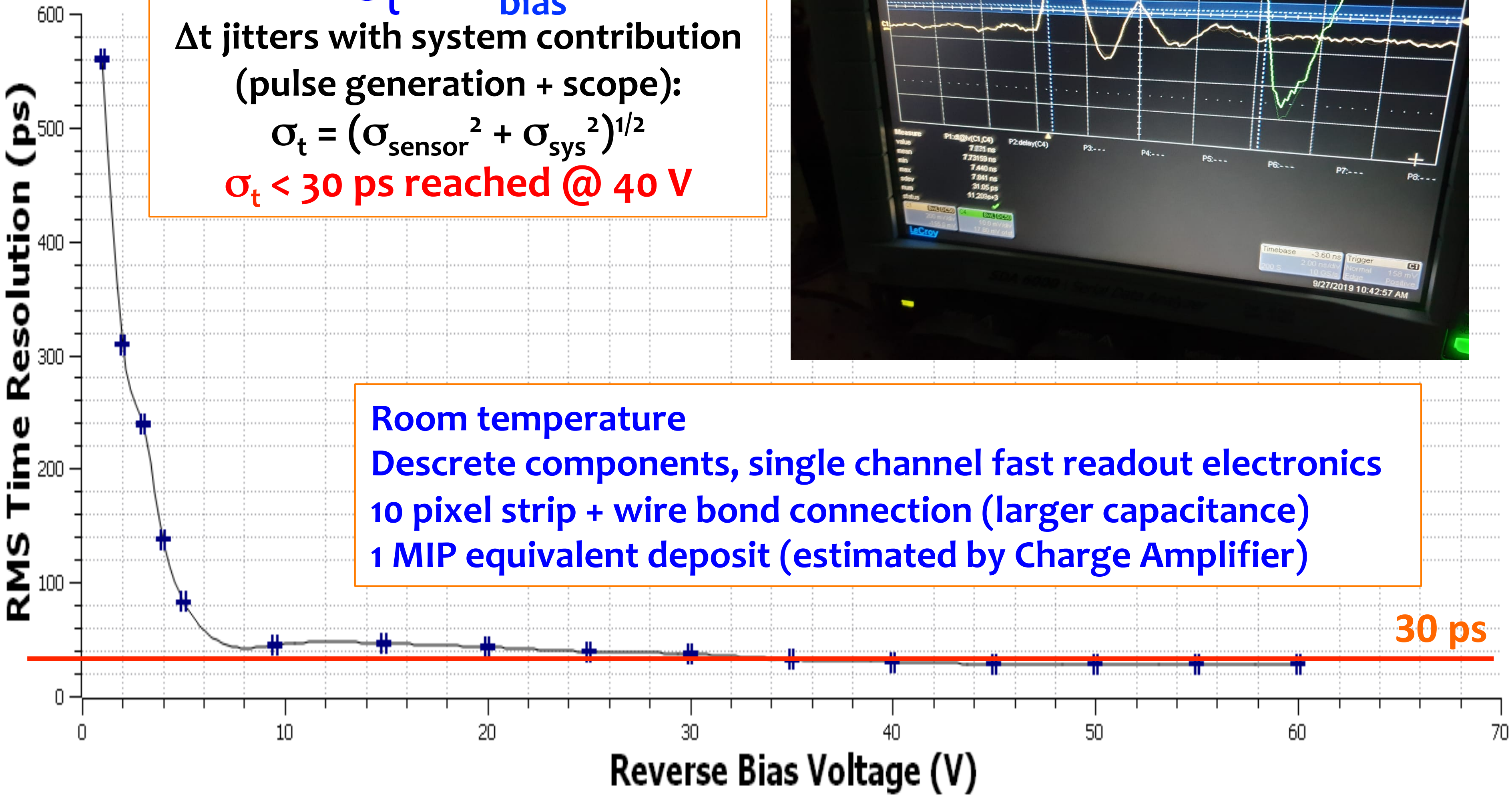
TCT: Time response vs V_{bias}

σ_t vs V_{bias}

Δt jitters with system contribution (pulse generation + scope):

$\sigma_t = (\sigma_{sensor}^2 + \sigma_{sys}^2)^{1/2}$

σ_t < 30 ps reached @ 40 V



Room temperature

Descrete components, single channel fast readout electronics

10 pixel strip + wire bond connection (larger capacitance)

1 MIP equivalent deposit (estimated by Charge Amplifier)

TCT: Time response vs charge deposit (signal amplitude)

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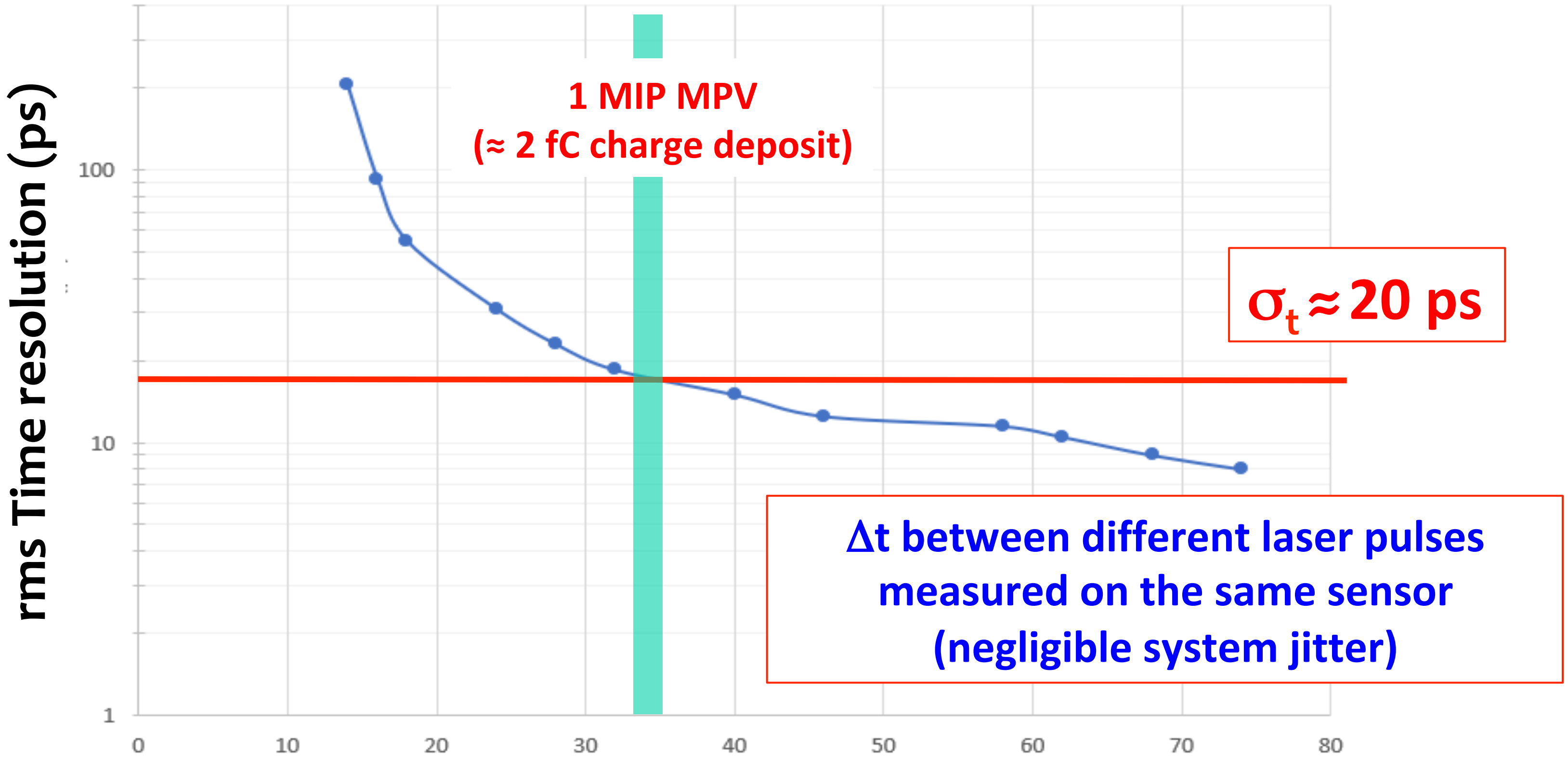
Pixel Strip @ V_{bias} = – 60 V

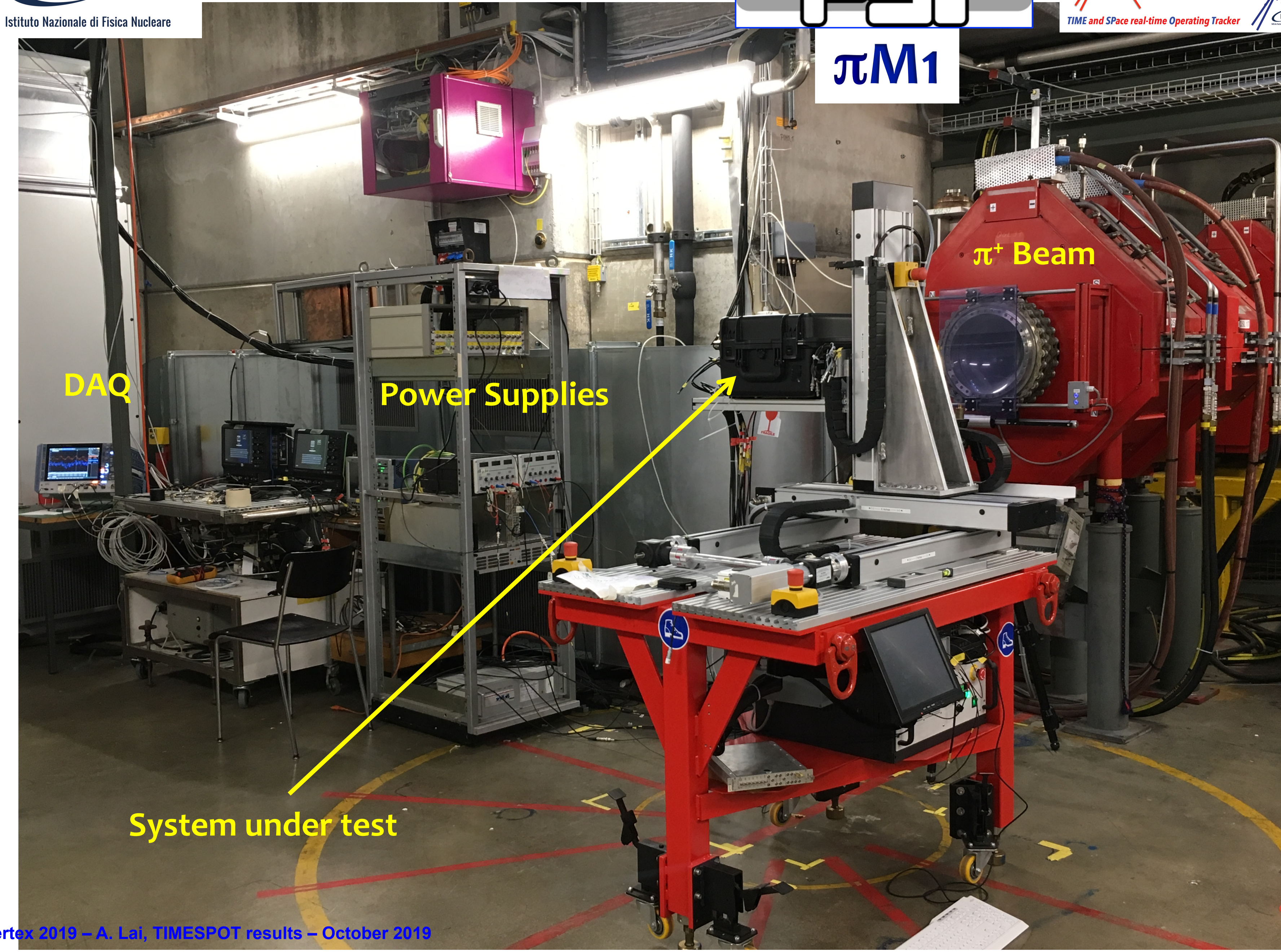


Amplitude (mV)

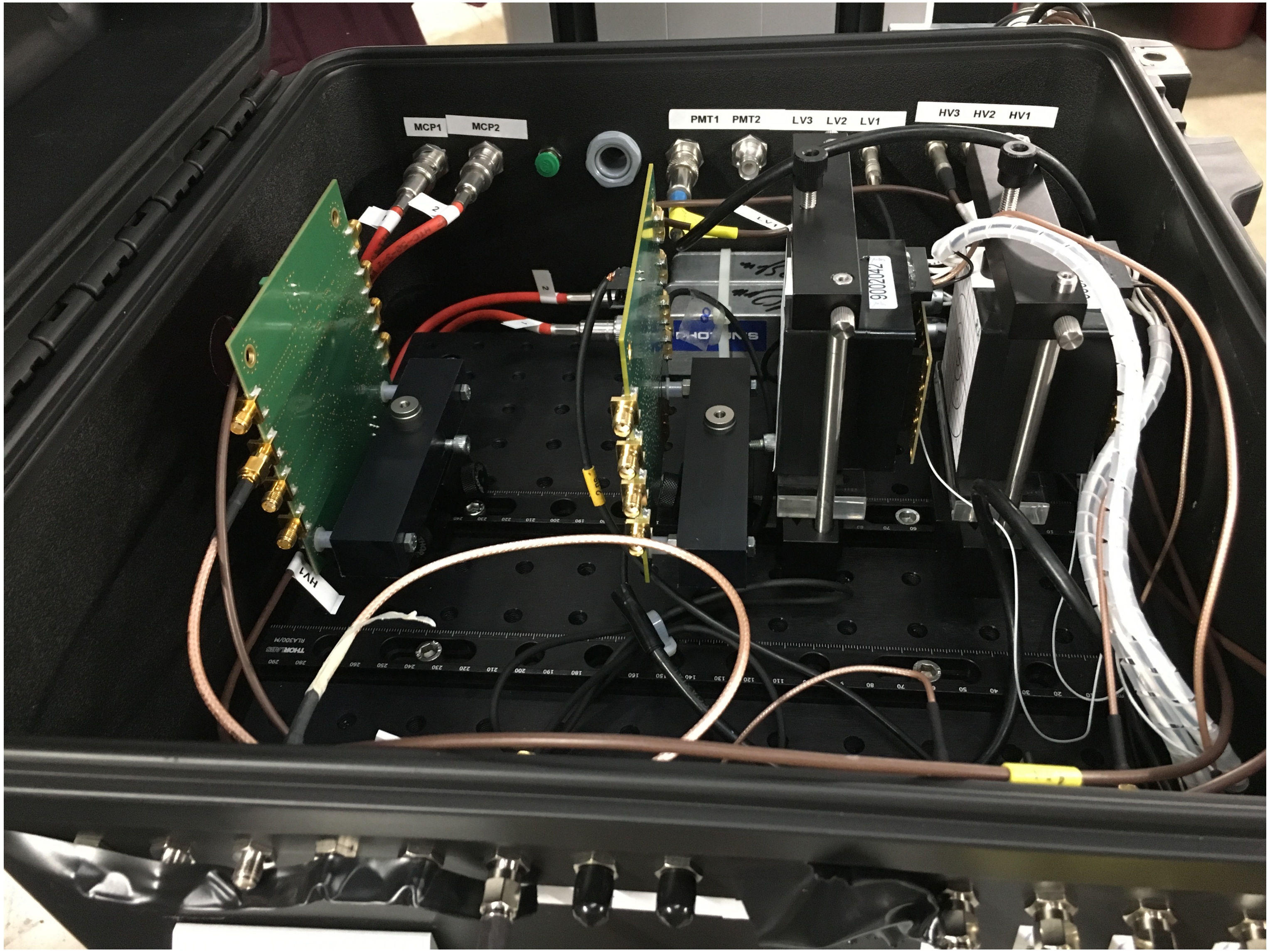
Room temperature.
Descrete components, single channel fast readout electronics
Digital CFD (on scope)
10 pixel strip + wire bond connection (total capacitance ≈ 1.5 pF)

Tests beam @ PAUL SCHERRER INSTITUT PSI

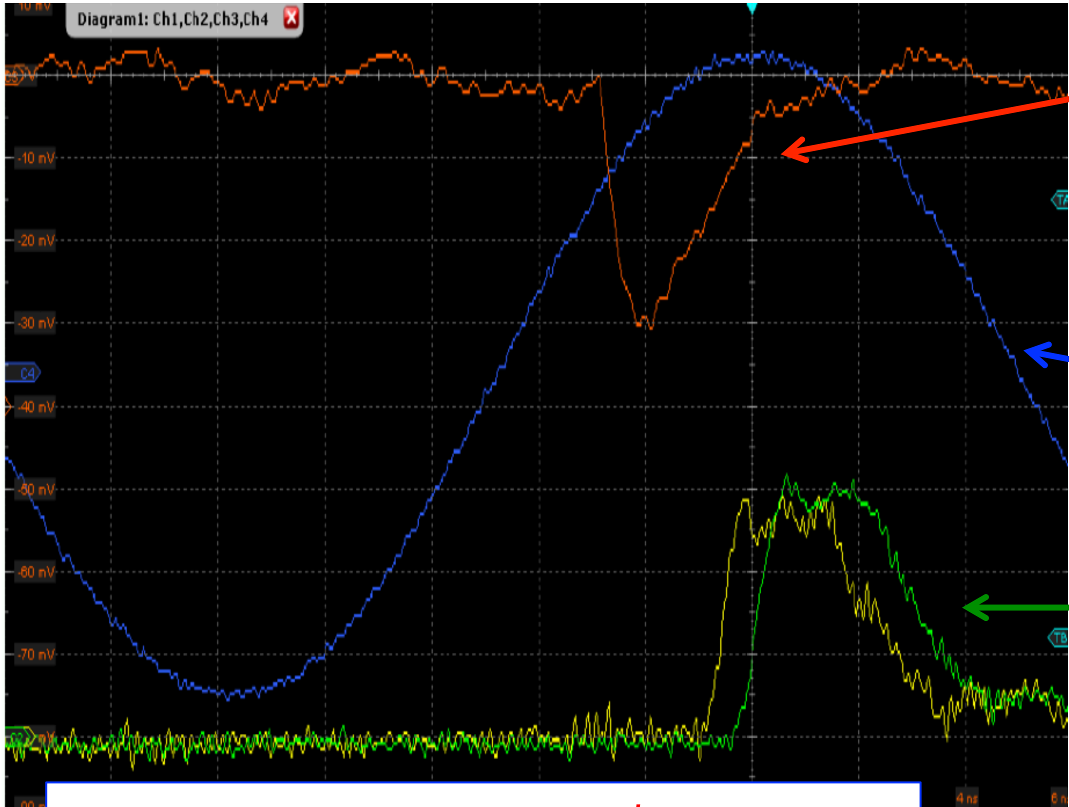
πM1



Tests beam @ PSI πM1
System inside the black box



Tests beam @ PSI πM1
Experimental conditions



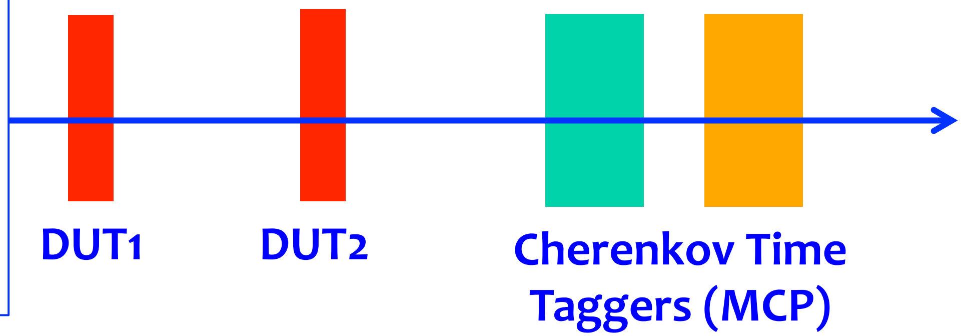
DUT signal (trigger)
Exposed Area of DUTs
<< 1 mm^2
Each DUT has a different DAQ chain
(8 GHz and 4 GHz BW scopes)

Beam RF signal
(50 MHz)

2 MCP signals
(time references)
Exposed area ≈ 5x5 cm^2

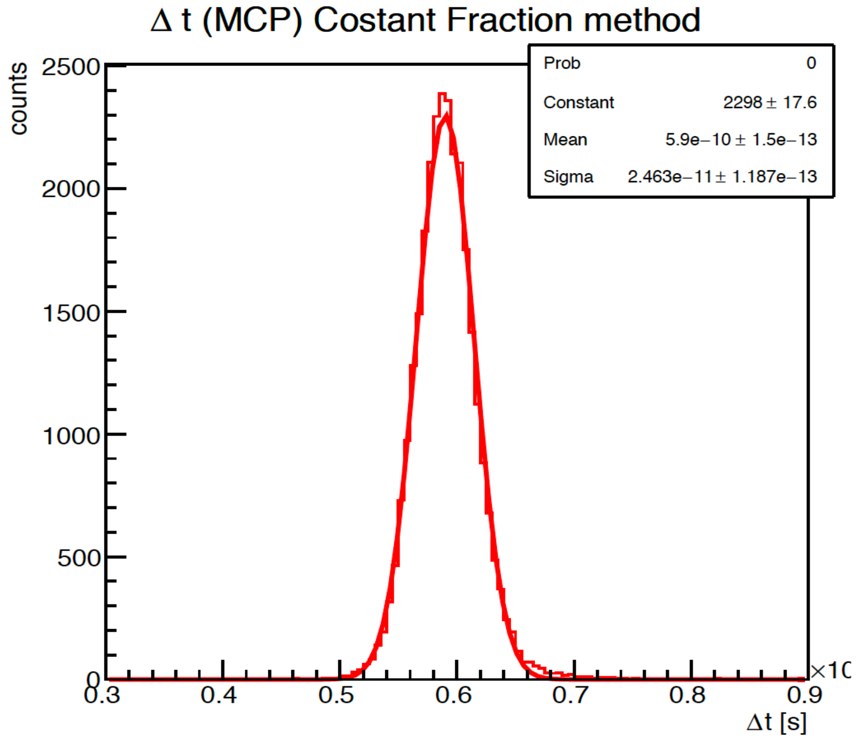
Beam E = 270 MeV/c.
Beam radius on the spot $\sigma \sim 1.5$ cm

Original beam: p, e$^+$, μ^+, π^+ Selectable by TOF
Using a plexiglas degrader and small slit apertures we obtained an almost pure π^+ beam (negligible e+ contamination)



Measurement conditions and Method

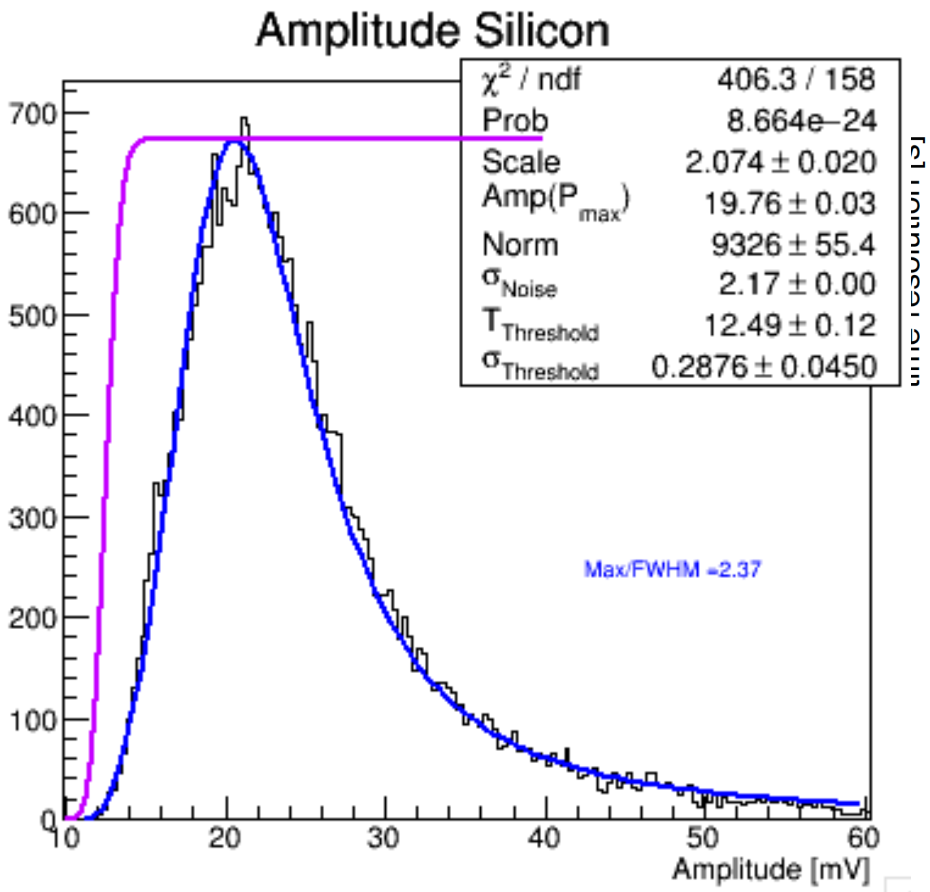
Test structure	Front-end
Pixel strip	KU modified prod. 1 – unshielded
Single pixel	KU modified prod. 1 – unshielded
Hexagon column	KU modified prod. 1 – unshielded
Double pixel	GE board BJT + BB amp – shielded
Single pixel	GE board BJT + GALI – shielded
ATLAS P2 50x50 poly connection	KU modified prod. 1 – unshielded
Diamond 110	KU modified prod. 2
Diamond 55	KU modified prod. 2

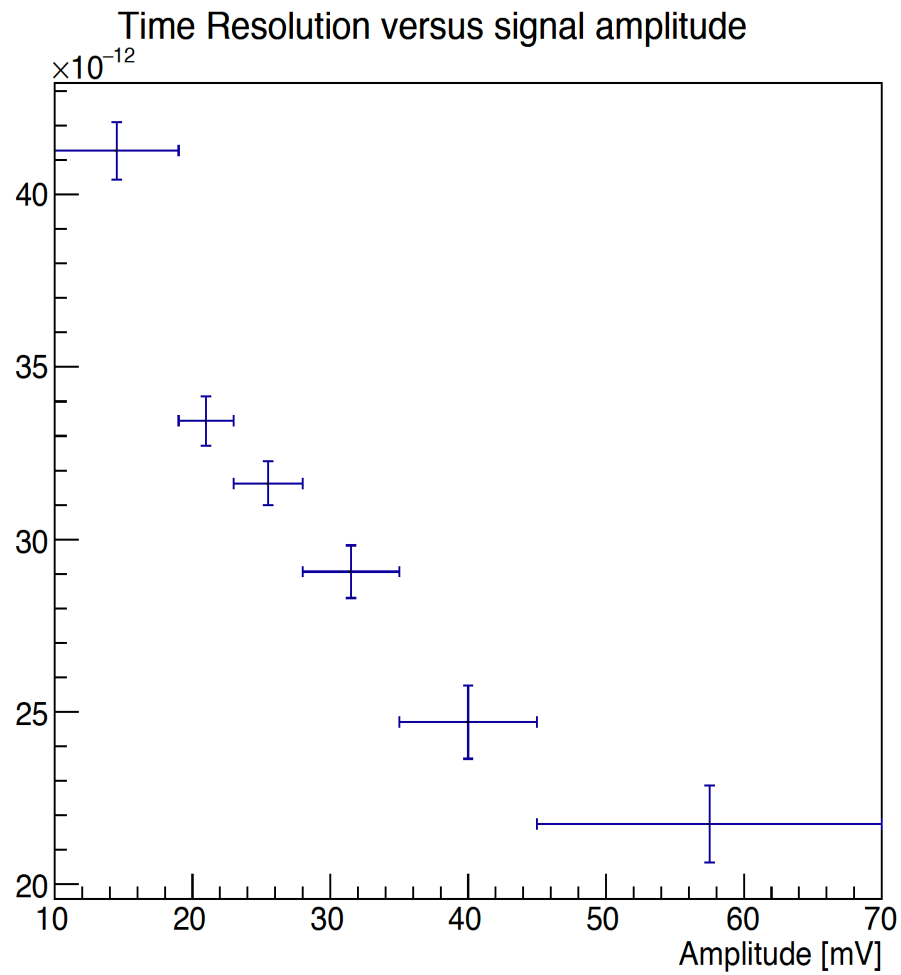


σ_t = 24.6 ps on Δt between MCP channels

- Trigger is on DUT;
- Waveforms of DUT, MCP1 and MCP2 (and RF) are entirely acquired by the scope;
- DUT time is calculated by applying a numerical CFD algorithm, taking time at 35% of the DUT waveform maximum;
- MCP1 and 2 average time is calculated and used to measure Δt w.r.t. DUT time.

Amplitudes and Time resolutions



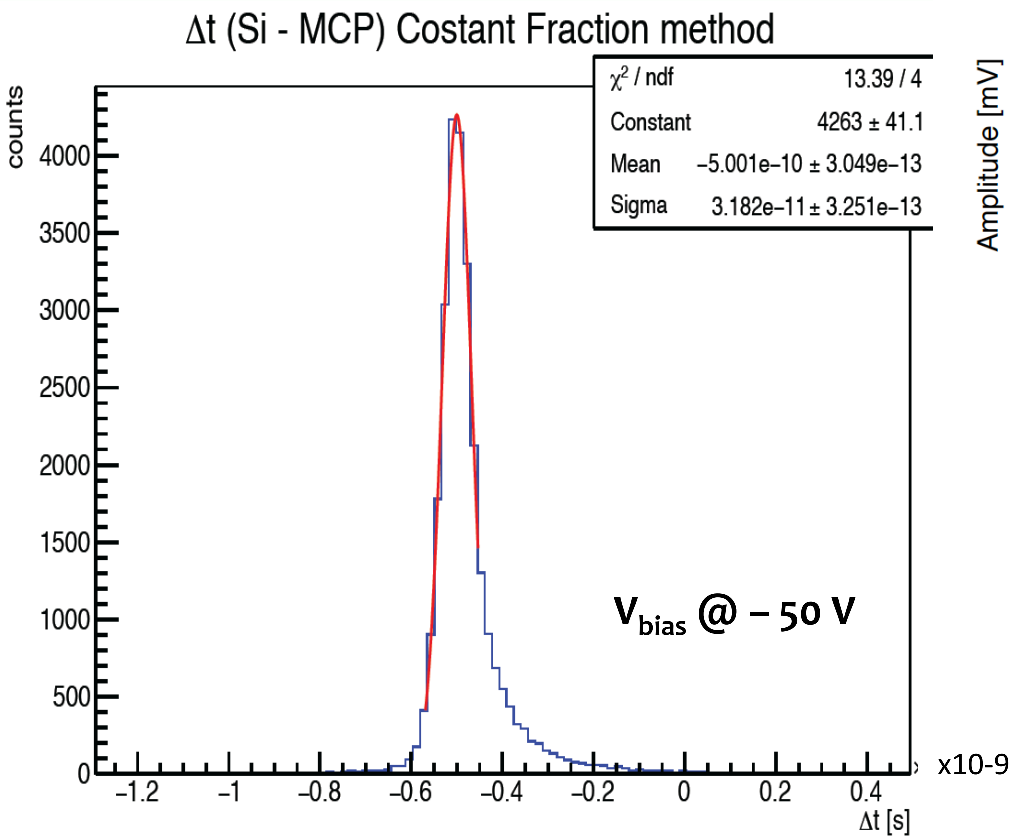


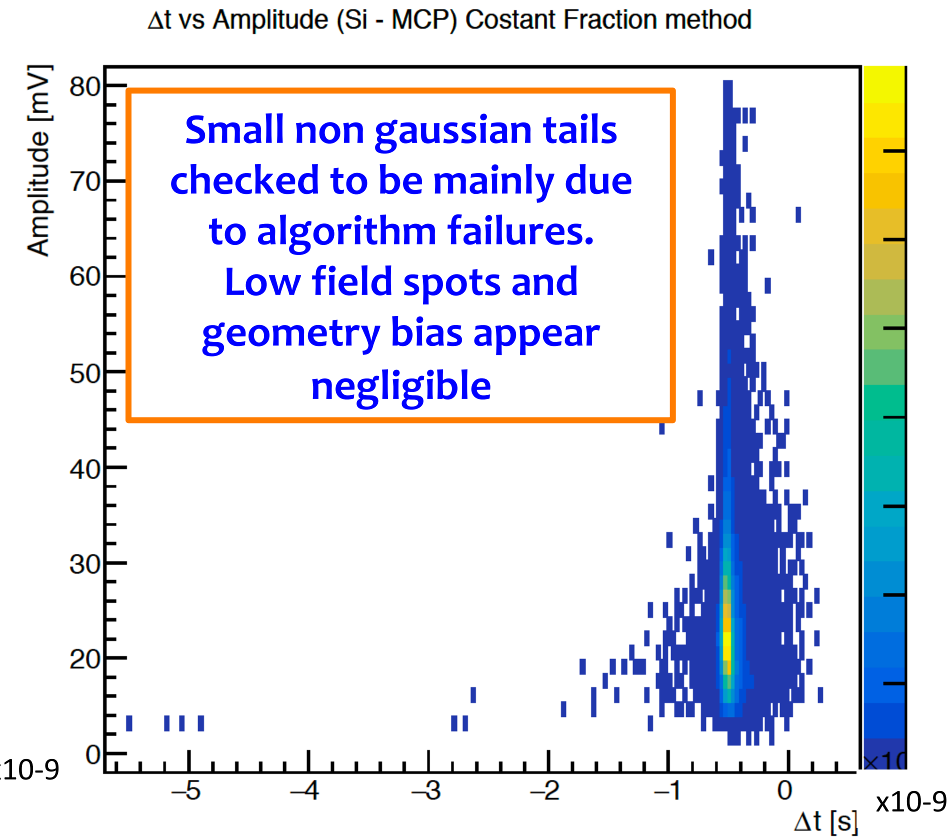
Fit of amplitude distribution with a gaussian convoluted with a Landau function.
The effect of trigger threshold is taken into account by a suitable efficiency function

The amplitude fit ensures that MIPs are acquired (+ noise)

Time resolution

of TIMESPOT 3D trench pixels





σ_t = 31.8 ps before de-correlation with Time Tagger time measurement

time resolution MCP method CFD 2.599e-11 +/-1.255e-13
time resolution Si method CFD 3.182e-11 +/-3.291e-13
time resolution Si1 method CFD 3.495e-11 +/-3.294e-13
time resolution Si2 method CFD 3.513e-11 +/-3.342e-13

time resolution MCP1 = 1.821e-11
time resolution MCP2 = 1.855e-11

σ_t = 29.8 ps after de-correlation

σ_t table of measurements (only indicative, still under study)

Test structure	Front-end	σ_t
Pixel strip	KU* modified prod. 1 – unshielded	40 – 50 ps
Single pixel	KU modified prod. 1 – unshielded	~ 40 ps
Hexagonal column (FBK DS process)	KU modified prod. 1 – unshielded	~ 60 ps
Double pixel	GE** board SiGe BJT + BB amp – shielded	~ 30 ps
Single pixel	GE board SiGe BJT + GALI – shielded	Bad (Oscillations)
ATLAS Phase2 50x50 with poly connection	KU modified prod. 1 – unshielded	High values (>100 ps) to be better studied.
Diamond 110	KU modified prod. 2	Under analysis. Smaller S/N ratio
Diamond 55	KU modified prod. 2	Under analysis. Smaller S/N ratio

*Kansas University

**INFN Genova

- Performance appear strongly limited by electronics and extrinsic noise (pick-up from EM enviroment, especially MCP). A better/dedicated electronics is needed.
- For practical reasons only collective and wire-bonded pixel structures have been tested (x10 increase in Capacitance)
- Final answer will be given using an integrated front-end

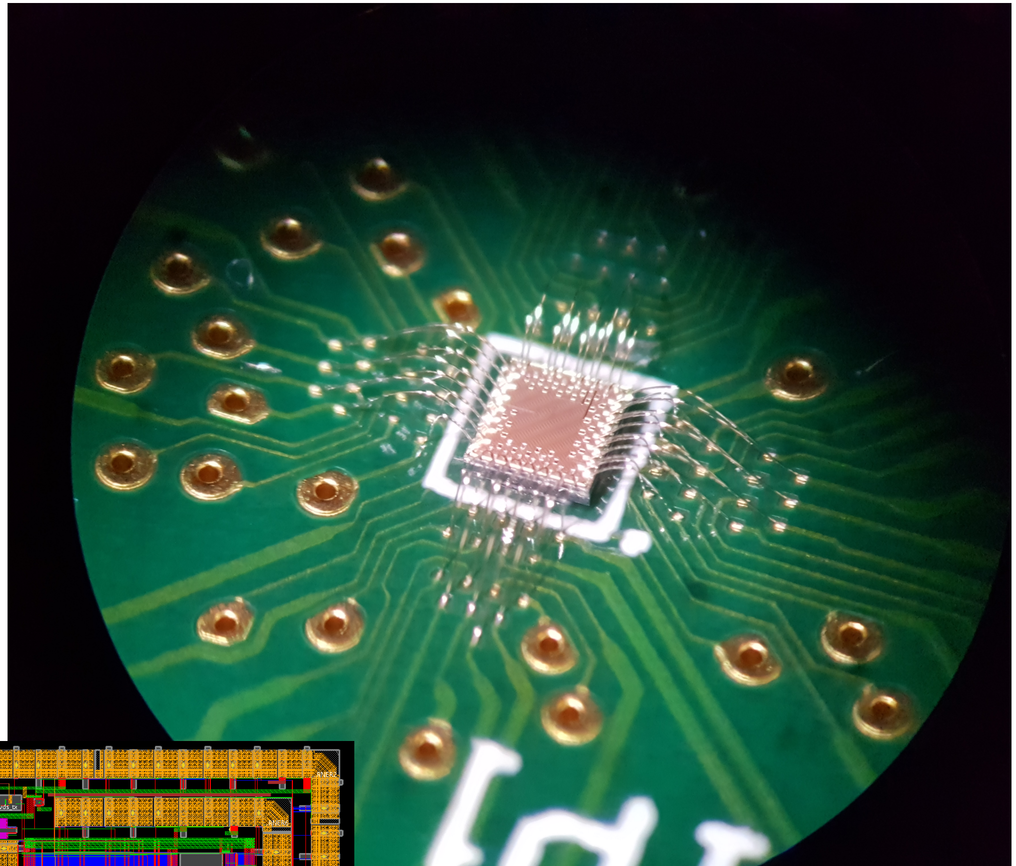
1st prototype in 28-nm CMOS
(presently under test)

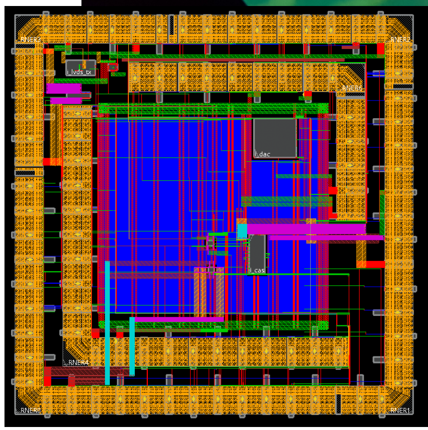
- Main purpose: gain confidence on 28-nm CMOS and test technology performance.
- All cells are kept independent and directly accessible from external pins (with a few exceptions)

  → strongly pad-limited

Integrated cells:

- 3 different TDC solutions
- 6-bit DAC + SPI I/F
- 8-channels CSA+Discriminator
- Programmable power (and speed)
- General purpose OPAMP
- LVDS Tx/Rx



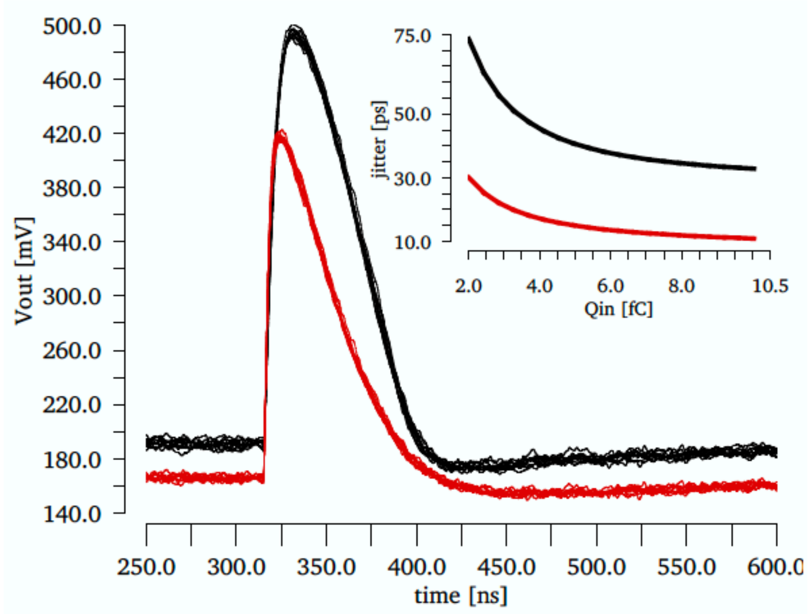


Total area 1.5x1.5 mm^2
mini@sic

CSA and TDC expected performance

Input Signal	Delta		Sensor	
Power [μW]	*4.1*	*7.2*	*4.1*	*7.2*
G [mV fC^{-1}]	190	168	150	124
σ_n [mV]	2.8	2.0	2.8	2.0
ENC [e]	94	77	120	103
t_{pk} [ns]	16.4	7.7	18.2	10.2
t_A [ns]	2.1	2.1	4.2	3.5
TOT [ns]	100	98	79	78
SR [mV ns^{-1}]	53	98	39	68
σ_j [ps]	54	21	74	30
σ_p [ps]	66	65	67	66
σ_{mm} [ps]	33	26	40	29

CSA performance is limited by power budget (limit was self-imposed)



TDC schemes

	DCO (dithering)	Tapped delay	Time Amplifier
Size (μm^2)	23 x 22	27 x 22	23 x 21
LSB (ps)	190	50	22
RMS (ps)	47	15	37
Power Active (μW)	1200	1200	65
Power Standby (μW)	10	10	34

PrototipoZero: 1st results

LVDS transmitter and receiver in loopback configuration.

ATLAS AM08 design

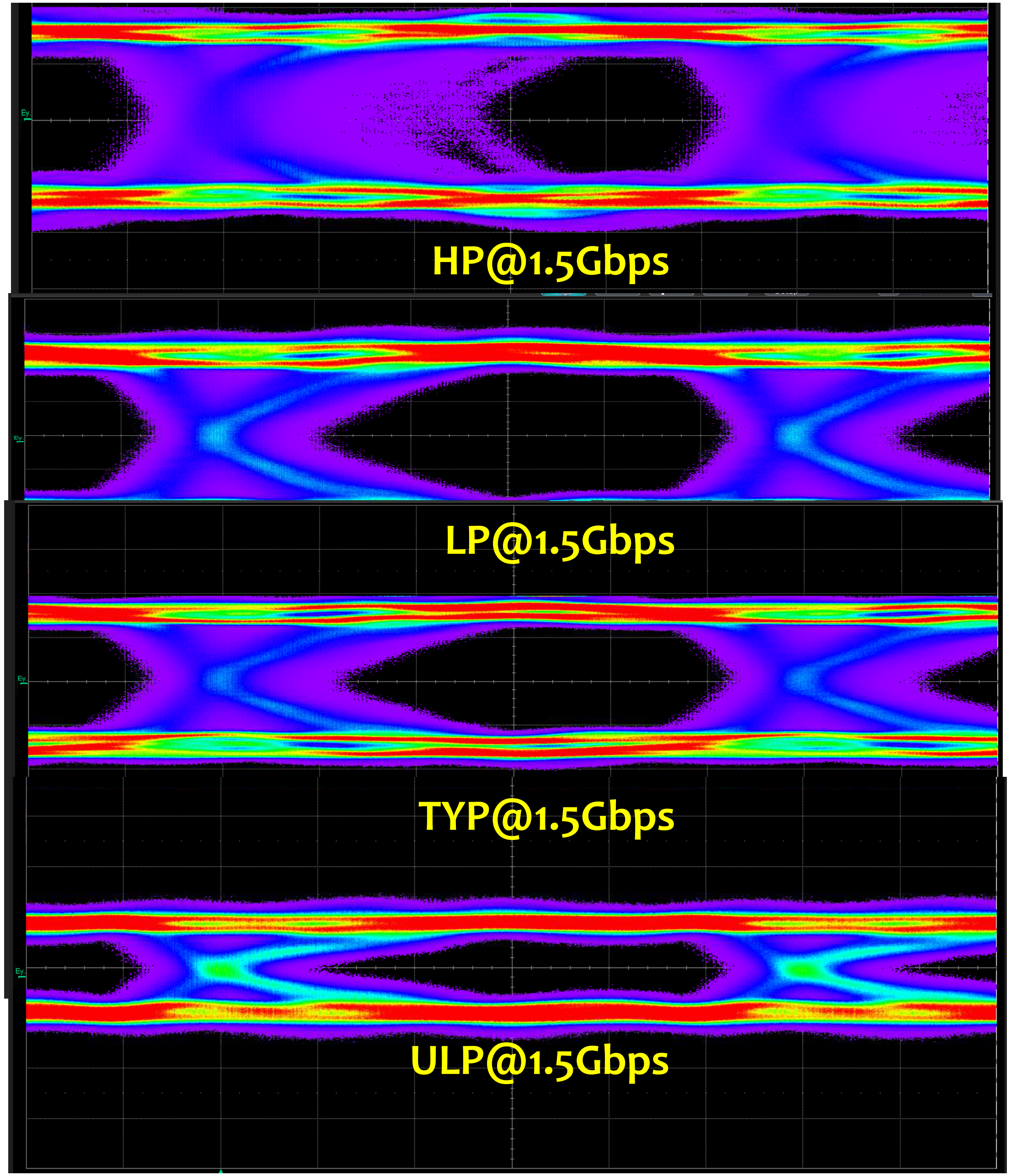
(Designers: G. Traversi & F. De Canio, Bergamo group)

The loopback have a nice eye (Bit Error Ratio $< 10^{15}$ @ 1.5 Gbps and low-power mode). AM08 specs is 1.0 Gbps.

This is a very good result by considering that PrototypeZero is wire-bonded and without decoupling capacitors

The LVDS link is "silicon proof" in all modes @1.5 GBps:

- **Ultra-Low-Power (ULP, 1.6 mA),**
- **Low-Power (LP, 2.7 mA),**
- **Typical (TYP, 4.1 mA)**
- **High Power (HP, 8.1 mA)**



Conclusions

- First unprecedented results on trench 3D Si pixels timing performance have been presented
- The time resolution of trench 3D sensor, 55x55x150 μm^3 , under laser beam has been measured being around 20 ps under 1-MIP-estimated deposit charge.
- The time resolution of the same sensor measured under a 270 MeV/c π^+ beam has been measured up to 30 ps
- 3D devices confirm their theoretical excellent performance in timing. Trench geometry shows up being the right direction to go
- Electronics appear to be the limiting factor to system performance
- Optimized electronics design is necessary to achieve the target performance at a system level (both in the lab and in apparatus)
- Further studies on the test beam data and on 28-nm CMOS IC are on the way. Results will be presented very soon.